

Preface

The commercial success of semiconductor industry is mainly driven by the continuous scaling of CMOS and the proceeding functional integration in system on chip applications. Reaching the nanometer scale severe scaling limitations enforce the introduction of novel materials, device architectures and device concepts. Multi-gate FETs employing high-k gate dielectrics are considered as promising solution overcoming the scaling limitations of conventional planar bulk CMOS. Especially analog, mixed-signal and RF device and circuit performance is affected by these revolutionary changes in technology. This work provides a technology oriented assessment of analog and mixed-signal circuits in emerging multi-gate CMOS technologies. On device level, the reduction of short channel effects is a major advantage of fully depleted multi-gate devices, resulting in beneficial output impedance, gain and matching behavior. Serious concerns related to high-k dielectrics are pronounced flicker noise and dynamic threshold voltage variations or hysteresis effects. The impact of flicker noise on circuits and noise reduction techniques are briefly discussed. A model for hysteresis effects is derived and applied in a systematic analysis on circuit level. Simulation and measurement results indicate, that moderate hysteresis effects are no show stopper for analog and mixed signal. Nevertheless exceptional cases have to be considered, corresponding countermeasures on circuit level are proposed and verified on silicon. The feasibility of important analog, mixed-signal and RF building blocks in an emerging multi-gate technology is proven by measurements, the performance is benchmarked against planar bulk. Multi-gate device specific design aspects are pointed out. Benefits on circuit level resulting from advantageous multi-gate device properties are explored: improved robustness and gain is demonstrated for current references and operational amplifiers. A significant reduction of circuit area is achieved for a 10 bit D/A converter. The use of gated p-i-n diodes in bandgap reference circuits is evaluated, a corresponding model covering temperature dependence is derived. Low-voltage bandgap references show competitive performance. Measured VCO and LNA characteristics indicate no road blocks for RF applications in the low GHz domain. Promising noise and jitter performance is demonstrated in a charge-pump PLL. Further multi-gate related design aspects like self-heating and selective tuning of fin width are outlined. Finally the integration of tunneling FETs in a low-power multi-gate technology is discussed as outlook

to analog design aspects beyond CMOS. Although these devices feature low on-currents, promising analog properties and low variability regarding temperature and threshold voltage are demonstrated. Gate stack engineering and tuning of doping profiles are suited for device optimization. A TFET reference circuit is developed, robust against temperature and supply voltage variations.

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