

## Chapter 2

# Capacitive Sensing Electrodes

The capacitive sensing electrodes on the top of a CMOS chip serve as an interface between the microelectronic readout system and the biological/chemical analyte. These electrodes are directly exposed to the analyte or an intermediate layer which will be described in Chapter 3 (Fig. 2.1). The sensing electrode can be realized by a standard CMOS process. However for some applications, further micromachining procedure may be necessary.

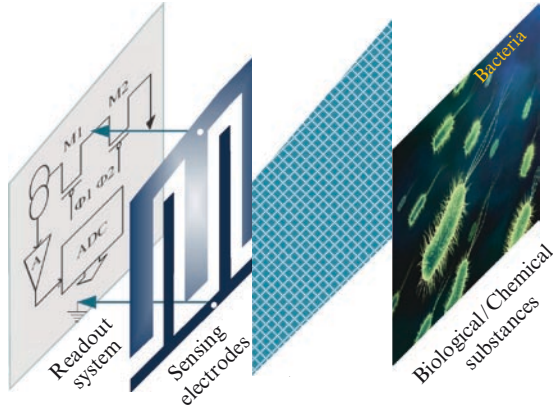
In this chapter, we first describe the various configurations of sensing electrodes created above the CMOS chip for various applications, and then we will discuss the electrical model and associated parasitic capacitances of sensing electrodes.

### 2.1 On-Chip Microelectrode Configurations

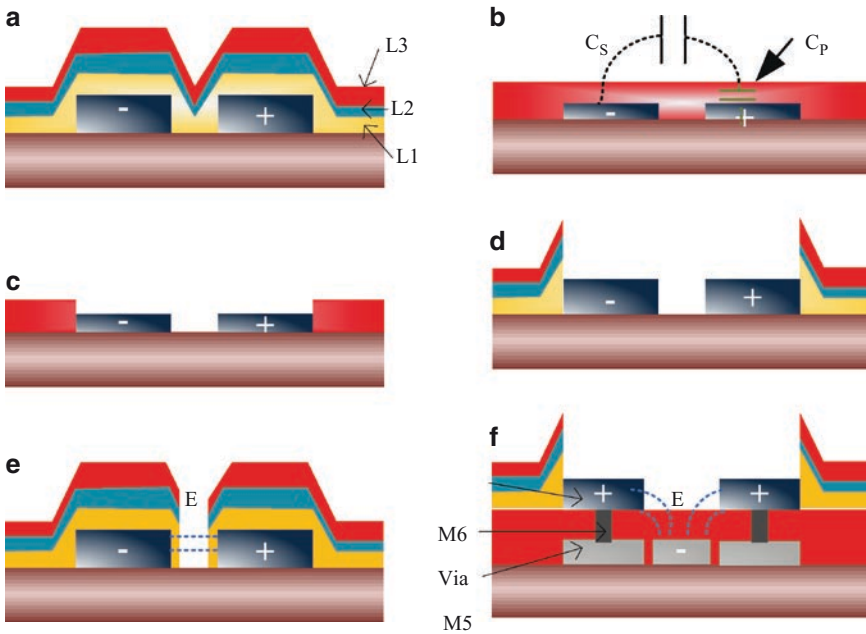
The design and implementation of sensing electrode can be done using Virtuoso layout editor software using the top most metal layer (e.g. metal 6 in 0.18 CMOS process) [141]. Sensing can be performed using various configurations as shown in Fig. 2.2.

#### 2.1.1 Passivated Electrodes

In standard CMOS technology such as 0.18  $\mu\text{m}$  process (Fig. 2.2a), the passivation layers including silicon oxide, silicon nitride and polyamide are stacked in the last step of the process. A thin passivation layer (Fig. 2.2b) with uniform thickness is a good candidate for cell growth monitoring [142–144]. In this case, a large parasitic capacitance  $C_p$  (e.g. 0.5  $\mu\text{m}$  CMOS process, 0.05  $\text{fF}/\mu\text{m}^2$  [75]) is created across the passivation layer. Therefore, the equivalent capacitance of the parasitic capacitance in series with a sensing capacitance  $C_s$  is approximately equal to sensing capacitance alone (see Fig. 2.2b).



**Fig. 2.1** CMOS based capacitive sensing LoC



**Fig. 2.2** Sensing electrodes realized atop a CMOS chip: **(a)** thick metal with three passivated layers, **(b)** thin metal with a passivated layer, **(c)** open-top thin metal electrode, **(d)** open-top thick metal electrode, **(e)** passivation electrode with a window in between the fingers, and **(f)** open-top electrodes with two metal layers

### 2.1.2 *Unpassivated Electrodes*

Aluminum is still the major material used for electrical contacts and interconnections in CMOS circuits. The top most metal layer in standard CMOS processes is basically made of aluminum plus a small impurity concentration of silicon (e.g. 0.18 CMOS, Al/1%Si, Al with 1% Silicon) [64, 145]. Aluminum is not widely used for biosensing purposes as opposed to gold and platinum. Due to the oxidizing property of the biological and chemical analytes, if a durable conductive electrode is required, only noble metals like gold (Au) and platinum (Pt) can be used but not aluminum (Al). Despite this, a native  $\text{Al}_2\text{O}_3$  layer ( $\approx 10$  nm) on the surface of Al is considered an advantage for biosensing applications [146]. This insulation layer makes the sensor more durable in typical biosensor environments. The viability of Al (along with the  $\text{Al}_2\text{O}_3$  layer) as a sensing electrode has already been demonstrated for DNA detection and bacteria sensing [147, 148].

The passivation layers can be removed from the top of the electrodes in order to make a direct contact with the Al electrode (Figs. 2.2c). The “Pad” mask layer in this technology can be selected by the designer if needed. By increasing the height of the sensing electrode, the distribution of electric field and the performance of the biosensor can be improved significantly. As shown in Fig. 2.2d, by selecting a thick topmost metal layer in CMOS process and also by selecting a pad-etch mask, a larger space in between the electrodes can be made. A strong electrical field is created in this space because the electric field is generated by the parallel electrodes. The sensing electrodes realized in a thin topmost metal layer (Fig. 2.2c) can only detect the bioparticles in the top of the sensing electrodes, of course with less electric field lines.

### 2.1.3 *Sensitivity-Enhanced Passivated Electrodes*

The passivation layer in between the fingers can be removed in order to increase the sensitivity and dynamic range of sensing electrodes. As shown in Fig. 2.2e, the electric field in between the passivated electrodes become very strong, so that, the presence of bioparticles can significantly vary the sensing capacitance. The viability of this technique has already been demonstrated for the detection of liquid phase organic solvents [140].

### 2.1.4 *Quasi Interdigitated Electrodes*

In addition to selecting thick or thin metal layers, combining the electrodes from the two top most metal layers can improve the electric field (E) and subsequently

the sensitivity. As shown in Fig. 2.2f, by selecting the topmost metal layer (e.g. metal 6 in 0.18 CMOS process) as the working electrode (including the sensing area), and by connecting ground to another electrode realized in the second metal layer (e.g. metal 5 in 0.18 CMOS process), a strong electric field can be created. This quasi interdigitated electrode with further polymer formation processes has already been reported for a CMOS-based gas sensor [149].

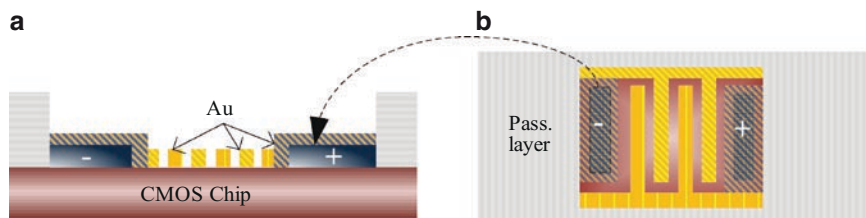
### 2.1.5 Gold Electrodes on CMOS Chip

Gold is used extensively as sensing electrodes for biomedical applications and is generally considered to be biocompatible [150–152]. While other less noble metal, such as platinum or iridium are oxidized to a depth of hundreds of nanometers, gold is a stable noble metal and a far better electron conductor than aluminum, copper or even silver. This highly defined and conductive surface of gold may be ideal for several biosensing applications including bacterial growth monitoring, virus detection, and DNA detection [153–155]. Furthermore, gold as a result of its unique surface chemistry allows for the self-assembly of organic molecules, through sulphur atoms. Such a self-assembled monolayer (SAM) can be used as a linker between gold sensing electrodes recognition layer [156, 157].

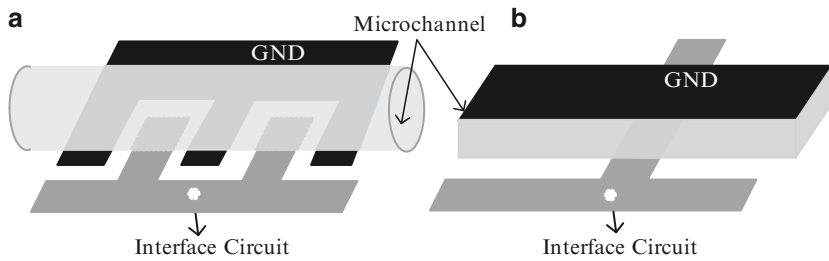
The gold layer can readily be fabricated using commercially available lithographic technologies on chip using CMOS compatible micromachining procedures at low temperature [158–162]. Figure 2.3a, b shows an illustration of gold electrode created above a CMOS chip. Section 2.3 presents the post-processing of gold on CMOS chip.

### 2.1.6 Microfluidic Channel Integrated Atop Sensing Electrodes

The sensing electrodes are usually realized on the same chip of capacitive interface circuit and a microfluidic channel is used to direct the biological fluid toward sensing site as seen in Fig. 2.4a [163, 164]. However, some rapid prototyping



**Fig. 2.3** Illustration of on-chip gold electrodes: (a) cross section and (b) top view of gold electrode on CMOS chip



**Fig. 2.4** Schematic representation of sensing electrodes incorporated with a microchannel: (a) interdigitated electrode and (b) configuration presented in [165]

methods have alternatively been reported to detect the bioparticles through the capacitive sensors created in between one electrode on the chip and another electrode between the chip and a grounded electrode above the chip as shown in Fig. 2.4b [165]. This figure shows a capacitive sensor including a common ground electrode on the top of microfluidic packaging. This technique can improve the dynamic range of the sensor by increasing the applied voltage.

## 2.2 Micromachining Gold Electrode on CMOS Chip

Extra micromachining procedures should also be performed to connect the deposited gold to underneath circuitry deep in the CMOS chip. Figure 2.5a–o depicts the micromachining steps to make gold electrodes atop a CMOS chip [158–162].

*Step 1:* Figure 2.5a shows a fabricated CMOS chip with two electrodes realized in two successive metal layers (e.g. Metal 5 and Metal 6 in 0.18 CMOS process). The pad-etch technique can be applied to remove the passivation layer.

After removing the passivation layers, the same passivation layers are deposited in order to create a small precise opening above the top most metal layer.

*Step 2:* A thin layer of silicon oxide is deposited (Fig. 2.5b).

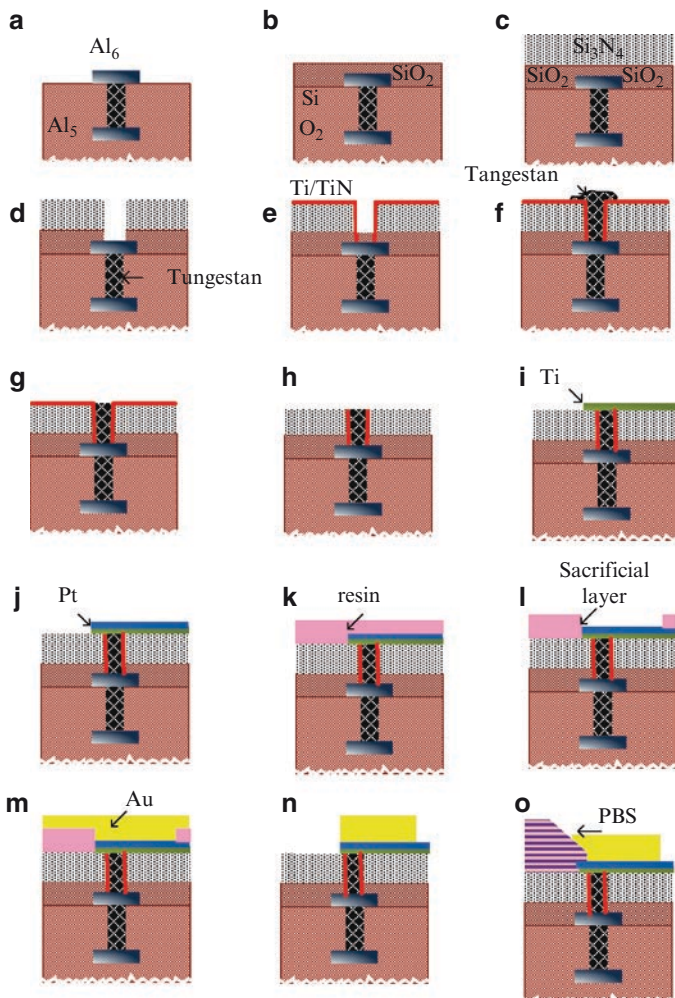
*Step 3:* Silicon nitride is deposited (Fig. 2.5c).

*Step 4:* An opening above an Al electrode is created (Fig. 2.5d).

*Step 5:* Thereafter, the top of the passivation layer and the inside of the opening is coated in subsequently deposition with titanium (Ti) and titanium nitride (TiN), generally using a reactive magnetron sputtering technique (Fig. 2.5e). TiN is an excellent diffusion barrier material that is used in the advanced metallization step of integrated circuit manufacturing processes in particular for contact and via. TiN separates tungsten which is used as conductive via from titanium and silicon dioxide in order to avoid the interaction between contiguous layers.

*Step 6:* The opening is thereafter filled with a tungsten material (Fig. 2.5f).

*Step 7:* An etching process is performed in order to form a fine via between the Al<sub>6</sub> and the gold electrode (Fig. 2.5g).



**Fig. 2.5** On-chip gold deposition method: (a) fabricated CMOS chip, (b) silicon oxide and (c) silicon nitride depositions, (d) opening, (e) Ti/TiN deposition, (f) tungsten filling, (g) etching process, (h) Ti/TiN removal, (i) Ti deposition, (j) Pt deposition, (k) resin deposition, (l) sacrificial layer patterning, (m) gold deposition, (n) lift-off, and (o) PBC creation

*Step 8:* In the next step, the barrier layer is removed from the top of the silicon nitride passivation layer (Fig. 2.4h).

*Step 9:* Ti is deposited (Fig. 2.5i).

*Step 10:* The double layer of Ti/Pt is created above the tungsten via by depositing Pt above Ti (Fig. 2.5j).

*Step 11:* A thin layer of resin is deposited (Fig. 2.5k).

*Step 12:* This resin layer is patterned above Ti/Pt double layer (Fig. 2.5l).

*Step 13:* An appropriate thicknesses of Au is deposited (e.g. Ti: 50 nm/Pt: 50 nm/Au: 500 nm [22]) as shown in Fig. 2.5m.

*Step 14:* Using a lift-off process, the sacrificial layer along with Ti/Pt/Au on top of sacrificial layer are etched in order to create a gold electrode connected to the  $Al_0$  through a tungsten via and Ti/Pt (Fig. 2.5n).

*Step 15:* A resist layer such as polybenzoxazole (PBS) is coated on the top of gold electrode and other parts of chip. This layer is thereafter developed and baked at a given temperature (Fig. 2.5o).

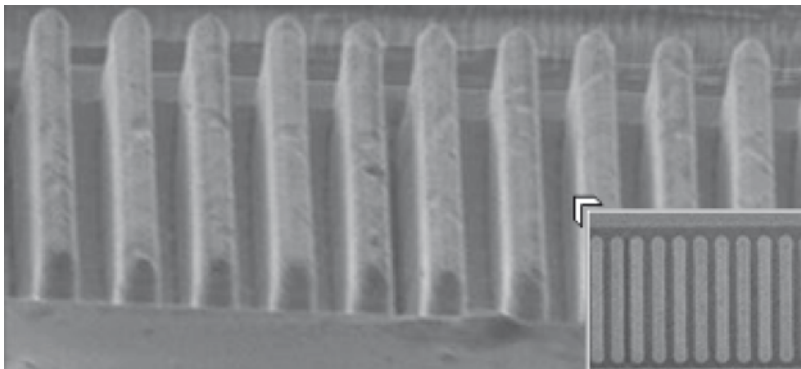
## 2.3 Electrical Model of Sensing Electrodes

A capacitive sensor with an interdigitated electrode on the top of a CMOS chip is implemented in order to detect the minute variations of capacitance on the sensing electrodes which are associated with large parasitic capacitances.

Figure 2.6 shows a SEM image of a sensing electrode where the passivation layers in between the electrodes have been removed [166]. The presence of analyte in between the fingers or above the electrodes can be detected by sensing electrodes. This figure shows the electrode from top and a 45° view. The width and the space between the fingers are about 10  $\mu\text{m}$  approximately.

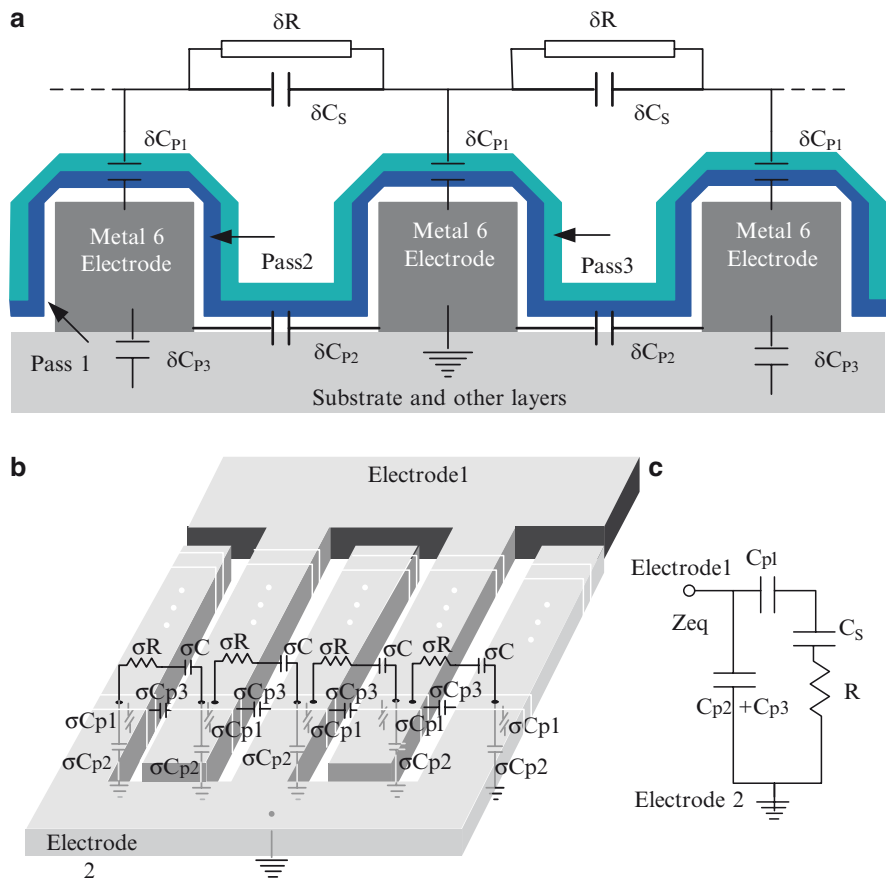
These parasitic capacitances and the equivalent circuit model of the sample are shown in Fig. 2.7. As seen in this figure, the capacitive and resistive properties of analyte are modeled by a parallel capacitance ( $C_s$ ) and resistance ( $R$ ). The parasitic capacitances across the passivation layer ( $C_{p1}$ ), in-between the electrodes ( $C_{p2}$ ) and in between silicon substrate and electrodes ( $C_{p3}$ ) are also shown in this model.

In fact,  $R$  and  $C_s$  can be obtained from the parallel combination of a large number of small elements ( $\delta C_s$ ,  $\delta R$ ). As seen in Fig. 2.7a, b, by assuming the same values for  $\delta C$  and  $\delta R$  in each branch, the dropped voltage  $V$  on this parallel combination



**Fig. 2.6** SEM image of implemented sensing electrode on CMOS chip seen from two different view angles





**Fig. 2.7** Illustration of (a) and (b) parasitics generated on top of a CMOS chip ( $\delta C$  and  $\delta R$  are the partial parasitic capacitance and resistance respectively), and (c) its equivalent circuit

results in a current  $I = I_1 + I_2 + \dots + I_n = nI_1$ . Considering the Laplace transform of  $I_1(S) = V(S)/(\delta R + 1/\delta C_s S)$ , therefore,  $I(S) = nI_1(S) = V(S)/(\delta R/n + 1/n\delta C_s S)$ .

In other words, by considering the above mentioned assumptions and  $I_1(0) = I_2(0) = \dots = I_n(0) = 0$ , the equivalent resistance and capacitance become  $R \approx \delta R/n$  and  $C_s \approx n\delta C_s$  respectively where the electrode is broken into  $n$  finite elements. Based on this discussion, the interdigitated electrodes with large number of fingers result in a large equivalent capacitance and a small resistance. The equivalent circuit shown in Fig. 2.7c is obtained for the capacitive electrode realized through a CMOS process. The parallel resistor and capacitor in this model is presented as an example. It should be mentioned that many other electrical models for biological and chemical samples have been documented for different applications [167].



## 2.4 Summary

In this chapter, we introduced with different methods used to realize sensing electrodes above CMOS chips. Corresponding to each biosensing method, the configuration of the sensing electrode is selected. The main advantage of these on-chip configurations is the simplicity of design and fabrication. However there are several limitations in selecting the materials exposed to analyte or the minimum dimensions. The modern nano-scale CMOS processes offer the implementation of large arrays of nanoscale electrodes; however in selecting the CMOS process, a compromise should be made between the minimum feature of the sensing electrodes, the applied voltage/current and the speed of sensor.

CMOS Capacitive Sensors for Lab-on-Chip Applications

A Multidisciplinary Approach

Ghafari-Zadeh, E.; Sawan, M.

2010, X, 146 p., Hardcover

ISBN: 978-90-481-3726-8