

# CHALLENGES OF COMPLETE CMOS/MEMS SYSTEMS INTEGRATION

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**Abstract** This paper is dedicated to the analysis of the needs and challenges of integration of CMOS and MEMS. It is acknowledged that individual sensors era is ending and the multi-sensor micro-systems era is beginning. On the example of cost requirements for IMU for high volume cell phone application it is demonstrated that achievement of required cost target is possible with monolithic MEMS CMOS integration. Among major challenges of this integration are: need for sensors sensitivity increase, as the way to scale their size down; process integration for different sensors and compatibility of this process with CMOS fabrication technology. General description of Siantis' technology, which met all major challenges of monolithic integration, is presented then. Finally, economic justification for monolithic integration is considered.

**Keywords:** CMOS MEMS integration, pressure sensor, accelerometer, piezoresistor, piezo-transistor, micro-structure, multi-sensor micro-systems, inertial measurement unit, sensitive integrated circuits, principle of multi-axis measurements.

## 1. Need for monolithic integration

Even before the term "MEMS" was coined and established, some of the early pioneers in this field envisioned ultimate monolithic integration of MEMS and ICs. Over three decades has passed and this is not yet a main stream technology in MEMS. However, the most significant MEMS products, like print-heads, ADI's accelerometers, TI's DLP, are utilizing monolithic integration. Their commercial success is the best evidence of this ultimate technological goal.

Nobody is arguing today that integration of MEMS and sensors in particular with CMOS is the next natural step in micro-technology evolution. Many researchers and companies are working in this direction addressing specific devices, applications and markets. Very good example of this effort is an initiative of Ken Wise, who founded Engineering Research Center for Wireless Integrated Microsystems (WIMS) funded by NSF in 2000. The center combined efforts of

about eight universities in creating microsystems capable of measuring a variety of physical parameters, interpreting the data and communicating over a wireless link [1].

The dramatic difference between what the market was looking for yet several years ago and now is the need for simultaneous measurements of multiple parameters of different physical and/or chemical domains. Several examples of these market needs are shown in Figure 1.

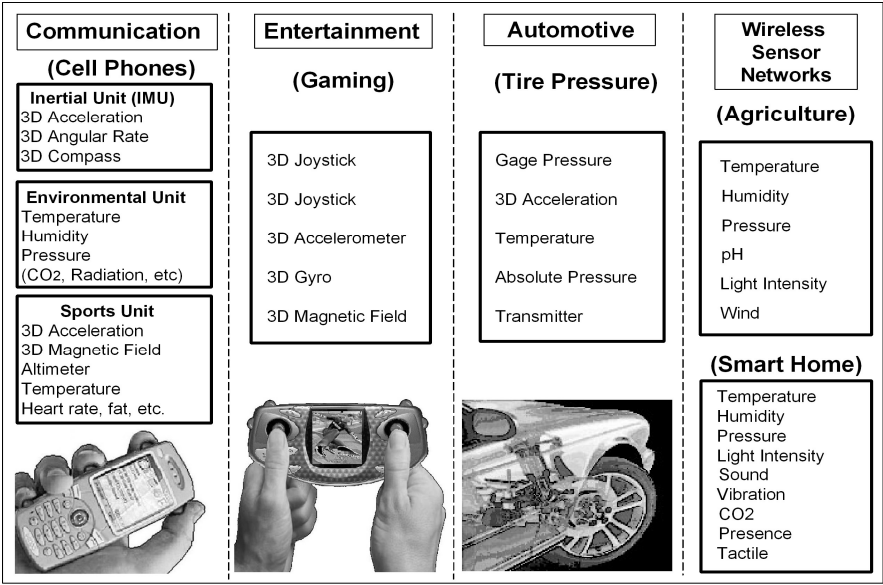


Figure 1. Examples of market need in micro-systems measuring multiple parameters.

It becomes obvious that Individual Sensors Era is ending. Multi-Sensor Micro-Systems Era is beginning.

Why is it happening now? The market is ready to accept and utilize huge amount of such systems for different high volume applications – market pull. The underlying technologies are developed enough to push the market. These are technologies in all three areas: sensing, computing and communicating. However, for all massive applications the major requirements are: low cost, small size, high reliability.

What kind of integration monolithic or hybrid would be better? Older generation of semiconductor industry professionals might remember that at the beginning of IC there were a lot of discussions about “monolithic” vs “hybrid” integration. The real life put everything on its place and brought an understanding that both approaches have the right to live depending mainly on the size of the market and related cost requirements.

Principally the history is repeating itself on the example of MEMS and CMOS integration. There are the same two basic approaches: hybrid (MCM) and monolithic, although the border between those two is fading with the advance of new technologies and processes. For example, when two silicon wafers, one with CMOS and another with MEMS, are bonded at the wafer level, it is certainly not a traditional hybrid integration but although not yet true monolithic. To add here chip-scale packaging (CSP), wafer-level packaging, through silicon vias (TSV), vertical multi-chip packaging, and we have even fuzzier line between two basic integration approaches. So the correct question should be not “Which MEMS/CMOS integration technology is better?” but rather “When different MEMS/CMOS integration technologies should be used?” By the other words the question should be: “When monolithic integration should be used instead of MCM, assuming that all technological issues of this integration are resolved for a given application?”

Let us consider an example of cost requirements for portable devices. How low the cost, how small the size and how high the reliability should be for these multi-sensor micro-systems depends on specific applications. For example, very high volume cell phone market is looking now for not just 3-axis accelerometer, which is already started to be implemented in some high-end phones, but for whole inertial measurement unit (IMU) for many potential applications, as shown in Figure 1. In particular it can be used for navigation assisting GPS between the transmissions and for navigation in the areas shielded from radio signals. Such multi-sensor micro-system should comprise at least three different sensors: 3-axis linear accelerometer, 3-axis angular sensor, 3-axis compass and CMOS processing circuitry. In some other requirements it also might have an altimeter for measuring elevation, for example within a building. Figure 2 illustrates the pie-chart of the six most important cost components including packaging and testing.

Sooner or later this technology will penetrate into all cell phones. It was reported that the bill of materials (BOM) for the low-end cell phones is approaching \$20. Let us aggressively assume that the cost of new component might be allowed at 10% of BOM, e.g. \$2. Let us also assume for the sake of discussion that this total cost of IMU will be equally broken down between six cost components. Then each of the 3-axis linear accelerometer, 3-axis angular sensor, 3-axis compass, CMOS, packaging and testing should cost \$0.33.

Is it realistic to achieve this low cost for all these separate components? The answer is “definitely not” without integration. Is it realistic to achieve this low cost with hybrid (MCM) integration? I would say: “Doubtfully” because there is no evidence that within the existing trend of scaling down the size and therefore the cost of 3-axis accelerometers and gyro the price \$0.33 per chip-packaged 3-axis device could be achieved soon.

Is it realistic to achieve this low cost with monolithic integration? The answer is “definitely yes”. More than that, the monolithic integration seems to be the only way to achieve this goal for such high volume application.

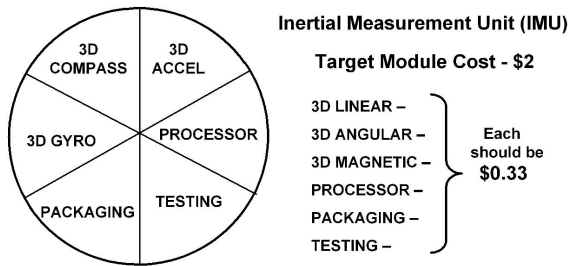


Figure 2. Cost structure of the inertial measurement unit components.

## 2. Major challenges of monolithic integration

What are the major challenges for achieving monolithic integration of MEMS sensors with CMOS?

The first and probably the main challenge is how to decrease the size (area) of the sensors shared with CMOS at the surface of the die. There are several obvious reasons for that. Multiple sensors require overall *size* reduction. Integration with IC and wireless requires smaller sensor *size*. Lower cost requires smaller *size*. But smaller sensors size typically infers lower sensor sensitivity. For a given application the required sensitivity is determined and therefore, the size of the sensor for a given technology is also determined. If sensor sensitivity can be increased with a new technology, then the size of the sensor can be decreased while still providing the required sensitivity.

The second challenge is different sensors process compatibility, meaning how to develop such fabrication process, which would allow fabrication of different multi-axis sensors at the same time.

The third major challenge is the selection of such additional materials and processes required for fabrication of different sensors that are CMOS process compatible, which would manifest MEMS CMOS monolithic integration.

Siantis successfully met all three major challenges of CMOS and sensors monolithic integration by:

1. Decreasing sensors size and providing their future scalability by increased sensitivity.
2. Providing unified sensing and processing components platform and novel microstructures.
3. Developing unified fabrication process for different sensors.
4. Using monocrystalline silicon as both a mechanical material for microstructures and a substrate for electronic components and also developing a two-stage process (CMOS first, MEMS second) allowing monolithic integration of CMOS with different sensors.

Foundation of Siantis' Technology for Sensitivity and Functionality Increase/Size and Cost Decrease comprises:

1. Big mechanical input element relative to small sensor size – *Novel Microstructures*.
2. Multiple sensitive components within multiple suspensions and *Simple Microstructure for multi-axis measurements*.
3. CMOS transistors as both sensitive and processing components – *Unified Component Platform*.
4. Collecting more energy induced by measurand – *Sensitive Integrated Circuits*.

### 3. Novel microstructures

On the example of mechanical sensors, such as accelerometers and gyros, let us look at the important criteria for their mechanical microstructures for the purpose of increasing their sensitivity and scaling size down. Table 1 summarizes these requirements.

TABLE 1. Requirements for mechanical sensors microstructure.

Bigger proof mass	Stronger silicon suspension	Simple mechan. structure
High sensitivity	High reliability	High reliability
High resolution	High shock protection	Better stability
Small mechanical noise	No stiction	Sensor size scaling
Better mass reproducibility	Wide frequency bandwidth	
Stronger suspension	High long-term stability	
Sensor size scaling	High yield	

There are many limiting factors for scaling down mechanical sensors. Physical principle, fabrication technology, microstructure and noise are among them. For example, all existing capacitive MEMS sensors have serious challenges in their ability to be significantly scaled down. Any multi-axis sensor cannot be smaller than its several sensitive components. All sensitive components of capacitive sensors are capacitors and they all are located at the surface of the sensor due to “surface micromachining”. These capacitors and the relative change of the capacitance are practically reached the physical limit. Capacitance value could be in the range of several fF and the measured change of capacitance corresponds to a measured charge smaller than the charge of one electron (by statistical measurements) [2]. Small capacitance and its change, on one end, and charge of electron, on the other end, make it very challenging to provide a wide dynamic range of the sensors in concert with scaling them down. If the goal is decreasing of the area occupied by the sensor microstructure at the surface of the die, then the only way to increase the capacitance and its relative change is to increase the thickness of the surface micro-machined layer keeping the length and the width of the fingers in the comb structures and the width of the gaps between the fingers the same. However due to the limits on the aspect ratio during DRIE it is very challenging to achieve this

goal [3]. Increasing the depth of DRIE etching would also require increasing the gaps between the fingers, which would not result in increasing the capacitance and its relative change, as capacitance would increase proportionally to the depth and inversely proportionally to the gap width. In reality it would result in increasing the area of microstructure at the surface of the silicon die. Therefore, it seems that MEMS surface micro-machined capacitors cannot be significantly scaled down in size, as well as capacitive MEMS sensors.

The second serious challenge of scaling capacitive sensors is that it is not easy to make a big proof mass due to the nature of surface micromachining. The device layer is thin and the mass of the device micro-structure is determined by the area occupied by the microstructure at the surface of the die, which one wants to scale down.

Of course, some new technological opportunities like SiGe films, which can be deposited at low temperature on the top of already fabricated CMOS circuit and which can be used as a structural material of the capacitive micro-structures, could make for some time less critical the issue of scaling down the size of capacitive sensors, while the other issues including complexity of the structure, small mass and the economy of this integration will still remain [4].

Figure 3 illustrates the relative size and mass of the proof mass of the current capacitive sensors compared to Siantis’ sensors.

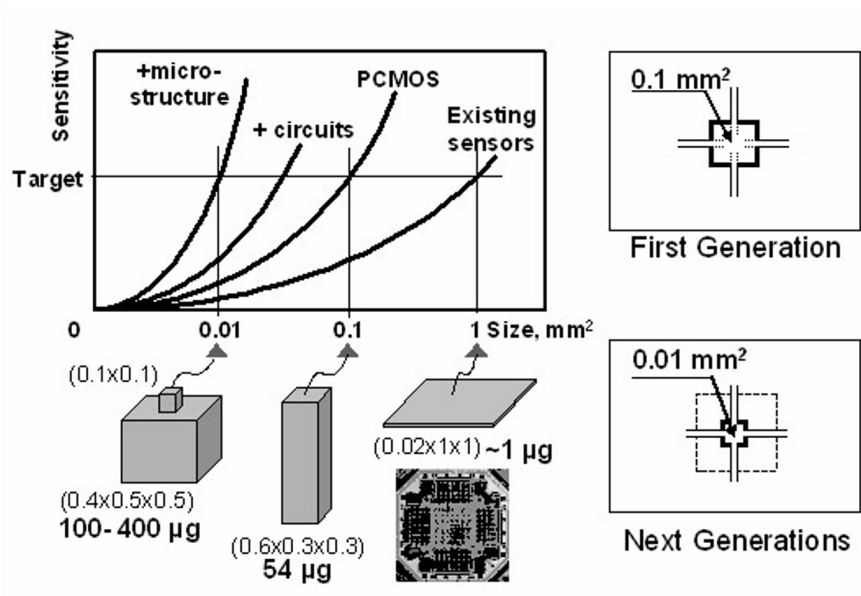
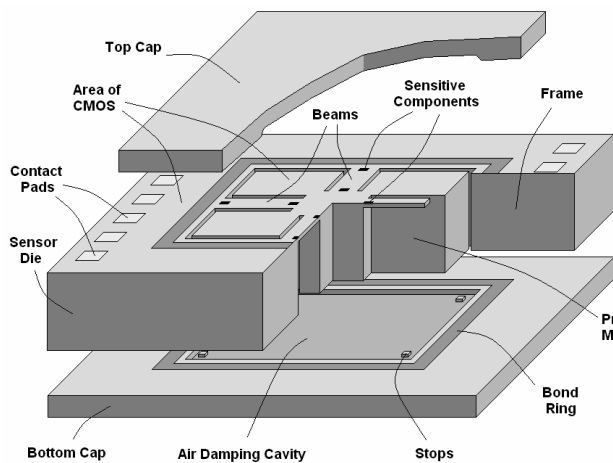
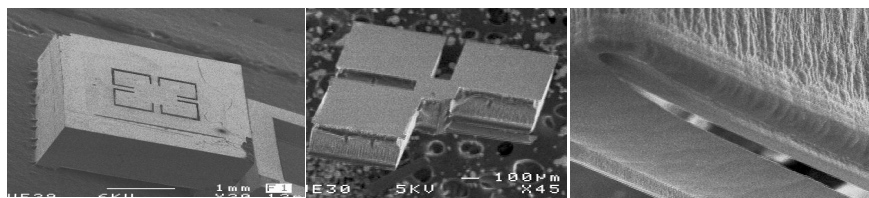


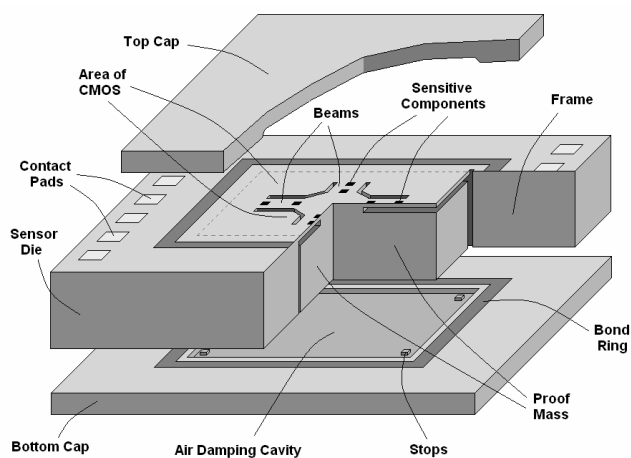
Figure 3. Size and proof mass of the current capacitive sensors compared to Siantis’ sensors.



(a)



(b)



(c)

Figure 4. (a) First generation of Siantis 3-axis accelerometer; (b) micro-photograph of the mechanical microstructure elements; (c) second generation of 3-axis accelerometer.

If capacitive sensor occupies  $1 \text{ mm}^2$  area and the device layer is  $2 \text{ }\mu\text{m}$  thick, then the proof mass would be about  $1 \text{ }\mu\text{g}$ . First generation Siantis' sensors occupy  $0.1 \text{ mm}^2$  and the proof mass is  $54 \text{ }\mu\text{g}$ . The second generation Siantis' sensors occupy  $0.01 \text{ mm}^2$  and have the proof mass of  $100\text{--}400 \text{ }\mu\text{g}$ . The result is that Siantis' sensors are more than 100 times smaller at the surface of the die shared with CMOS and at the same time have proof mass more than 100 times bigger.

Figure 4a illustrates the first generation of Siantis 3-axis accelerometer [5]. The microphotographs of the die, mechanical microstructure of the proof mass and one of the beams are shown from the back side in Figure 4b. Figure 4c illustrates the second generation of 3-axis accelerometer, where microstructure of the sensor occupies a small area at the surface of the die shared with CMOS and the big proof mass providing large sensitivity is located within the thickness of the wafer [6].

#### 4. Simple microstructures for multi-axis measurements

General principle, which Siantis uses for multi-axis measurements, is that the large proof mass is formed within thickness of the silicon wafer rather than by depositing structural layers on the surface of the wafer. The proof mass is connected by multiple suspensions to the frame of the die and multiple sensitive elements are incorporated within those suspensions, as schematically shown in Figure 5.

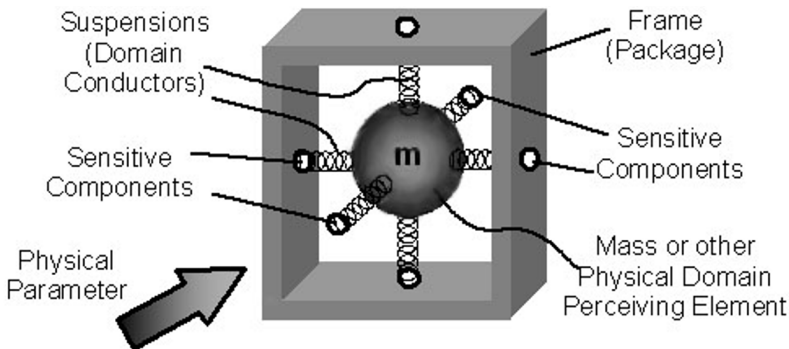


Figure 5. Generalized principle of multi-axis measurements.

The proof mass might move in different directions relative to the frame depending on the vector of the mechanical parameter to be measured. As the mass is not directly connected to the sensitive components, it might have no restrictions on arbitrary motion in any direction. The combination and the value of the output signals from different sensitive components, as a result of mechanical stress in the location of these components within suspensions, allow determining the value of the measurand vector. In case of capacitive sensors the sensitive elements



(capacitors) at least partially are connected to the proof mass and move with the mass relative to the frame, which is mechanically connected to the other plates of the sensitive capacitors. Clearly it limits the freedom of proof mass movements and therefore the flexibility of designs, makes the mechanical microstructure very complex compared to Siantis' approach and it makes a development of such sensors, as 6-axis sensors, very challenging, if not practically impossible. Siantis' approach can be applied to different types of multi-axis sensors. If the proof mass is a structure exhibiting linear motion then the sensor can be a linear accelerometer, or inclinometer, or vibrometer. If the proof mass is a structure exhibiting angular motion then the sensor can be an angular accelerometer. If the proof mass is subjected to forced oscillations then the sensor can be an angular rate sensor (gyro). If the proof mass is an oscillating structure capable of an additional linear motion under acceleration then the sensor can be a 6-axis motion sensor. If instead of the proof mass an external force is used to load the microstructure then the sensor can be a three-axis force sensor. This patented technology for force sensors is being commercialized now for high volume application [7, 8]. Similar principle can be also applied to a magnetic field sensor. This unified approach builds the foundation for monolithic integration of different multi-axis sensors within one fabrication process.

## 5. Unified component platform

It is well known that transistors both bipolar and CMOS can be used as mechanical stress sensitive components. It was also demonstrated that piezo-transistors can be fabricated within MEMS sensors, as was described above. Therefore, there are no limits for transistors to being used as both sensitive components and as signal processing components creating a unified component platform. This creates not only the convenience of components and processes standardization but also a basis for unified scaling of total micro-system, as the size of CMOS transistor scales down.

As piezo-transistor area can be more than 1,000 times smaller than typical piezoresistor area, it immediately opens an opportunity to scale down the size of the sensor mechanical microstructure and springs, beams and other types of suspensions in particular. Figure 6 illustrates how the size of the beam connected to the frame in piezoresistive sensors can be decreased by switching to piezo-transistors, as stress sensitive components.

In typical layout of the piezoresistors, shown in Figure 6a, for a half-bridge circuit one of the p-type resistors should be longitudinal and another is transversal. It determines the minimal width of the beam for a chosen size of resistor. When piezo-transistors are used instead of piezoresistors, it allows decreasing the width of the beam, as multiple transistors would require much smaller area (Figure 6b). If requirements for the allowed deflection of the beam remain the same, then the length of the beam can also be decreased.

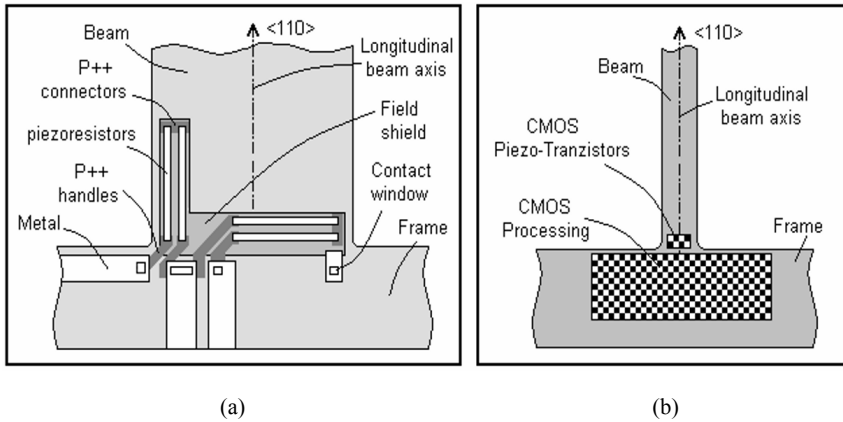


Figure 6. Comparative geometries of the beams for piezoresistors (a) and piezo-transistors (b), as sensitive components.

Multiple sensitive components located in one area of the beam also allow measuring different stresses at this location: tensile, compressive, shear in different directions, which gives an additional advantage in measuring very complex mechanical motion of the proof mass relative to the frame of the sensor. It is important for the multi-axis measurements like 6-axis measurements.

## 6. Sensitive integrated circuits

The general principle of sensitive integrated circuits technology is to combine large number of piezo-sensitive components for the purpose of increasing sensor sensitivity. In this case piezo-transistors are used not as active amplifying components but rather as three-port-pole components, which allows to combine more than four, like within Wheatstone bridge, components and by these means increase the signal-to-noise ratio. Without diving into the depth of this pending patenting technology let us illustrate this principle on the example of one specific sensitive integrated circuit based on bipolar piezo-transistors and piezoresistors shown in Figure 7 [9].

As can be seen from the circuit, only two three-port-pole sensitive components bipolar transistors allowed combining 10 piezo-sensitive components: two transistors and eight piezoresistors.

While four piezoresistors, with about 1% relative resistance change in the working range, give output signal of about 1% of voltage supply, ten piezo-sensitive components of the above circuit gave 8.4% of voltage supply. Fabricated circuit pressure sensor for 40 KPa pressure range and 5 V voltage supply provided sensitivity 10.5 mV/KPa.

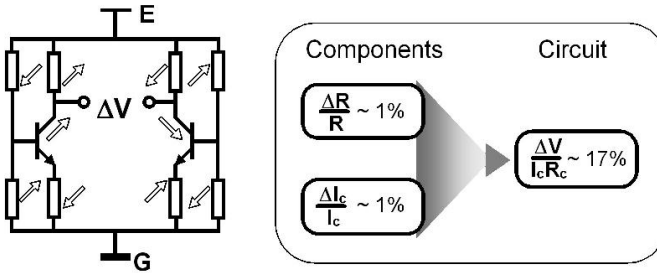


Figure 7. Example of sensitive integrated circuit based on two bipolar piezo-transistors and eight piezoresistors.

Sensitive integrated circuits open the way of achieving dynamic range of these sensors about or greater than  $10^6$  with significant scaling sensor size down. One can imagine the unlimited hidden opportunities of this technology applied to CMOS circuitry.

Differentiation of Siantis' technology can be summarized as follows:

- Integration of CMOS with different sensors
- Smallest sensor area size shared with CMOS
- CMOS piezo-transistors as sensor components
- Circuit sensors
- Single simple microstructure for multi-axis measurements

All the above open an opportunity in decreasing cost per sensor more than 10 times, higher sensitivity more than 100 times and higher reliability, which creates a strong foundation for a long-term roadmap of wide range of multi-sensor microsystems.

## 7. Economic justification of monolithic integration

For the last 17 years the price per sensor axis decreased about 7 times, the same as for sensor size. Similar to IC in general, decrease of the die size is the major source of cost reduction. Today the lowest price for Accelerometers is about \$0.4/axis and \$1.5–2.5/axis for Gyro. Future individual sensor cost is predictable for currently employed technology and provides basis for sensors monolithic integration commercial rationale.

As Sensor price decrease is exponential, it has become asymptotic – paradigm shift is required. Figure 8 illustrates some historical sensor die size decrease data.

For the last 17 years the size of a sensor die has only decreased at the rate of 2X every 6.3 years (compared with CMOS rate of 2X every 1.5 years per Moore's Law). Current average die size is around  $1.3 \text{ mm}^2/\text{axis}$  for accelerometers

and 10 mm<sup>2</sup>/axis for gyro. Best results, to our knowledge, are 0.8 mm<sup>2</sup>/axis for accelerometers (Hitachi) and 5 mm<sup>2</sup>/axis for gyro (Invensense). Future individual sensor die size (cost) is therefore predictable for currently employed technology. There are no reasons to believe that this rate will significantly change for the current technology – novel technology is required to improve this trend.

For the same 17 years the size of a sensor microstructure was decreasing with the rate of 2X in every 17 years for accelerometers and 13 years for gyros. The size of the die was decreasing faster (2X/6.3 years) due to faster decreasing surrounding signal processing electronic circuits (ADI). Today micro-structure size is about 0.3–0.5 mm<sup>2</sup>/axis for accelerometers and about 3.5–5 mm<sup>2</sup>/axis for gyros. Future microstructure size (cost) is therefore predictable for currently employed technology. Siantis’ novel technology changes this paradigm.

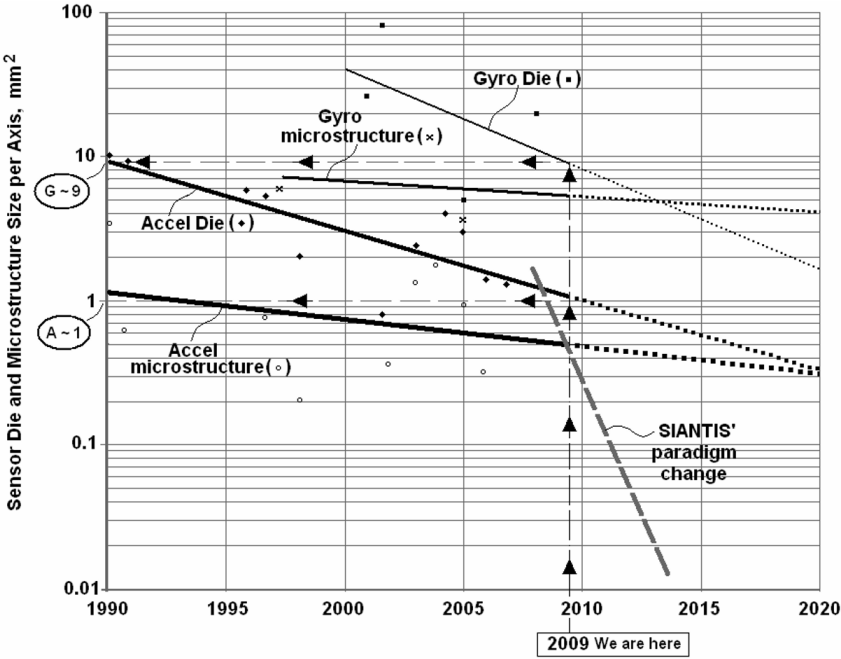


Figure 8. Historical sensor die and sensor microstructure size decrease.

Estimating the IMU sensors cost for integration one can conclude that for a number of years ahead: expected price for 3-axis accelerometer will be in the range of \$1–1.5; for 3-axis gyro – \$3–4; for altimeter – \$0.3–0.5; total cost (price) for a set of stand alone sensors will be therefore about \$4–6.

These prices (\$1–1.5), (\$3–4) and (\$4–6) serve as benchmarks that determine the upper limits of the corresponding monolithic integration costs.

The logistics of monolithic integration of sensors with CMOS might be describes as:

1. Monolithic Integration of CMOS with Sensors involves the following major additional expenses: cost of SOI initial material (~\$800/wafer), cost of cap wafers (~\$100/wafer), cost of MEMS processing (~\$500/wafer). Total cost of monolithic integration ~\$1,500/wafer.
2. Acceptance of this additional expense per wafer depends on the number of die per wafer. In turn, this depends on the die size, where these sensors are to be integrated.
3. Both sensor and CMOS costs reduce in concert with the die size reductions – effect on cost reduction is multiplied, as both are integrated on the same die.

Large proof mass allows for stronger suspensions, which provides better reproducibility of sensor micro-structure geometry formed on SOI wafers. As a result, the yield loss related to fabrication of mechanical microstructures of sensors can be up to order of magnitude smaller than yield loss related to CMOS process.

On the chart in Figure 9 the maximum allowable cost of monolithic integration per die, as a function of the die size is presented.

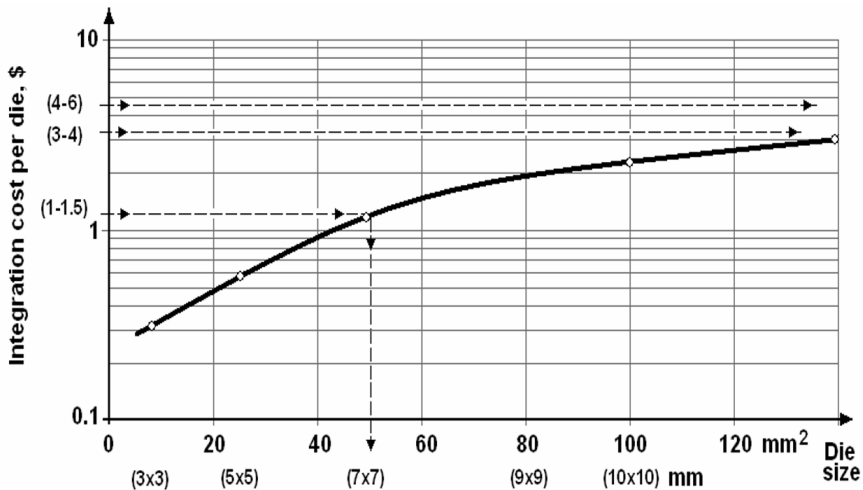


Figure 9. Maximum allowable cost of monolithic integration per die.

As can be seen from the chart, Siantis technology provides reduced cost even with large die sizes. Cost reduction improves dramatically with die size reduction and this is already part of CMOS roadmap.

The size of the CMOS die, where monolithic integration can be justified today, should be smaller than about  $7 \times 7$  mm for integration only with 3-axis accelerometer, smaller than  $12 \times 12$  mm for integration only with 3-axis gyro and smaller than  $15 \times 15$  mm for integration with 6-axis sensors. While the cost of

monolithic integration (SOI wafers, MEMS processing, etc.) will be decreasing, the size of the CMOS dice, with which integration is needed, will also be decreasing along with the decreasing of the node size of CMOS. It will result in compounded savings on monolithically integrated products.

One can make corrections to the above estimates of justified die size for monolithic integration by safeguarding the forecast of the corresponding stand alone sensors prices and cost of integration.

## 8. Conclusion

Monolithic integration of CMOS with multiple sensors is inevitable. It provides clear path to lower cost and improved technical performance. However, current sensor technologies cannot support the required price point or process compatibility for monolithic CMOS integration. Siantis' novel technology changes this paradigm by making monolithic integration of multiple different sensors with CMOS possible. Manufacturing costs are already lower than alternative schemes and there is a logical path to significantly reducing these costs further. These future cost reductions are realized in parallel with and due to decreasing size of CMOS transistors and provide a multiplication effect on the overall cost reduction achieved – far beyond what can be met by alternative approaches.

## Acknowledgments

I would like to express my gratitude to Dr. Nickolai Belov, my colleague, partner and friend for many years who contributed to the development of Siantis' technology and to some materials published in this paper.

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Advanced Materials and Technologies for  
Micro/Nano-Devices, Sensors and Actuators

Gusev, E.; Garfunkel, E.; Dideikin, A. (Eds.)

2010, XI, 314 p., Hardcover

ISBN: 978-90-481-3805-0