

Chapter 2

PSP-SOI: A Surface-Potential-Based Compact Model of SOI MOSFETs

Weimin Wu, Wei Yao, and Gennady Gildenblat

Abstract Surface-potential-based models, which represent the mainstream approach to compact modeling of bulk MOSFETs, are now in the process of being applied to SOI devices. In this chapter we discuss two advanced SOI models—PSP-SOI-PD for partially depleted devices and PSP-SOI-DD including the dynamic depletion effects. Both models are based on the popular PSP model of bulk MOSFETs. The theoretical foundation of all PSP-family models is the symmetric linearization method that allows one to raise the physical contents of the compact model without prohibitive increase in its computational complexity. In addition to the physics-based structure of the new models inherited from bulk PSP, they account for phenomena specific to SOI devices (e.g. floating body, and valence band tunneling current) and include a detailed description of parasitic effects. We discuss both the theoretical developments and verification of the model against test data and TCAD simulations with particular emphasis on the interplay between the model structure and its simulation capabilities.

2.1 Introduction

Compact models of SOI devices provide a bridge between the manufacturing process and circuit design. They are required to accurately reproduce the device characteristics responsible for placing SOI technology in the mainstream for low-power high performance ULSI applications [12, 46]. These include reduced junction capacitance, elimination of body effect in stacked devices (e.g. NMOS transistors in NAND gates), dynamic threshold voltage shift brought about by the floating body effect (FBE) and the corresponding increase of the ON/OFF ratio which is beneficial for the low power CMOS SOI applications. At the same time particular attention

W. Wu (✉) · W. Yao · G. Gildenblat
School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe,
AZ 85287, USA
e-mail: Weimin.Wu@asu.edu

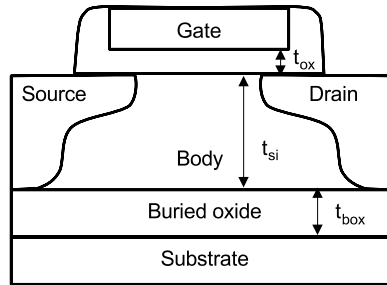
should be paid to the reproduction of numerous parasitic elements (e.g. body contact resistance) and secondary effects (e.g. self-heating) which are not present or less important in bulk CMOS technology. More recently growing RF applications of SOI technology placed even more stringent requirements on the qualitative behavior of compact SOI models: it is now common to request that advanced SOI compact models have the capability to model intermodulation effects. This requires preserving the model symmetry with respect to the source-drain interchange in order to obtain non-singular $I(V)$ and $C(V)$ characteristics at zero drain bias. In other words, it is now expected that SOI compact models provide all the advanced features of the latest bulk MOSFET models. With this in mind it is natural to take one of these models (PSP) as a starting point in developing compact models of SOI. From a more general point of view, we are witnessing the paradigm change in the development of SOI compact models. With a few years delay relative to the bulk CMOS technology, threshold-voltage based models of SOI MOSFETs are gradually being replaced by the more advanced surface-potential-based models.

The surface-potential-based approach to compact models is not new—for bulk devices it goes all the way back to the classic work of Pao and Sah [41] and its efficient approximation in the charge-sheet model (CSM) [3]. The feasibility of this approach for modeling SOI MOSFETs has been demonstrated in [43, 49, 69]. In particular, complete surface-potential model of partially-depleted SOI devices including all secondary effects and charge model has been developed and verified in [69] starting with the SP model [20] which together with MM11 [60] is one of the predecessors of the industry standard PSP. The new element of the present situation is that for bulk devices the transition to the surface-potential-based models is completed and hence it is time to move from experimental models and feasibility studies to the industrial strength surface potential based models of SOI transistors.

Two such models based on the PSP model [19] and the experiences gained in the process of development of the SP-SOI [69] are discussed in the present chapter. We start with the partially depleted SOI MOSFET model PSP-SOI-PD. Since the model inherits drain current and terminal charges formulation from the bulk PSP model, we concentrate on the effects specific for the SOI devices. In Sect. 2.2 we discuss the modeling of the FBE including impact ionization Junction diode and parasitic bipolar transistor. We also describe the compact model of the electron tunneling from the valence band (EVB) which is usually negligible in bulk MOSFETs but is often required to catch the fine details of the SOI MOSFET transfer characteristics. Both experimental data and circuit implications of the EVB current are considered in some detail. Following the discussion of the self-heating effect in Sect. 2.3, non-linear body resistance model in Sect. 2.4 and noise sources are in Sect. 2.5 we proceed with the parameter extraction procedure and model verification against the experimental data in Sect. 2.6.

The second part of the chapter describes a more general “dynamic depletion” model, PSP-SOI-DD, which can model the transition between the partial depletion and the full depletion regimes of SOI MOSFETs. Superficially, it may appear that the development of the dynamic depletion model obviates the need for a separate model of the partially depleted SOI devices. However, the surface potential formu-

Fig. 2.1 Cross-sectional view of a PD-SOI MOSFET; t_{ox} is the gate oxide thickness, t_{si} is the channel region silicon thickness, and t_{box} is the buried oxide thickness



lation of the DD model is inevitably more complex and requires the solution of coupled surface potential equations at the two (or even three) interfaces. This is justified if there is a real possibility of the DD behavior in the simulated circuits. However, for the PD technology, using separate SOI model of partially depleted devices is more computationally efficient and should be preferred.

Theoretical background of the PSP-SOI-DD model is developed in Sect. 2.7 by developing well-conditioned system of surface potential equations and obtaining a particular version of the symmetric linearization method which underlies all PSP family models and has been recently extended to multiple-gate devices [13, 14]. We also provide a detailed discussion of how the electrostatics of the SOI-DD transistors can be simplified without noticeable effects for the output characteristics. Since PSP-SOI-DD inherits from both PSP and PSP-SOI-PD the discussion of the SOI-specific effects in Sect. 2.2 remains directly applicable to PSP-SOI-DD and is not repeated. Section 2.8 presents model verification by TCAD computations followed by conclusions in Sect. 2.9.

2.2 PD-SOI Floating Body Effect Modeling

PD-SOI with floating body is often the most desirable configuration in SOI technology. In this case, the active channel of a PD-SOI MOSFET is electrically isolated from its underneath substrate by the insulating buried oxide (Fig. 2.1). Unlike the conventional bulk MOSFET, the individual SOI MOSFETs have different body potentials which are determined by various physical mechanisms and needs to be modeled accurately for circuit simulations. The threshold voltage is a function of the body potential and affects the device characteristics. Thus, an accurate characterization and modeling of these mechanisms is essential in determining the body potential and capturing the floating body effect in PD-SOI MOSFETs.

The floating body effect in a PD-SOI MOSFET is manifested by the “kinks” in output characteristics at high drain biases. These are usually caused by the forward bias of the junction produced by the impact ionization current in the body. With scaled ultra-thin gate oxide, the direct gate tunneling current also injects charge carriers into the body and causes “kinks” which can be observed in the transfer characteristics [11, 29, 74].

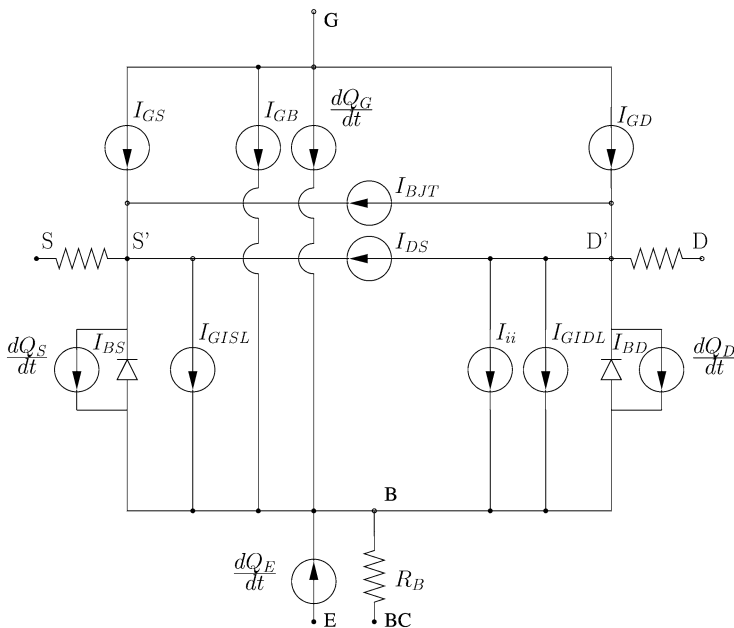
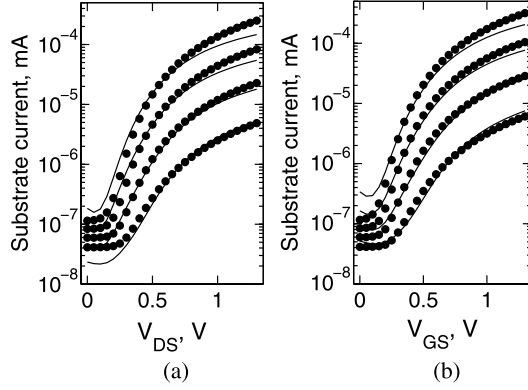


Fig. 2.2 Circuit representation of PSP-SOI. I_{DS} —intrinsic drain current, I_{BJT} —parasitic bipolar current, I_{ii} —impact ionization current, I_{GIDL}/I_{GISL} —gate induced drain (source) leakage. I_{BS}/I_{BD} is source/drain junction current. $I_{GS}/I_{GD}/I_{GB}$ is gate to source/drain/body tunneling current. Q_S , Q_D , Q_G , Q_E are source, drain, gate and back-gate charges. For body-contacted SOI, an extra node (BC) is provided to control the internal body node (B) voltage through a body resistance R_B

All known physical mechanisms that affect the body potential are included in PSP-SOI and are shown in the circuit representation in Fig. 2.2. For the floating body configuration, there are four external nodes: source (S), drain (D), gate (G) and substrate/back-gate (E). In the DC regime, the body bias relative to the source, V_{BS} , is established by the equilibrium between the injection of majority carriers (holes in nMOS) into the body and the removal of majority carriers out of the body. The injection primarily includes: (i) impact ionization near the channel-drain side caused by the high lateral electric field, (ii) reversed biased drain-body junction leakage, (iii) direct tunneling between the gate and the body, (iv) gate-induced drain/source leakage (GIDL/GISL). The majority carriers are removed mainly by (i) forward-biased body-source junction when the body potential is high enough, and (ii) thermal recombination in the junctions. In the transient or AC regime, capacitive coupling between the body and external nodes (source, drain, gate and substrate) also influences the body potential.

For the body-contacted configuration, an external body contact node (BC) connects to the internal body node (B) through a resistive path (body resistance R_B). In this configuration, the balance of currents from the external body contact node, capacitive coupling (displacement currents), and above-mentioned DC paths determines the body potential.

Fig. 2.3 PSP-SOI simulated (lines) and measured (symbols) substrate current of a body-contacted PD-SOI at 25°C. (a) $V_{GS} = 1.0, 1.1, 1.2, 1.3$ V; (b) $V_{DS} = 0.8, 0.9, 1.0, 1.3$ V. $W/L = 3 \mu\text{m}/0.065 \mu\text{m}$. After [72]



2.2.1 Impact Ionization

PSP-SOI uses the same impact ionization model as PSP [20, 23]. It includes accurate descriptions of the subthreshold region and the effect of body bias V_{BS} :

$$I_{ii} = a_1 (V_{DS} - a_3 \Delta\psi) \exp\left(-\frac{a_2^*}{V_{DS} - a_3 \Delta\psi}\right) I_{DS}, \quad (2.1)$$

$$a_2^* = a_2 (T_{KD}/T_{KR})^{\kappa_{a2}} \left[1 + a_4 \left(\sqrt{2\phi_B - V_{BS}} - \sqrt{2\phi_B}\right)\right]. \quad (2.2)$$

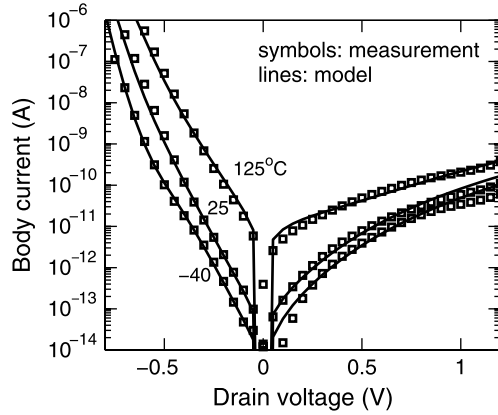
Here a_1 , a_2 , a_3 and a_4 are model parameters, $\Delta\psi = \psi_{sd} - \psi_{ss}$, ψ_{ss} and ψ_{sd} are the surface potentials at the source and drain ends of the channel, respectively, $\phi_B = \phi_t \ln(N_A/n_i)$ is the Fermi potential, N_A is the substrate doping density and n_i is the intrinsic carrier density of silicon. In SOI MOSFETs, the impact ionization current can be enhanced due to self-heating which increases the channel current [54]. This temperature dependence of I_{ii} is accounted for by introducing the temperature dependence parameter κ_{a2} of impact ionization exponent a_2^* . T_{KD} , T_{KR} are the device and reference temperatures, respectively. Self-heating and its effect on device characteristics are further discussed in Sect. 2.3.

Figure 2.3 shows the model fits the substrate current of a short-channel SOI device very well, including the low drain and low gate bias regions. This is important to capture the experimentally observed gradual turn-on of the “kink” effect that may occur at a drain bias below the impact ionization threshold owing to various energy gain mechanisms [1, 17].

2.2.2 Junction Diode

The characteristics of junction diodes formed by the body and the source or drain are essential to the electrical behaviors of SOI MOSFETs. In PD-SOI technologies,

Fig. 2.4 Model fit of junction leakage current. The source and drain terminals of the body-contacted n-channel SOI device are tied together. $V_{GS} = 0$ V. $W/L = 3 \mu\text{m}/0.065 \mu\text{m}$. After [72]



the junction leakage characteristics are highly non-ideal, due to the high doping concentration in the HALO region. Thus, the band-to-band tunneling (BTB) and trap-assisted tunneling (TAT) components must be included to model the junction current of PD-SOI MOSFETs in addition to the ideal drift and diffusion current, Shockley-Read-Hall recombination and generation current:

$$I_{B,S/D} = I_{ideal} + I_{SRH} + I_{TAT} + I_{BBT}. \quad (2.3)$$

To achieve the accurate modeling of the junction current, PSP-SOI includes JUNCAP2 [45] diode model. The junction current is very sensitive to the temperature variations. Accordingly, the body potentials and device performance (drain current) will be affected as well. JUNCAP2 includes temperature dependence of all physical diode leakage components, making it ideal for modeling the PD-SOI MOSFETs. The resulting temperature dependence of the body current is shown to be in a good agreement with experimental data. Typical results are illustrated in Fig. 2.4 for three different temperatures.

2.2.3 Parasitic Bipolar Current

The major issue in the PD-SOI technology is the parasitic bipolar effect primarily resulting from the floating body under the gate, which acts as the base of the parasitic bipolar transistor (shown in Fig. 2.1). The source and drain act as the emitter and collector, respectively. The base current is supplied by the impact ionization current and can be amplified by the forward biased emitter-base junction (i.e. source-body).

In circuit operation, the parasitic bipolar effect primarily manifests itself during transient switching if there is a large voltage across the body-to-source junction of the parasitic bipolar transistor. This current can cause extra power consumption, degrade noise margins in static CMOS configurations, or lead to logical state errors in some dynamic circuits [33]. Hence, it needs to be included in PD-SOI compact models.

In PSP-SOI, parasitic bipolar current is modeled by adding a parasitic BJT current element described by a simplified version of the Gummel-Poon model [18, 25]:

$$I_{BJT} = \alpha_{BJT}(I_S/q_B) [\exp(\beta V_{BS}) - \exp(\beta V_{BD})], \quad (2.4)$$

where the bipolar transport factor $\alpha_{BJT} = \text{sech}(L/L_n)$, L_n is the minority carrier diffusion length and I_S is the saturation current. The normalized base charge q_B given by

$$q_B = \frac{q_1}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2}, \quad (2.5)$$

where

$$q_1 = 1 + (V_{BS} + V_{BD})/V_A, \quad (2.6)$$

and

$$q_2 = (4I_S/I_K) [\exp(\beta V_{BS}) + \exp(\beta V_{BD}) - 2]. \quad (2.7)$$

Here V_A is the Early voltage of the parasitic bipolar transistor and I_K is the knee current. The recombination current in the quasi-neutral body are also included. The source junction contribution is

$$I_{JS,rec} = (1 - \alpha_{BJT})(I_S/f) [\exp(\beta V_{BS}) - 1], \quad (2.8)$$

where f accounts for the high-level injection effect

$$f = \frac{1}{2} + \sqrt{\frac{1}{2} + \frac{I_S}{I_K} \exp(\beta V_{BS})}. \quad (2.9)$$

A similar expression is used for the drain junction contribution $I_{JD,rec}$. Thus, the total junction leakage current consists of the recombination-generation current in the junction depletion regions, hole and electron diffusion currents and the recombination current in the neutral body region. For completeness, the diffusion capacitances are included as well by introducing transit time coefficient τ_t

$$Q_{JS,diff} = \tau_t \cdot I_{JS,rec}. \quad (2.10)$$

Figure 2.5 shows Gummel plot measured on a body-contacted SOI nMOSFET, which can be used to extract parasitic bipolar current model parameters. A maximum bipolar gain of 10 is observed for this device. At large forward V_{BS} , the bipolar gain becomes smaller due to high-level injection and series resistance.

Figure 2.6 shows a simulation of pass-gate logic with the PSP-SOI model. Initially, the control signal “C” and the input signal “IN” are “High” (V_{DD}). With both the nMOS and pMOS turned on, the drain node and internal body potentials settle to V_{DD} . If the source node (IN) is pulled down after switching the control signal “C” to “Low”, a large body-to-source voltage is created. This turns on the parasitic npn BJT and causes a transient bipolar current I_{BJT} to flow. Once the body is discharged, this current disappears.

Fig. 2.5 Gummel plot of parasitic BJT in a body-contacted SOI (nMOS). The gate and source are grounded and $V_{DB} = 0$ while sweeping V_{BS} . $W/L = 3 \mu\text{m}/0.055 \mu\text{m}$. After [72]

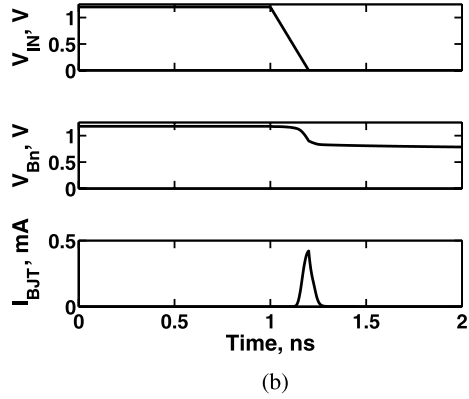
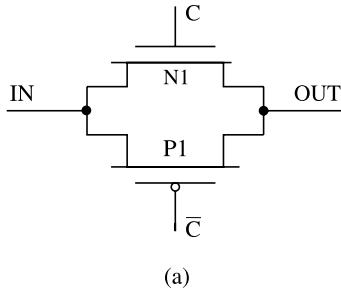
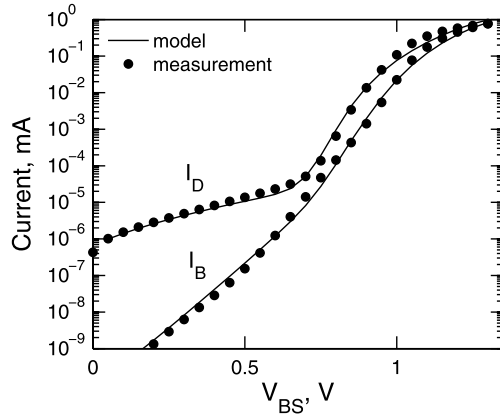


Fig. 2.6 (a) Circuit diagram of a basic pass-gate logic. (b) Waveforms of input signal V_{IN} , body potential V_{Bn} and parasitic bipolar current I_{BJT} in nMOS. The model parameters are extracted from typical 65 nm PD-SOI technology; $W/L = 30 \mu\text{m}/0.065 \mu\text{m}$. After [72]

2.2.4 Gate-to-Body Tunneling Current

As the gate oxide thickness t_{ox} scales to 1.0 nm, the oxide tunneling current increases dramatically. Gate-to-body tunneling includes several components: ECB (electron tunneling from conduction band), HVB (hole tunneling from valence band) and EVB (electron tunneling from valence band) [4]. In bulk MOSFETs EVB tunneling generates the substrate current, which is much less than the gate-to-channel tunneling current (ECB or HVB) and therefore can be neglected. However, in SOI MOSFETs the EVB tunneling current charges and discharges the body, and consequently affects the threshold voltage V_T by altering the body potential. The impact of gate-to-body tunneling current on PD-SOI CMOS circuits has been investigated in [11, 29].

In PSP-SOI, the EVB model is developed from a surface potential based approach. In the Tsu-Esaki formulation [59], the tunneling current density has the form

$$J_{EVB} = \frac{4\pi q m^*}{h^3} \int_0^{qV_{ox} - E_g} D(E_x) (qV_{ox} - E_g - E_x) dE_x, \quad (2.11)$$

where q is the magnitude of electron charge, m^* is the effective electron mass in the valence band of Silicon, h is the Planck's constant, E_g is the energy gap, and V_{ox} is the voltage across the oxide which is position dependent. $D(E_x)$ is the tunneling transmission coefficient which for simplicity is evaluated in a WKB approximation:

$$D(E_x) = \exp \left\{ -2 \int_0^{t_{ox}} \sqrt{\frac{2m_{ox}^*}{\hbar^2} [E_C(x) + E_x]} dx \right\}, \quad (2.12)$$

where integration is over the component of the electron's energy E_x in the direction normal to the potential barrier, $E_C(x)$ is the conduction band energy in the oxide and m_{ox}^* is the effective mass of electrons in SiO_2 . To obtain an explicit and simple expression, we assume that the EVB tunneling current is mainly from electrons having energy $E_x = 0$ in the valence band (mono-energetic approximation already used for ECB in [24]). The total EVB tunneling current is obtained by integrating the current density along the channel

$$I_{EVB} = W \int_0^L J_{EVB} dy. \quad (2.13)$$

As Fig. 2.7 shows, the drain current I_{DS} is increased due to higher body potential induced by the EVB tunneling. The model accurately reproduces the “linear kink effect” induced by the EVB tunneling current [15, 37], as observed in the transconductance g_m , particularly at low V_{DS} .

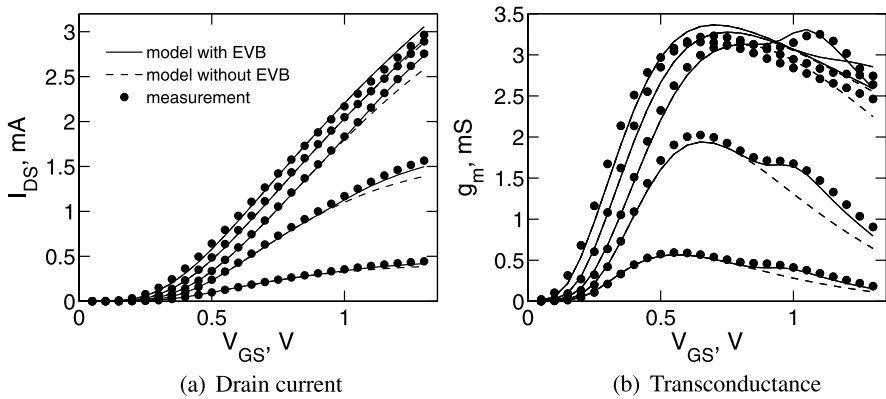


Fig. 2.7 Impact of gate-to-body tunneling current (EVB) on the DC transfer characteristics of floating body SOI MOSFETs. $V_{DS} = 0.05, 0.2, 0.6, 1.0, 1.3$ V, $W/L = 3 \mu\text{m}/0.13 \mu\text{m}$. After [72]

Fig. 2.8 (a) Circuit diagram of a transmission-gate multiplexer. (b) Input signal waveforms used in simulations. Signal “A” has a period of 2 ns and slew time of 20 ps. After [72]

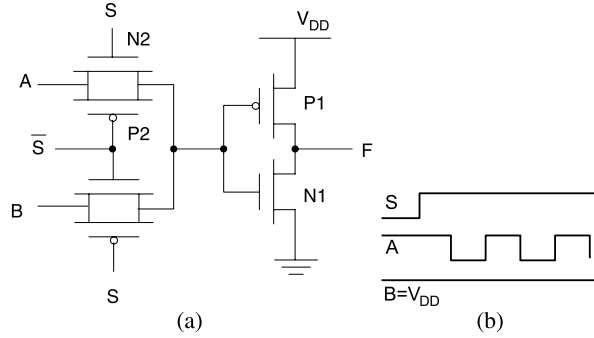


Fig. 2.9 Body potential of nMOS (N1) before the input falling transition. After [72]

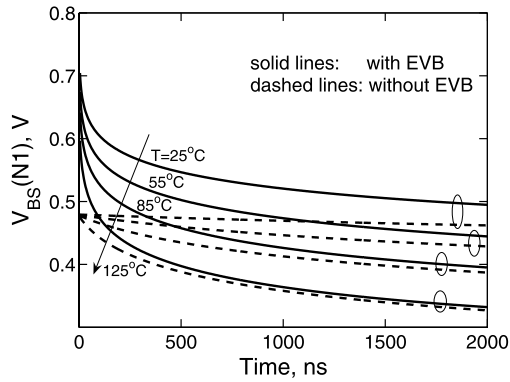


Figure 2.8 shows a transmission-gate multiplexer implementing the Boolean function $F = A \cdot S + B \cdot \bar{S}$. If initially the inputs “A”, “B” are “High” ($V_{A,B} = V_{DD}$) and control signal “S” is “Low”, the input of the inverter is settled at “High”. Under this scenario the pre-switch body potential of nMOS (N1) is determined by the EVB tunneling current and two forward biased junction currents. The body potential of pMOS (P1) is determined by the balance of back-to-back junction leakage currents. The EVB tunneling current has little impact on the body potential of P1. Consequently, the initial input-fall delay t_{pLH} is larger and the input-rise delay t_{pHL} is smaller because N1 is “stronger” (a lower V_T) in the presence of EVB tunneling current. In the transient steady state, the body potentials are determined by both the capacitive coupling and DC currents (junction leakage, impact ionization current and EVB tunneling), as illustrated in Figs. 2.9 and 2.10. Also, the nMOS (N2) of the top transmission-gate becomes “slightly stronger” during input rise transitions due to the EVB tunneling current. This makes the input rise delay even faster.

As temperature increases, the junction leakage current become larger and the amount of body potential increase caused by the EVB tunneling, which is less temperature sensitive, becomes smaller. The impact of EVB tunneling current on circuit delay times becomes less significant. This is also illustrated in Figs. 2.9 and 2.10.

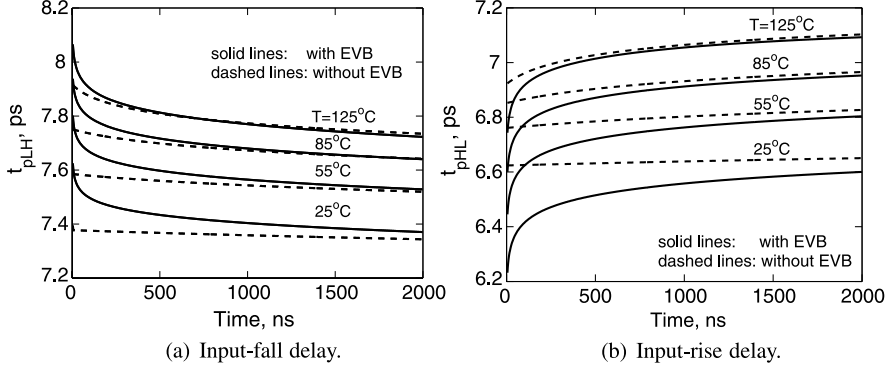


Fig. 2.10 Impact of EVB tunneling current on the delay times of a transmission-gate multiplexer with initial “High” condition. Simulations are done at several ambient temperatures. The model parameter sets used in simulations are representing typical 65 nm PD-SOI technology. After [72]

2.2.5 Gate-Induced Drain Leakage Current

In both bulk and SOI MOSFETs, high electrical field may be induced in the gate-to-drain (source) overlap regions when the MOSFET is in off-state (gate bias $V_{GS} \leq 0$). This causes significant leakage current flow between the drain (source) and the body [7]. In addition, for floating body PD-SOI MOSFETs, this current can raise the body potential if the device is biased into accumulation region and may affect the hysteresis behavior [8, 10]. In PSP-SOI, this leakage current is modeled by the same expressions as in bulk MOSFETs [19, 42]

$$I_{GIDL} = A_{GIDL} V_{DB} V_{tov} V_{ov} \exp(-B_{GIDL}/V_{tov}), \quad (2.14)$$

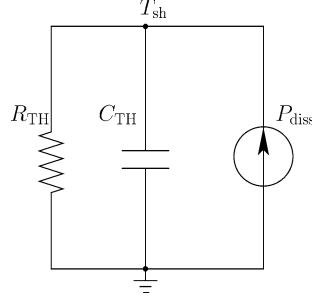
$$V_{tov} = \sqrt{V_{ov}^2 + (C_{GIDL} \cdot V_{DB})^2}, \quad (2.15)$$

where $A_{GIDL} \propto W \cdot L_{OV}$, W is the channel width and L_{OV} is the overlap length of the gate-to-drain (source) overlap region. V_{ov} is the voltage across the overlap region. V_{tov} is proportional to the maximum electrical field at the Si/SiO₂ interface in the overlap region. B_{GIDL} and C_{GIDL} are model parameters.

2.3 Self-Heating Effect

It is well known that SOI MOSFETs suffer from the self-heating effect (SHE) because the buried oxide is an efficient thermal insulator. The Joule heat generated in the channel region can not be transferred outside of the local device quickly, consequently raising the chip temperature. The elevated chip temperature lowers the device performance (by lowering the drain current and transconductances). The self-heating effect in SOI devices and circuits has been extensively studied [51, 56].

Fig. 2.11 Auxiliary self-heating network. $P_{diss} = I_{DS} \times V_{DS}$. The thermal node T_{sh} is accessible by the user to monitor the device temperature rise in SPICE simulations



In PSP-SOI, the self-heating effect is modeled by a standard auxiliary R_{th} - C_{th} sub-circuit [53, 62] (cf. Fig. 2.11). The nodal voltage on T_{sh} is interpreted as the increased local device temperature while R_{th} and C_{th} are thermal resistance and capacitance, respectively. Multifinger SOI devices are also considered in the model of self-heating effect. For example, R_{th} is given by [63]

$$R_{th} = \frac{R_{THW}}{NF \cdot (W + W_{TH0})}, \quad (2.16)$$

where R_{THW} is the normalized thermal resistance, W_{TH0} is the width offset, and NF is the number of fingers. This is important for low power RF applications where multifinger devices are commonly used.

To accurately model the impact of local device temperature rise on the device characteristics, the temperature dependence of key model parameters are also included. In PSP and PSP-SOI, the temperature dependence of flat-band voltage V_{FB} is accounted for by

$$V_{FB} = V_{FB0} + \kappa_{V_{FB}} (T_{KD} - T_{KR}). \quad (2.17)$$

Here V_{FB0} is the flat-band voltage at the reference temperature, and $\kappa_{V_{FB}}$ is the temperature coefficient of V_{FB} . The temperature dependence of mobility, carrier saturation velocity and series resistance are modeled by the following empirical equation

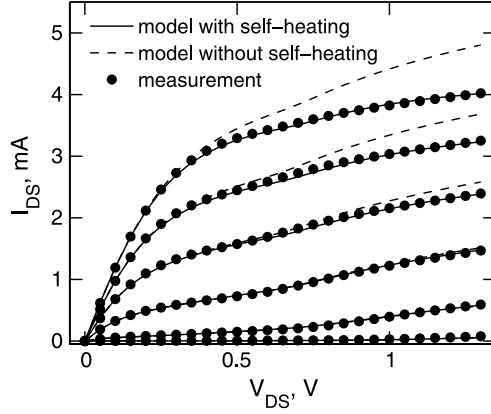
$$P = P_0 (T_{KR}/T_{KD})^{\kappa_P}, \quad (2.18)$$

where P is the corresponding model parameter, P_0 is the value of P at the reference temperature, and κ_P is its temperature coefficient.

Figure 2.12 shows the measured and simulated static output characteristics of a floating body SOI device. Simulations for high gate and drain bias without self-heating predict a larger drain current I_{DS} than when self-heating is enabled. The rise of device temperature is about 60–100 K.

In most high performance logic circuit applications, self-heating is negligible since the power consumption per device under switching condition is low [39]. Furthermore, the thermal time constant (0.1–1 μ s) is much larger than the switching clock rate and self-heating is therefore effectively suppressed. The same simulation

Fig. 2.12 Measured and modeled output characteristics of a floating body SOI nMOSFET. $W/L = 3 \mu\text{m}/0.065 \mu\text{m}$. After [72]



results can be obtained with self-heating disabled in order to improve the computational efficiency of the model.

However, self-heating effect should be taken into account while extracting model parameters. The data are usually taken from DC measurements where self-heating effect is present. The first step in PD-SOI model calibration to hardware data is to determine the thermal resistance and capacitance. They are usually extracted from the AC conductance measurement [28, 39]:

$$G_{DS} = G_{DS0} - \frac{I_{DS0} + G_{DS0}V_{DS}}{V_{DS} - (G_{th} + j\omega C_{th})(\frac{\partial I_{DS}}{\partial T})^{-1}}, \quad (2.19)$$

where G_{DS0} is the intrinsic drain conductance when self-heating is suppressed at high frequency. G_{th} is the thermal conductance. $\frac{\partial I_{DS}}{\partial T}$ can be measured experimentally.

2.4 Body Contact Model

In some critical circuits, especially in high voltage I/O and analog applications, where the instabilities of the threshold voltage are not acceptable, body contacts are used to control the body potential and suppress the floating body effect. A common configuration of the body-contacted (BC) devices is the T-gate structure shown in Fig. 2.13. The body contact is connected to the internal body of the intrinsic device through the region directly under the T-shaped extrinsic gate.

The body contact introduces extra capacitances associated with the extrinsic gate which are modeled by empirical expressions in PSP-SOI. The body resistance, which provides a path for the body currents flowing out the device, depends strongly on the doping profile and channel silicon film thickness. A simple bias-independent model often used to estimate the body resistance is given by

$$R_B = R_{bsh}(W/L), \quad (2.20)$$

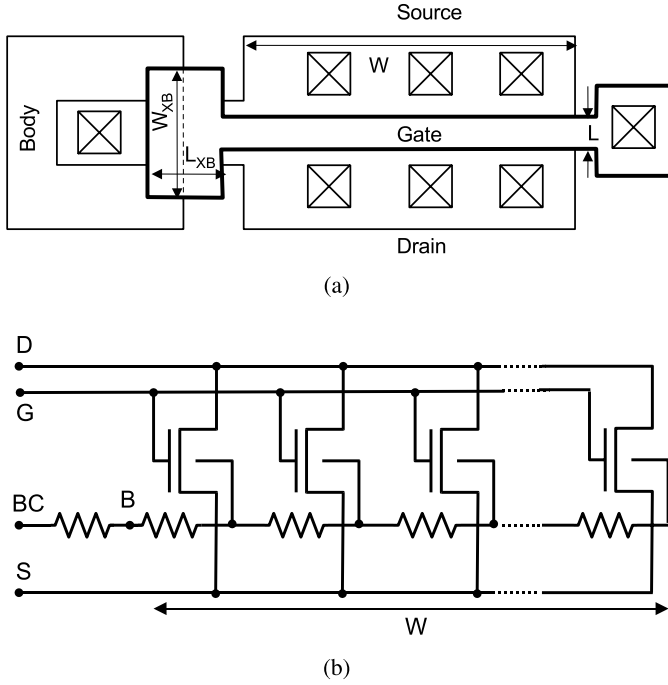


Fig. 2.13 (a) Typical structure of a T-gate SOI device. For an H-gate SOI device, another body contact is patterned at the other end of the gate. (b) Schematic representation of the T-gate SOI subcircuit taking into account the distributed nature of body resistance

where R_{bsh} is the body sheet resistance and W and L are the width and length of the device. In practical applications the body resistance is highly bias-dependent. In some cases, the silicon film can become fully depleted and the resistance of the body region becomes so high that the body terminal is effectively disconnected from the internal body of the device.

In PSP-SOI, a bias-dependent body resistance model is provided to capture the variation of R_B with the terminal voltages:

$$R_B = W^2 / (\mu_B Q_{nbr}), \quad (2.21)$$

where μ_B is the mobility of majority carriers in the body (holes in nMOSFETs), and Q_{nbr} is the absolute value of the mobile charge in the quasi-neutral body region. It can be expressed as

$$Q_{nbr} = q N_{EFF} t_{si} W L - Q_B. \quad (2.22)$$

Here N_{EFF} is the effective channel doping including the effect of halo implants, and t_{si} is the channel silicon film thickness. The total bulk charge Q_B includes the (front) gate induced bulk charge Q_B^f , the junction depletion charges $Q_{j,S/D}$ and the back-gate induced bulk charge Q_E , as illustrated in Fig. 2.14.

Fig. 2.14 Illustration of the calculation of mobile charge Q_{nbr} in the neutral body region

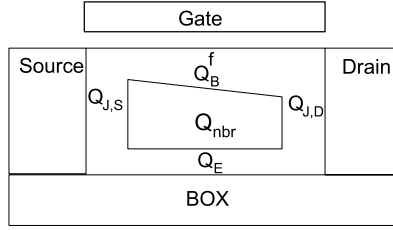


Fig. 2.15 Measured and modeled body resistance of a body-contacted SOI MOSFET (H-gate). $V_{GS} = -0.3$ V, $V_{DS} = 0$ V, back-gate bias $V_{ES} = 0$, -10 V; $W/L = 3$ $\mu\text{m}/0.065$ μm . The sudden drop of body resistance near $V_{BS} = 0.8$ V is caused by the leakage current of highly forward biased junction). After [71]

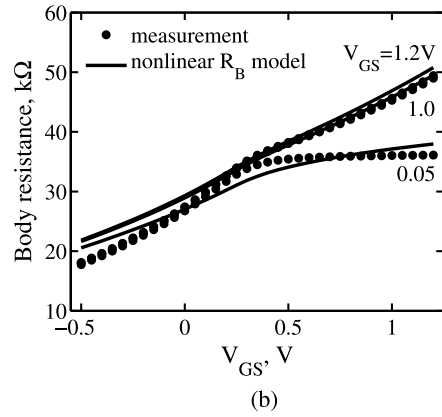
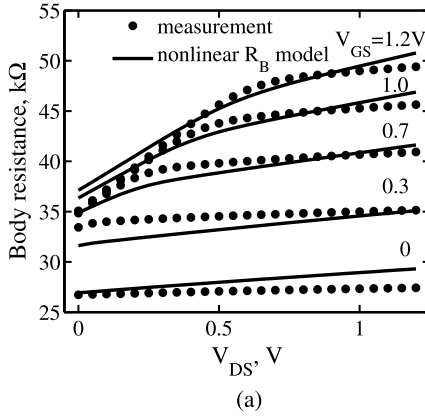
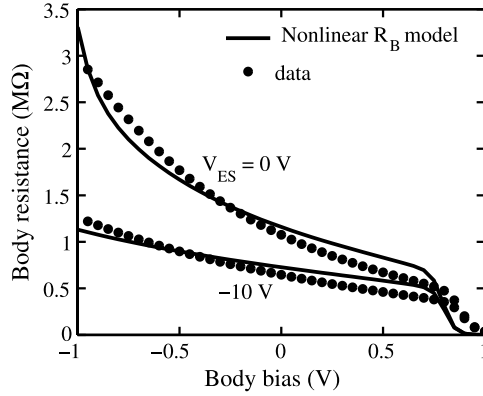


Fig. 2.16 Measured and modeled body resistance of an H-gate SOI structure under varying DC bias condition; $W/L = 4$ $\mu\text{m}/2\mu\text{m}$. After [70]

Figure 2.15 shows the fitting results of body resistance measured on a body-contacted SOI MOSFET with the nonlinear body resistance model. It clearly shows that the body resistance varies significantly with the external body bias V_{BS} even when the device is off. If the linear, bias-independent model is used, the body resistance is commonly set between the minimum and maximum measured values. In the simulations presented in this work, we set $R_B = 1.09$ M Ω (value at $V_{BS} = 0$ V)

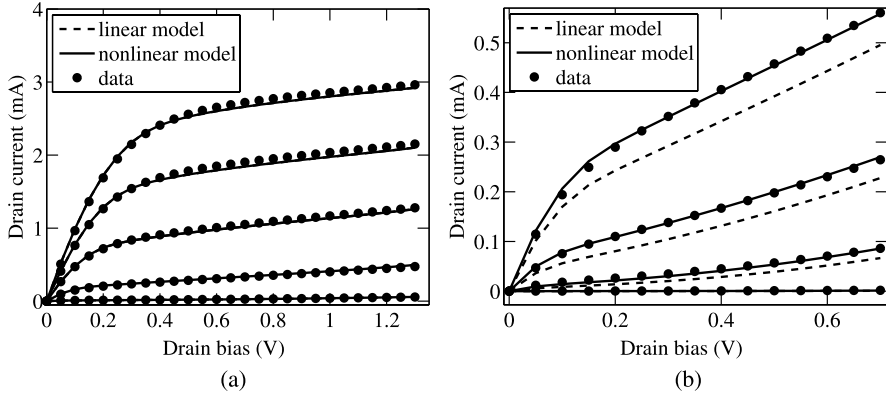


Fig. 2.17 (a) Measured and modeled drain current of a body-contacted SOI MOSFET at large forward body bias. $V_{BS} = 0.6$ V, $V_{GS} = 0.2, 0.4, 0.6, 0.8, 1.0$ V; $W/L = 3 \mu\text{m}/0.065 \mu\text{m}$. (b) Measured and modeled drain current at large reverse body bias. $V_{BS} = -0.6$ V, $V_{GS} = 0.2, 0.4, 0.5, 0.6$ V. After [71]

for the linear model. Figure 2.16 shows measured and modeled body resistance of an H-gate SOI structure under varying DC bias conditions.

When the body of a PD-SOI MOSFET is highly forward biased, the body resistance becomes small enough to bleed off all the DC currents injected into the body region without causing any substantial variation in the body potential. As shown in Fig. 2.17, both linear and nonlinear models can predict the output characteristics of the body-contacted SOI MOSFET when $V_{BS} = 0.6$ V and $V_{BS} = -0.6$ V. However, when the body is highly reverse biased, the body resistance becomes very large. The body contact becomes less effective in controlling the internal body potential and thus the device has a lower threshold voltage.

Figure 2.18 shows the impact of body resistance on the threshold voltages of the body-contacted SOI MOSFET at both low and high drain biases. As expected, V_T is significantly overestimated by the linear R_B model at a large reverse body bias, while the nonlinear model can accurately fit the experimental data. The effect of body resistance on I_{dlin} (I_{DS} at $V_{DS} = 0.05$ V, $V_{GS} = 1.2$ V) is also illustrated in Fig. 2.19. Simulation results indicate that I_{dlin} is increased if the nonlinear R_B model is used. This is consistent with the corresponding results for V_T shown in Fig. 2.18.

In several sensitive applications (e.g. DTMOS), the distributed nature of the body resistance needs to be included in SOI compact models [52, 66]. In PSP-SOI, the internal body node (B) is accessible to the model user so that the distribution effect can be accounted for by partitioning a wide device into several segments along the width direction with proper handling of the narrow-width effects [cf. Fig. 2.14(b)]. For each segment, the width $W_i = W/N_i$, where N_i is an integer number and $\sum_i 1/N_i = 1$ [52]. In this chapter, the effect of body resistance on device characteristics is studied using distributed R_B model.

In principle, segmentation can pose a significant penalty in terms of simulation time. Practically, a lumped body resistance model with the effective resistance

Fig. 2.18 Measured and modeled threshold voltage at low drain bias ($V_{DS} = 0.05$ V). After [71]

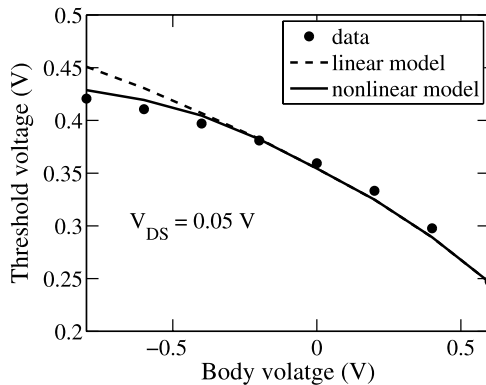
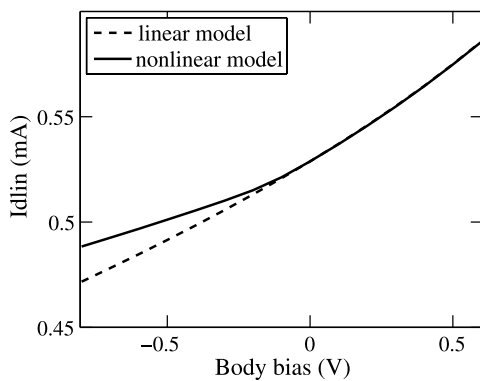


Fig. 2.19 Simulated Idlin (drain current at $V_{GS} = 1.2$ V and $V_{DS} = 0.05$ V). Model parameters for PSP-SOI are extracted from IBM 65 nm PD-SOI technology data. After [71]



$R_{B,eff} = R_B/3$ for T-gate SOI devices or $R_{B,eff} = R_B/12$ for H-gate SOI devices is often adequate [22, 66]. This lumped model works well when hysteresis is negligible, and is even accurate to within 10% in predicting delays when the device is hysteretic [66].

2.5 Noise Modeling

SOI technology has become a viable option for RF applications and RF systems-on-chip. Consequently, accurate noise descriptions in compact models of SOI MOSFETs become essential.

The two main noise sources in MOSFETs are the low frequency noise (also called $1/f$ noise) and the thermal noise. In PSP-SOI, these noise sources, together with the channel induced gate noise are modeled physically following the description developed for the bulk PSP model including velocity saturation effects [19, 44]. In particular, the shot noise in the subthreshold region is recovered automatically from the channel thermal noise using surface potential based formulation. Several other noise sources common to both bulk and SOI MOSFETs are included, such as shot

noises associated with gate-tunneling current, junction leakage current, GIDL/GISL and impact ionization. PSP-SOI includes three additional noise sources relative to the bulk PSP model: shot noise associated with the EVB tunneling current with the spectral density [47]

$$S_{I_{EVB}}(G, B) = 2q I_{EVB}, \quad (2.23)$$

and the shot noise associated with the parasitic BJT [67]

$$S_{I_{BJT}}(D, S) = 2q I_{BJT}. \quad (2.24)$$

For body-contacted SOI device, the thermal noise generated in the body resistance [16] is

$$S_{V, R_B}(B, BC) = 4k_B T R_B, \quad (2.25)$$

where the body resistance R_B is given by (2.21).

For floating body PD-SOI MOSFET, experimental data indicate the presence of excess Lorentzian-like noise overshoot in the low-frequency range [27, 57, 67]. The frequency dependence of the excess noise spectral density has been found to be

$$S_f = \frac{S_0}{1 + (f/f_c)^2}, \quad (2.26)$$

where S_0 corresponds to the low-frequency plateau and f_c is the corner frequency, which is determined by the small signal impedance of the body node and hence strongly depends on the drain bias through impact ionization current.

The excess noise in the drain current is caused by the floating body effect which amplifies the shot noises associated with the body-source junction current [27], impact ionization current, gate-to-body tunneling current, and for body-contacted SOI, the thermal noise of the body resistance. Since the parasitic body currents and the associated shot noises are physically modeled in PSP-SOI, the excess noise at low frequency with the spectral density (2.26) comes out automatically. The simulated equivalent drain output noise is shown in Fig. 2.20, demonstrating the qualitative agreement of simulation results with experimental observations [27].

2.6 PD-SOI MOSFET Model Verification

PSP-SOI has been verified against several PD-SOI processes, including 90 nm and 65 nm nodes from both Freescale and IBM. The first step in the model verification process is the treatment of self-heating effect for which two methods have been proposed [22]. The common approach is to characterize the thermal resistance through the electrical resistance measurement of the polysilicon gate [51]. The subsequent model fitting and calibration involve the tuning of both temperature-independent and temperature-dependent model parameters simultaneously (cf. “method 1” in

Fig. 2.20 Simulated equivalent drain output noise spectral density; $V_{GS} = 0.8$ V. $W/L = 3 \mu\text{m}/0.065 \mu\text{m}$. Same set of model parameters as in Figs. 2.22 and 2.23 are used in simulation. After [72]

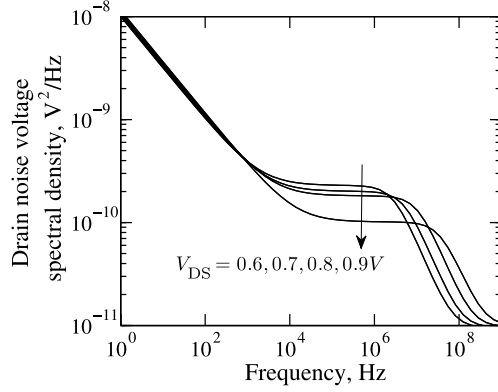


Fig. 2.21 PD-SOI model parameter extraction flow. After [22]

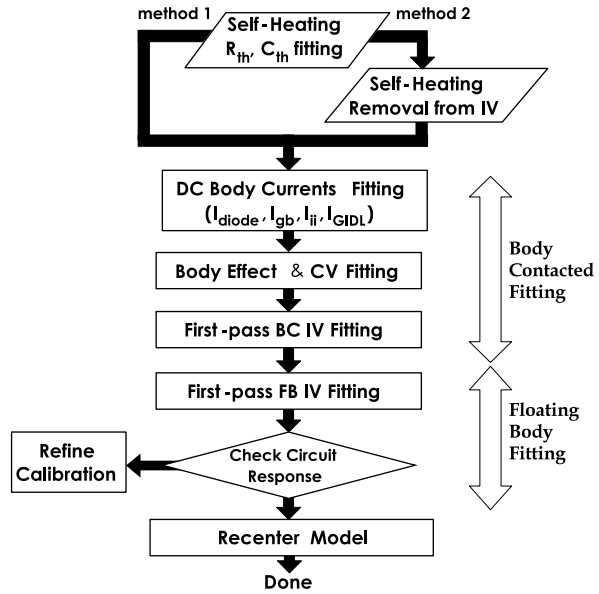


Fig. 2.21). The second approach starts from generating self-heating free $I(V)$ data from static measurements [9, 39] (cf. “method 2” in Fig. 2.21). The self-heating removal is applied to various body currents, such as impact ionization current. In method 2, the temperature-independent and temperature-dependent model parameters are tuned separately which requires fewer iterations relative to method 1.

To fit the floating body device characteristics, parasitic capacitance and current components should be fitted first on body-contacted devices. The reason is that impact ionization current, junction current, gate-to-body tunneling, and GIDL/GISL, etc. are all important in determining the floating body effect but can not be measured directly on floating body devices.

Figures 2.22 and 2.23 show typical model fitting results on an n-channel floating body SOI MOSFET with channel length $L = 55$ nm. In the parameter extrac-

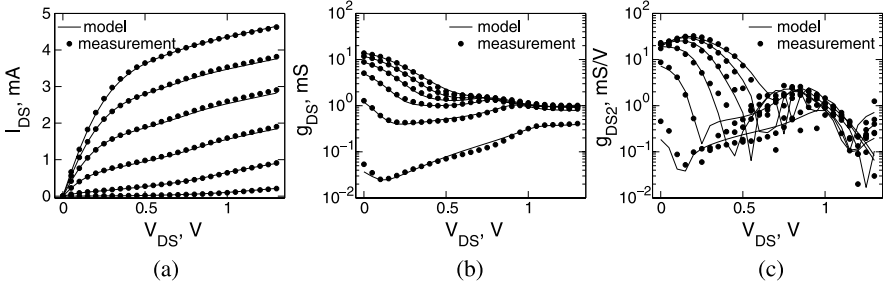


Fig. 2.22 Output characteristics of a short channel floating body nMOSFET. (a) Drain current; (b) Conductance g_{DS} ; (c) Second-order conductance $g_{DS2} = \partial g_{DS} / \partial V_{DS}$. $W/L = 3 \mu\text{m}/0.055 \mu\text{m}$. $V_{GS} = 0.2, 0.4, 0.6, 0.8, 1.0, 1.2 \text{ V}$. After [72]

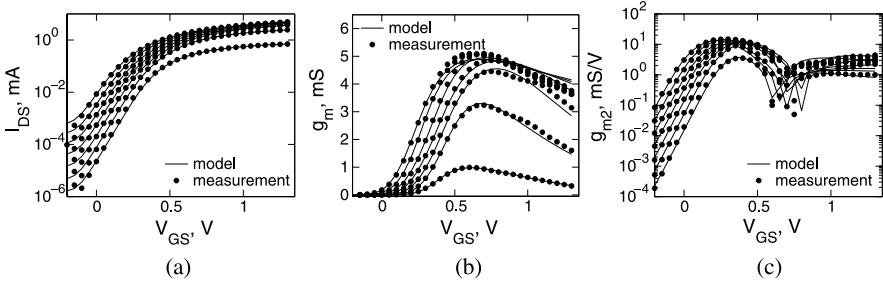


Fig. 2.23 Transfer characteristics of a short channel floating body nMOSFET. (a) Drain current; (b) Transconductance g_m ; (c) Second-order transconductance $g_{m2} = \partial g_m / \partial V_{GS}$. $W/L = 3 \mu\text{m}/0.055 \mu\text{m}$. $V_{DS} = 0.05, 0.2, 0.4, 0.6, 0.8, 1.0, 1.2 \text{ V}$. After [72]

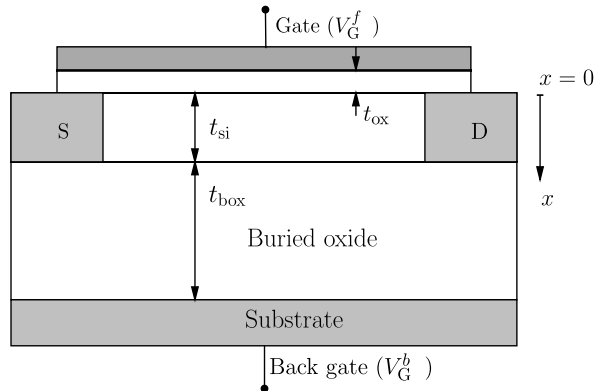
tion routine, we first extract the model parameters on a body-contacted n-channel MOSFET with the same channel length. Parasitic current components which control the floating body effect (as discussed in Sect. 2.2), such as impact ionization, junction leakage, etc., are extracted from separate dc measurements. As we can see, not only the drain current is accurately reproduced by the PSP-SOI model, the conductance [Fig. 2.22(b)] and transconductance [Fig. 2.23(b)] are also reproduced by the model. This demonstrates that PSP-SOI is suitable for both digital and analog applications.

In order to simulate the signal distortion associated with the nonlinearities of PD-SOI MOSFETs, the compact model should reproduce the higher-order conductances and transconductances. Typical results are shown in Figs. 2.22(c) and 2.23(c).

2.7 Modeling of Dynamically Depleted SOI MOSFETs

An SOI MOSFET switching between the PD and FD modes for different terminal voltages is said to be operating in the dynamic depletion mode [49, 55]. Accurate

Fig. 2.24 Cross-section of a DD-SOI MOSFET structure. V_G^f is the (front) gate voltage, V_G^b is the back gate (substrate) voltage



modeling of the DD effect can be based on the well-known principles, but the challenge is to make the formulation compatible with the needs of compact modeling without any significant loss of the accuracy essential for the SOI circuit simulations.

There are several approaches to develop compact models of dynamically depleted SOI devices. In the traditional threshold-voltage-based formulation this has been accomplished using the concept of the body-to-source built-in potential lowering to provide a link between the PD and FD modes [55, 63]. The surface-potential-based approach, which has emerged as the mainstream of the compact modeling for both bulk [19, 20] and PD-SOI [38, 69, 72] devices, has been already introduced for the DD-SOI in [2, 26, 30, 49, 75]. It starts from the first integral of Poisson's equation in the channel region. The surface potential equation (SPE) is then obtained by including boundary conditions at the two Si/SiO₂ interfaces. Together with the coupling equation between the front and back surfaces, the front and back surface potentials (denoted as ψ_s^f and ψ_s^b) are calculated and then used to formulate the drain current and the terminal charges models.

PSP-SOI-DD is based on a mathematically well-conditioned SPE and an approximate coupling equation which explicitly includes the back gate effect. To obtain explicit expressions for both the drain current and terminal charges, a new symmetric linearization method is developed specifically for DD-SOI. This allows us to formulate the model within the context of the PSP and PSP-SOI-PD models but with DD effects included. The secondary effects can be then adopted directly from PSP-SOI-PD as in [19, 70, 72].

2.7.1 Surface Potential and Coupling Equations

The surface potential equation for dynamically depleted SOI MOSFETs can be obtained from Poisson's equation considering the boundary conditions at the front and

back interfaces [40] (cf. Fig. 2.24):

$$\begin{aligned} & \left(V_G^f - V_{FB}^f - \psi_s^f \right)^2 - \left(\frac{t_{ox}}{t_{box}} \right)^2 \left(V_G^b - V_{FB}^b - \psi_s^b \right)^2 \\ & = G(\beta \psi_s^f, \Delta_n) - G(\beta \psi_s^b, \Delta_n). \end{aligned} \quad (2.27)$$

In PSP-SOI-DD, the form of G is somewhat different than in [40] in order to take advantage of the experience gained in the development of the bulk PSP model:

$$G(x, \Delta_n) = \gamma^2 \phi_t \left[e^{-x} + x - 1 + \Delta_n \left(e^x - x - 1 - \frac{x^2}{x^2 + 2} \right) \right], \quad (2.28)$$

where ψ_s^f and ψ_s^b are the front and back surface potentials, and V_{FB}^f and V_{FB}^b are the front and back gate flat-band voltages, respectively. γ is the body factor, $\Delta_n = \exp[-\beta(2\phi_B + V_{CB})]$ where V_{CB} is imref splitting. Function $G(x, \Delta_n)$ has been conditioned to prevent the possibility of being negative ($G < 0$) and allows us to set $\Delta \psi_s^f = 0$ in accumulation without producing spurious $C(V)$ characteristics [21, 35, 68].

The rigorous form of the coupling equation required to solve the surface potentials (ψ_s^f and ψ_s^b) from (2.27) is given by [34, 40]

$$t_{si} = \int_{\psi_s^b}^{\psi_s^f} d\phi / E_x, \quad (2.29)$$

where

$$E_x = \text{sgn}(\phi) \cdot \sqrt{\left(E_s^f \right)^2 - (C_{ox}/\varepsilon_s)^2 \left[G(\beta \psi_s^f, \Delta_n) - G(\beta \phi, \Delta_n) \right]} \quad (2.30)$$

is the electric field component along the x direction and E_s^f is the electric field at the front interface. Since the integral in (2.29) requires numerical evaluation, this formulation is not conducive to the compact model development. It is used primarily to verify the accuracy of the approximate closed form coupling equation developed below.

The simplest approximate coupling equation is obtained by neglecting the inversion charge and assuming that Si film is fully depleted [32]:

$$\psi_s^b = \psi_s^f - \psi_c + r_c \left(V_G^b - V_{FB}^b - \psi_s^b \right), \quad (2.31)$$

where $r_c = C_{box}/C_b$, $C_{box} = \varepsilon_{ox}/t_{box}$, $C_b = \varepsilon_s/t_{si}$, and

$$\psi_c = \frac{q N_A t_{si}^2}{2\varepsilon_s}. \quad (2.32)$$

From (2.31)

$$\psi_s^b = \frac{1}{1+r_c} (\psi_s^f - \psi_c) + \frac{r_c}{1+r_c} (V_G^b - V_{FB}^b). \quad (2.33)$$

The second term describes the back gate effect.

The coupling equation (2.33) is applicable only in the FD mode of operation. In the PD mode, ψ_s^b is decoupled from ψ_s^f and its value ψ_{s0}^b is determined from

$$\left(\frac{t_{ox}}{t_{box}} \right)^2 (V_G^b - V_{FB}^b - \psi_{s0}^b)^2 = G(\beta \psi_{s0}^b, 0). \quad (2.34)$$

To explicitly describe the transition between the PD and FD modes, smoothing function is employed:

$$\psi_s^b = \psi_{s0}^b + \frac{\phi_t}{1+r_c} \ln \left\{ \frac{1 + \exp[\beta(\psi_s^f - \psi_c^*)]}{1 + \exp(-\beta\psi_c^*)} \right\}, \quad (2.35)$$

where

$$\psi_c^* = \psi_c - r_c (V_G^b - V_{FB}^b) + (1+r_c)\psi_{s0}^b. \quad (2.36)$$

For $\beta(\psi_s^f - \psi_s^b) \gg 1$ we recover the FD mode described by (2.33), while for $\psi_s^f < \psi_c^* - 3\phi_t$ the device operates in the PD mode and $\psi_s^b \approx \psi_{s0}^b$. The inclusion of the small factor $\exp(-\beta\psi_c^*)$ assures that $\psi_s^b = \psi_{s0}^b$ for $\psi_s^f = 0$, as expected from the physical considerations.

Equation (2.35) is conceptually similar to that used in [49] but does not assume $r_c = 0$ and uses a more complete form of ψ_c^* including the back gate effect.

2.7.2 Symmetrically Linearized Charge-Sheet Model for DD-SOI

Compact surface-potential-based models of bulk and SOI MOSFETs are based on charge-sheet approximation [3]. Following [40], the front channel inversion charge density (normalized to WLC_{ox}) is approximated by

$$q_i = -(V_G^f - V_{FB}^f - \psi_s^f) + \sqrt{(V_G^f - V_{FB}^f - \psi_s^f)^2 - \gamma^2 \phi_t \Delta_n (e^{\beta\psi_s^f} - \beta\psi_s^f - 1)}. \quad (2.37)$$

Once surface potentials and inversion charge are available, the intrinsic drain current can be computed from the drift and diffusion equation [3, 58]

$$I_{DS} = -W\mu_n C_{ox} \left(q_i \frac{\partial \psi_s^f}{\partial y} - \phi_t \frac{\partial q_i}{\partial y} \right), \quad (2.38)$$

y is the position along the channel. After integration

$$I_{DS} = -\mu_n \left(\frac{W}{L} \right) C_{ox} \left[\int_{\psi_{ss}^f}^{\psi_{sd}^f} q_i d\psi_s^f + \phi_t (q_{is} - q_{id}) \right] \quad (2.39)$$

where ψ_{ss}^f , ψ_{sd}^f and q_{is} and q_{id} are the values of ψ_s^f and q_i at the source and drain ends of the channel, respectively.

In SP [6, 20] and PSP [19] models, the drain current and the intrinsic terminal charges are formulated using symmetric linearization method. The inversion charge (per unit area) is approximated by its first order Taylor expansion at the potential middle point ψ_m :

$$q_i = q_{im} - \alpha_m u, \quad (2.40)$$

where $q_{im} = q_i|_{\psi_s=\psi_m}$ is the inversion charge at the surface potential middle point, $u = \psi_s - \psi_m$, and the linearization coefficient

$$\alpha_m = - \left. \frac{\partial q_i}{\partial \psi_s} \right|_{\psi_s=\psi_m}. \quad (2.41)$$

For an SOI MOSFET operating in the PD mode, (2.40) is the same as for a bulk MOSFET. When MOSFET enters the FD mode, the channel silicon film is fully depleted and the bulk charge density $-qN_{Atsi}$ becomes position-independent and also no longer depends on ψ_s^f . Once it happens [34]

$$q_i = - \left[V_G^f - V_{FB}^f - \psi_s^f - \frac{qN_{Atsi}}{C_{ox}} - \frac{C_b}{C_{ox}} (\psi_s^f - \psi_s^b) \right] \quad (2.42)$$

becomes an approximately linear function of ψ_s^f . This results in unit value of the linearization coefficient because in FD mode, $\alpha_m^{DD} \approx 1 + C_b/C_{ox} \approx 1$. Hence the original symmetric linearization method [19, 20] can not be applied directly to the modeling of dynamically depleted SOI MOSFETs.

Instead, the following adaptation of symmetric linearization method is used:

$$q_i = q_{im} - \alpha_m^{DD} u_f, \quad (2.43)$$

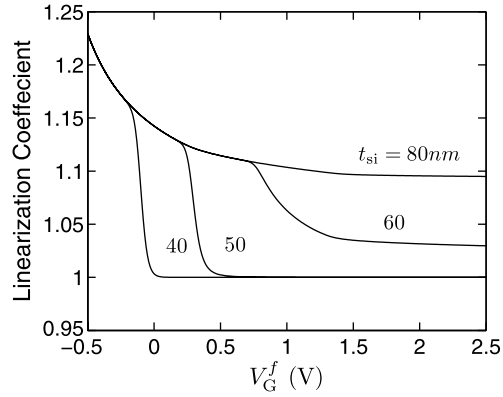
where $u_f = \psi_s^f - \psi_m^f$ and $\psi_m^f = (\psi_{ss}^f + \psi_{sd}^f)/2$. The linearization coefficient is approximated as

$$\alpha_m^{DD} = \frac{q_{is} - q_{id}}{\Delta \psi_f}, \quad (2.44)$$

where $\Delta \psi_f = \psi_{sd}^f - \psi_{ss}^f$.

A similar form for the linearization coefficient has been already used in the recent core compact model of a double-gate MOSFET [13, 14]. In [14] its accuracy was also verified for a bulk MOSFET case. In the final analysis, the accuracy of (2.43) and (2.44) is established by comparison with numerical computations presented below.

Fig. 2.25 Linearization coefficient α_m^{DD} as a function of the front gate bias for different silicon film thicknesses. $t_{ox} = 2$ nm, $t_{box} = 200$ nm, $N_A = 5 \times 10^{17}$ cm $^{-3}$. $V_{FB}^f = -0.9$ V, $V_G^b = 0$ V, $V_{FB}^b = 0$ V and $V_{DS} = 1$ V. After [73]



The expression for the drain current follows from (2.39) and (2.43) and has the same form as in [19, 20]

$$I_{DS} = \mu(W/L)C_{ox} \left(q_{im} + \alpha_m^{DD} \phi_t \right) \Delta\psi_f \quad (2.45)$$

except that now q_{im} and α_m^{DD} are different functions of the terminal voltages.

Figure 2.25 shows α_m^{DD} calculated from (2.44) as a function of front gate voltage for several different silicon film thicknesses. For $t_{si} = 80$ nm, the device is always partially depleted, thus, the dependence of α_m^{DD} on the front gate bias is similar to that in a bulk MOSFET. For $t_{si} = 40, 50$ nm, we can see the smooth transition of α_m^{DD} between the PD and FD modes of operation. For $t_{si} = 60$ nm, the silicon film is always partially depleted at the source end, but it can be fully depleted at the drain end, depending on the front gate bias. For this case, we can see that α_m^{DD} lies between its values in PD and FD modes. It follows that without using any smoothing functions expression (2.44) provides the expected limits of the linearization coefficient in the PD and FD modes as well as the smooth transition between the two limiting cases.

The derivation of the compact expressions for the terminal charges requires position dependence of the front surface potential which follows from (2.38) and (2.45):

$$y = y_m + \frac{L}{\Delta\psi_f} \cdot \left[\psi_{ss}^f - \psi_{sm}^f - \frac{(\psi_{ss}^f - \psi_{sm}^f)^2}{2H} \right], \quad (2.46)$$

where

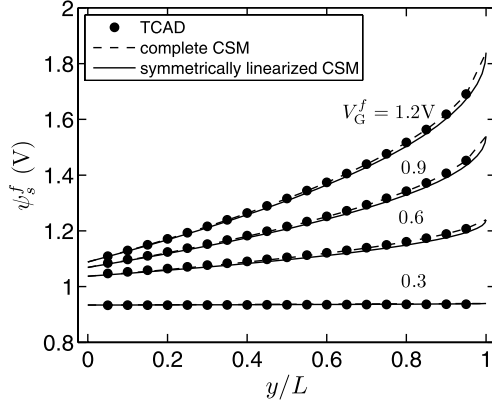
$$y_m = \frac{L}{2} \cdot \left(1 + \frac{\Delta\psi_f}{4H} \right) \quad (2.47)$$

is the coordinate of the front gate surface potential middle point and

$$H = \phi_t - q_{im}/\alpha_m^{DD}. \quad (2.48)$$

Fig. 2.26 Front surface potential along the channel for the complete and symmetrically linearized charge-sheet model.

$t_{ox} = 2$ nm,
 $N_A = 5 \times 10^{17} \text{ cm}^{-3}$,
 $t_{si} = 40$ nm, $t_{box} = 200$ nm,
 $V_{FB}^f = -0.8$ V, $V_{FB}^b = 0$ V,
 $V_{DS} = 1.2$ V. After [73]



Solving for $\psi_s^f(y)$ yields

$$\psi_s^f = \psi_{sm}^f + H \left[1 - \sqrt{1 - \left(\frac{2\Delta\psi_f}{HL} \right) (y - y_m)} \right]. \quad (2.49)$$

Comparison of (2.49) with $\psi_s^f(y)$ dependence corresponding to the complete CSM is shown in Fig. 2.26. This further confirms the accuracy of the proposed version of the symmetric linearization method.

With $\psi_s^f(y)$ given by form (2.49) the total gate charge (all charges are normalized to WLC_{ox})

$$Q_G = (1/L) \int_0^L (V_G^f - V_{FB}^f - \psi_s^f) dy \quad (2.50)$$

can be evaluated in a closed form:

$$Q_G = V_G^f - V_{FB}^f - \psi_{sm}^f + \frac{\Delta\psi_f^2}{12H}. \quad (2.51)$$

The source and drain terminal charges are obtained in the Ward-Dutton partition [65]. We have

$$Q_D = (1/L) \int_0^L (y/L) q_i dy, \quad (2.52)$$

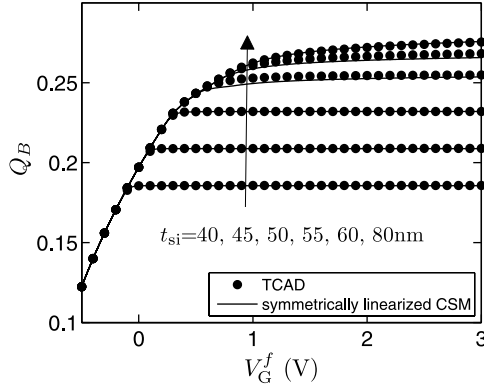
or, explicitly

$$Q_D = \frac{q_{im}}{2} + \frac{\alpha_m^{DD} \Delta\psi_f}{12} \left(1 - \frac{\Delta\psi_f}{2H} - \frac{\Delta\psi_f^2}{20H^2} \right). \quad (2.53)$$

The source charge $Q_S = Q_I - Q_D$ where

$$Q_I = q_{im} + \frac{\alpha_m^{DD} \Delta\psi_f^2}{12H}. \quad (2.54)$$

Fig. 2.27 Normalized bulk charge Q_B as a function of the front gate bias. In the simulation, $t_{ox} = 2$ nm, $t_{box} = 200$ nm, $N_A = 5 \times 10^{17} \text{ cm}^{-3}$, $V_{FB}^f = -0.9$ V, $V_G^b = 0$, $V_{FB}^b = 0$, $V_{DS} = 0.5$ V. After [73]



Finally, the bulk charge is obtained from the neutrality condition $Q_B = Q_G - Q_I$.

Of the various charges, Q_B is most sensitive to the operating mode of the SOI MOSFET. For this reason it is chosen to investigate the accuracy of the symmetrically linearized CSM relative to the TCAD simulations. The results shown in Fig. 2.27 indicate that introducing symmetric linearization has little or no effect on the CSM output. In particular, the qualitative change in the $Q_B(V_G^f)$ dependence associated with the transition to the FD mode of operation is accurately reproduced.

It is worth noting that for bulk MOSFET analytical expressions for terminal charges are complex but, nevertheless, available in a closed form [36, 64] so that the use of symmetric linearization is a matter of efficiency. For DD-SOI analytical evaluation of the terminal charges using complete CSM is impossible. Hence symmetric linearization is the enabling factor in the formulation of compact model for the terminal charges.

Apart from the different bias dependence of α_m^{DD} and H , the final forms of the expressions (2.51), (2.53) and (2.54) is the same for bulk, PD, DD and multi-gate transistors [13, 19, 20]. The accuracy is about the same in all cases.

2.8 DD-SOI Model Verification and Discussion

In the previous section we considered the core PSP-SOI-DD model and accuracy of symmetric linearization method relative to the complete CSM formulation. A more detailed model verification is accomplished by comparing the $I(V)$ and $C(V)$ characteristics with the results of TCAD simulations. The complete PSP-SOI-DD model including small-geometry effects is implemented in circuit simulators using Verilog-A approach [31]. The front and back surface potentials are solved using analytical approximation conceptually similar to the PSP bulk and PSP-SOI-PD models. Secondary effects, such as quantum mechanical correction, polysilicon depletion, velocity saturation, etc. are included as well. The model retains the floating body simulation capability which is important to model the device characteristics in the PD mode.

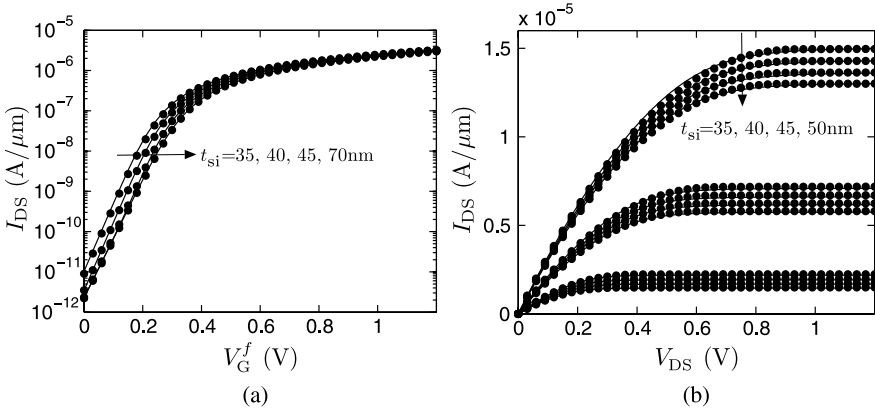


Fig. 2.28 (a) Transfer characteristics of SOI MOSFETs with different silicon film thicknesses. $V_{DS} = 0.1$ V and $V_G^b = 0$; (b) Output characteristics of SOI MOSFETs with different silicon film thicknesses. The front gate bias $V_G^f = 0.6, 0.9$ and 1.2 V and the back gate bias $V_G^b = 0$; The symbols represent the TCAD simulation data and the lines stand for the PSP-SOI-DD model. After [73]

Figure 2.28(a) shows the transfer characteristics of SOI MOSFETs with different silicon film thicknesses. The compact model accurately reproduces the TCAD simulation data. The device which is fully depleted for $t_{si} = 35$ nm becomes partially depleted for $t_{si} = 70$ nm. The transition between PD and FD modes is clearly indicated by the subthreshold slope change as a function of silicon film thickness. In FD mode, the SOI MOSFET has nearly ideal subthreshold slope due to the very small capacitance of the buried oxide layer. In PD mode, the subthreshold slope increases as a consequence of the relatively large capacitance of the depletion layer.

Figure 2.28(b) shows the output characteristics of SOI MOSFETs with different silicon film thickness. The output current increases as t_{si} is reduced. This follows from the fact that an FD SOI device with smaller t_{si} has a lower threshold voltage with other device parameters being the same.

Figure 2.29(a) shows the simulated and modeled transfer characteristics of a long-channel SOI MOSFET. As V_G^b changes from -4 V to 4 V, the subthreshold slope is decreasing to its ideal value (60 mV/dec) as the device enters the FD mode. Figure 2.29(b) shows the output characteristics of an SOI MOSFET with $t_{si} = 40$ nm for different gate and substrate biases. At large positive substrate bias ($V_G^b = 5$ V) the device is fully depleted and shows minimum floating body effect (“kink”). However, for $V_G^b = -5$ V, the device is partially depleted and exhibits pronounced floating body effect.

As all modern compact models, PSP-SOI-DD is charge based in order to preserve charge conservation [5]. However, it is a common practice to evaluate the model accuracy in terms of $C(V)$ characteristics which are more sensitive than terminal charges to any problems in model formulation. Figure 2.30 compares the simulated gate transcapacitances obtained from TCAD simulation and the compact model. For $t_{si} = 40$ nm, the device becomes fully depleted around $V_G^f \simeq 0$ V; without channel

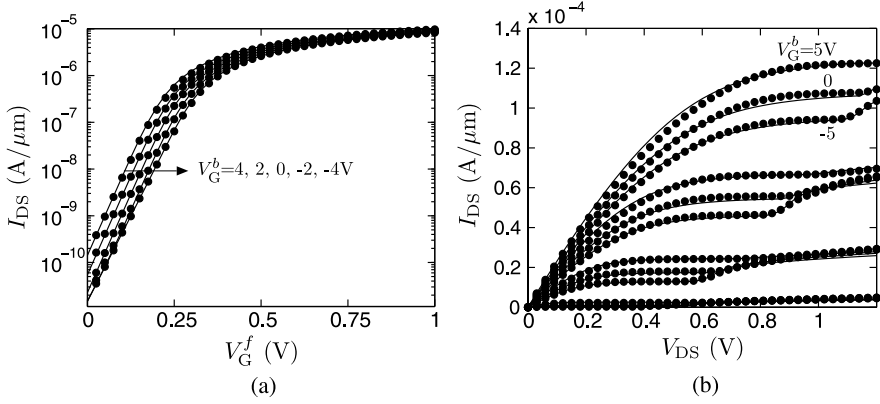


Fig. 2.29 (a) Transfer characteristics of an SOI MOSFET with $t_{si} = 40$ nm at different back gate biases. $V_{DS} = 0.1$ V; (b) Output characteristics of an SOI MOSFET with $t_{si} = 40$ nm at different back gate biases. The front gate bias $V_G^f = 0.3, 0.6, 0.9$ and 1.2 V, the back gate bias $V_G^b = -5, 0, 5$ V; The symbols represent the TCAD simulation data and the lines stand for the PSP-SOI-DD model. After [73]

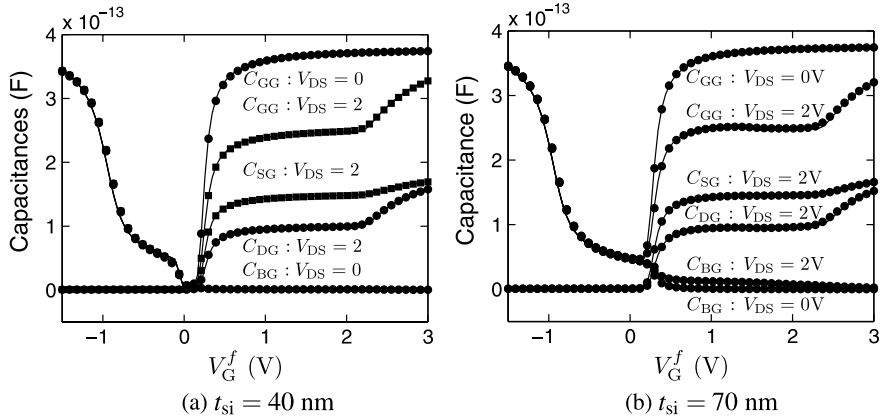


Fig. 2.30 Capacitances for $t_{si} = 40$ and 70 nm. $N_A = 5 \times 10^{17} \text{ cm}^{-3}$, $V_{DS} = 0$ and 2 V. The symbols represent the TCAD data and the lines stand for the PSP-SOI-DD model results. After [73]

inversion, the gate capacitance becomes

$$C_{gg} \approx \frac{C_{ox} C_b}{C_{ox} + C_b} \approx C_b \quad (2.55)$$

assuming $C_{ox} \gg C_b$. This behavior has been already experimentally observed and captured in a threshold-voltage based DD-SOI model [48]. Finally, as shown in Fig. 2.30(b) PSP-SOI-DD also accurately describes the transcapacitances of a partially depleted device with a thicker channel film thickness ($t_{si} = 70$ nm).

2.9 Conclusions

Surface-potential-based approach provides a foundation for the advanced compact models of SOI transistors compatible with the compact models of bulk MOSFETs. Using PSP model as a starting point we present two fully developed SOI models for PD and DD applications which satisfy all requirements imposed by the growing analog-mixed signal and RF applications of SOI technology. For the SOI-DD applications it is sufficient to solve two rather than three coupled surface potential equations as long as $t_{box} \gg t_{ox}$. This enables analytical approximations for the front end surface potential and obviates the need for the iterative solution. Efficient formulation of the SOI-DD electrostatics allows one to capture the details of the transistor behavior including the smooth transition between the PD and FD modes on all $C(V)$ and $I(V)$ characteristics and the back bias effect. Symmetric linearization method can be extended to both SOI-PD and SOI-DD models to achieve a unified formulation of the drain current and terminal charges in all PSP-family models (SP [20], PSP [19], PSP-SOI-PD [72], PSP-SOI-DD [73], MOSVAR [61], PSP-DGFET [13, 14, 50]). For the core model the details of the device physics enter through the bias and geometry dependence of the function H and linearization coefficient. Surface potential-based formulation of the effects specific for SOI devices such as the bias dependence of the body resistance and of the EVB tunneling current has been developed as well. When combined with the advanced junction model [45], and thermal node for the description of the self-heating effects, new formulation provides accurate description of SOI devices already verified against experimental data for several SOI technology nodes.

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