

Chapter 2

Terrestrial Neutron-Induced Failures in Semiconductor Devices and Relevant Systems and Their Mitigation Techniques

2.1 Introduction

2.1.1 SER in Memory Devices

Scaling down of semiconductor devices to sub-100 nm technology encounters a wide variety of technical challenges like V_{th} variation [1], negative bias temperature instability (NBTI) [2], short-channel effect [3], gate leakage [4], and so on. Terrestrial neutron-induced single-event upset (SEU) is one of such key issues that can be a major setback in scaling.

SEU research in memory devices has initially focused on DRAM but the reliability of SRAMs became very poor in late 1990s [5], triggering intense researches on SRAM SER.

JESD89A [6] was issued in 2003 as the revised version of JESD89, in which alpha-ray, thermal neutron, spallation neutron, (quasi-mono) energetic neutron, and high-altitude/underground field tests are described in a more reasonable way compared to the original JESD89. SERs in logic devices and field programmable gate arrays (FPGAs) were discussed there to a certain degree but test methods were not defined. EIAJ EDR4705 [7] was issued in 2005 with a similar scope with JESD89A as the Japanese guideline. IEC60749-38 [8] was issued with similar scope with JESD89A in 2008. Basic concepts in JESD89A are accepted worldwide as such. Some recent works after 2009, however, have revealed that basic assumptions in JESD89A as exemplified below may not be true anymore beyond 90 nm generations.

Recent works show that some evolution of the standards may be needed. For instance

- The contribution of low-energy proton as the secondary ions from nuclear spallation reaction is significant and will be much greater in smaller generations.
- The SEU cross-section has high peak below 10 MeV due to secondary protons and the peak height continues to be higher as devices scale down.

Also, SER tests for automotive LSIs with memories over 1 Mbits are strongly recommended in AEC-Q100-Rev.G [9]. The impacts from AEC-Q100-Rev.G were discussed in the IOLTS2008 special session [10].

2.1.2 MCU in Memory Devices

In particular, “multi-cell upsets (MCUs),” which are defined as simultaneous errors in more than one memory cell induced by a single event, have been under close scrutiny [11–16]. The concept of MCU, therefore, contains both upsets that can be corrected by error detection/error correction code (EDAC/ECC) as well as those which cannot. The latter is called “multiple bit upset” or “multi-bit upset” (MBU) of memory cells in the same word, and can lead, for example, to hang-ups of computer systems. Though MBUs can be avoided by a combination of ECC and the interleaving technique [2.16], MCUs may still be problematic in high performance devices such as contents addressable memories (CAMs) [17] used in network processors and routers. In the case of system design, it is therefore very important to evaluate MCUs as well as soft-error rates (SERs) of the device in design phase.

Historically, MCUs are understood as taking place when two or more storage nodes are hit by one secondary ion from nuclear spallation reaction in a device. As device scaling down proceeds, novel MCU modes are being reported as “charge sharing among memory storage nodes in the vicinity [15, 18–20] or bipolar effects in p-well [16, 21, 22].” Ibe et al. have proposed multi-coupled bipolar interaction (MCBI) for one of the bipolar MCU mechanisms that is regarded as a parasitic thyristor effect triggered by a single-event snapback (SESB) in the p-well and causes MCU multiplicity of more than 10 bits [16]. It is also reported that MCU physical address pattern differs depending on written data patterns typically between the groups ALLX (all “1” or all “0”) and Checkerboard (CHB or its complement CHBc).

2.1.3 SET and MNU in Logic Devices

Concerns on SEUs are shifting to logic devices. Quantification efforts of SER in logic devices are being developed. Gate-chain methods are among such techniques, where logic gates like inverters [23, 24], NAND [25], NOR [25, 26] gates are connected in series with FFs in-between. Single-event transients (SETs) that take place in some of the gates may be latched in FFs and stored.

Data corruption in radiation hardened-by-design (RHBD) flip flops (FFs) such as DICE [27] is getting recognized as a real threat due to the multi-node upset (MNU) mechanisms caused by the charge-sharing or potential elevation in wells by bipolar events. Some novel RHBD FF designs are proposed to encounter this emerging threat [28–30]. Errors due to glitches in global control line such as clock [31]/SET/REST [32] lines are also being recognized.

2.1.4 Chip/System-Level SER Problem: SER Estimation and Mitigation

MCU and MNU can be a threat in mission-critical systems with an extreme number of logic devices that are mainly protected by spatial or time. Typically, redundancy circuits such as triple module redundancy (TMR) [33], duplication and comparison [34], replication [35] are applied to realize such protection. However, space redundancy techniques cause power, speed and area overhead.

In the actual electronic components, direct estimation of component-layer SER from the database of such logic/memory-level SERs is quite a difficult and painful work. Masking or derating factor must be quantified for such works. Even though such factors are obtained, the estimated component-layer SER must have very wide variation depending on circuits and applications. The variation is not originated from random process so that any statistical cannot be applied, in principle.

2.1.5 Scope of This Chapter

The statistics in SEUs and MCUs in static random access memories (SRAMs) are predicted down to 22 nm process by using the Monte-Carlo simulator CORIMS [36, 37]. It is shown that the impact of MCU and neutrons with energy of less than 10 MeV becomes harsh as the scaling proceeds.

All of the new threats make device/component/system design much more complicated and difficult. To cope with the new threats, they have to be quantified first. New standards for characterization of the fault/error modes in memory/logic devices, components and system may be necessary in order to

- (1) obtain the target level of raw SER (SER without any masking effects) in designing devices for device vendor;
- (2) design cost-effective, low-power, and acceptably reliable components and systems starting with the raw SER databases.

This chapter also discusses and proposes novel approaches with the following features that can overwhelm the setbacks mentioned above:

- (i) Overall reduction approach in component-layer SERs.
- (ii) Experimental approach by which SERs in the component or board layer can be quantified and reduced.
- (iii) Inter-layer built-in reliability (LABIR) that potentially detects and reduces SERs with very low additional spatial overhead, power dissipation, and costs.

In Section 2.2, basic knowledge on terrestrial neutron-induced SER is reviewed. In Section 2.3, experimental techniques to quantify soft-error rate (SER) and relevant international standards are reviewed. In Section 2.4, novel MCU characteristics and their significances are introduced. The physical model, major algorithms relevant to neutron-induced soft-error and SRAM device models for Monte-Carlo

simulation are described in Section 2.5. In Section 2.6, simulation results for scaling effects of SER in SRAMs are presented and discussed. In Section 2.7, quantification methods of SEEs in sequential and combinational logic devices are introduced and possible and necessary revisions in the international standards are discussed. Section 2.8 shows an example of board-level evaluation and mitigation techniques. Section 2.9 discusses hierarchical countermeasures in devices/components/systems. Section 2.10 proposes LABIR and its concept is introduced. Section 2.11 summarizes this chapter.

2.2 Basic Knowledge on Terrestrial Neutron-Induced Soft-Error in MOSFET Devices

2.2.1 Cosmic Rays from the Outer Space

High-energy neutrons, protons, pions, muons, and neutrinos are primarily produced by nuclear spallation reactions of extremely high-energy cosmic rays (mainly protons) with atmospheric nuclei (nitrogen and oxygen) as illustrated in Fig. 2.1 [38]. Charged particles are halted in a relatively short range, but neutrons produce a cascade of spallation reactions (air shower) that eventually make terrestrial neutrons at the ground level. Since charged particles twine around magnetic force lines, the geomagnetic and heliomagnetic fields act as shields against low-energy cosmic rays. Air also acts as a shield against neutrons, so that neutron flux varies with the location on the Earth and solar activity. The neutron energy spectrum at the sea level in NYC is shown in Fig. 2.2 [6]. The terrestrial neutron flux at the sea level is about $20 \text{ n/cm}^2/\text{h}(E_n > 1 \text{ MeV})$.

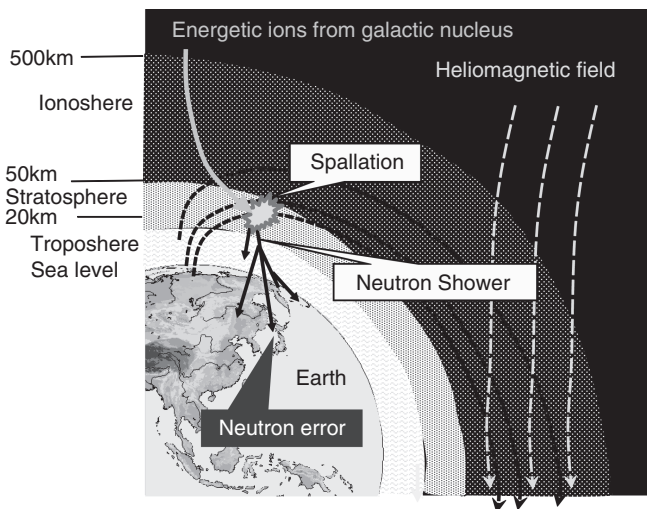


Fig. 2.1 Macroscopic neutron-induced soft-error mechanism

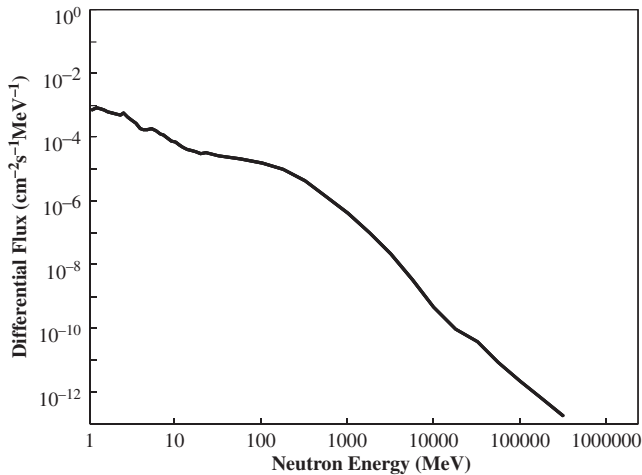


Fig. 2.2 Neutron differential flux spectrum at the sea level in NYC (JESD89A) [6]

2.2.2 Nuclear Spallation Reaction and Charge Collection in CMOSFET Device

A simplified bird's eye view of one-bit CMOS-SRAM (static random access memory) cell is illustrated in Fig. 2.3, with a physical model of neutron-induced soft-error. The n-well (pMOSFET) is placed at the center of the SRAM device sandwiched by p-wells (nMOSFETs). The MOSFET channels are isolated by shallow trench isolation (STI). When a nucleus in the device undergoes a collision with a ballistic neutron, a nuclear spallation reaction, in which the nucleus breaks into

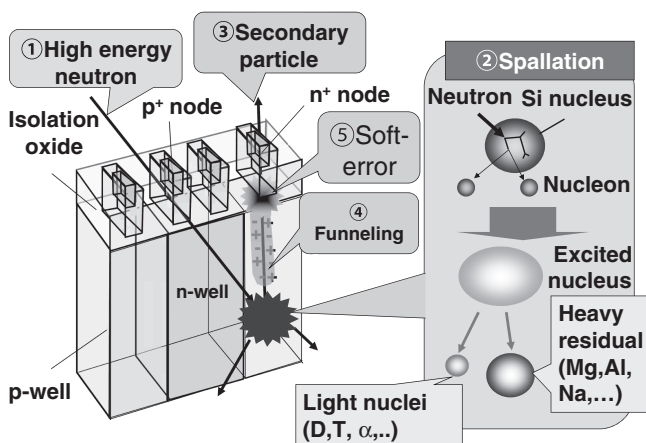


Fig. 2.3 Microscopic mechanism of neutron-induced soft-error in a SRAM bit. Secondary ions are produced by nuclear spallation reaction and soft-error takes place when enough amount of charge is collected to the n^+ storage node

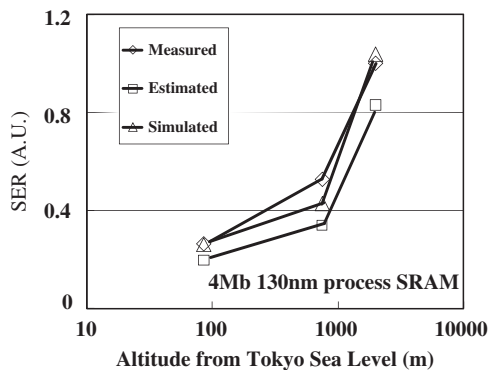
secondary fragments, can take place with a certain probability. Similar to alpha-ray soft-error, when the storage node (diffusion layer) is hit by a secondary ion, a certain amount of electrons/holes produced along the ion track are collected to the nodes, typically by the funneling mechanism [39] and/or the drift-diffusion process. An SEU takes place when charge collected to the node exceeds the critical charge Q_{crit} over which the data “1 (high)” in the node changes to “0 (low).”

2.3 Experimental Techniques to Quantify Soft-Error Rate (SER) and Their Standardization

2.3.1 The System to Quantify SER – SECIS

The SER evaluation techniques using high-energy particle accelerators are integrated as an SER evaluation system, self-consistent integrated system (SECIS for SER evaluation system) [40, 41], combined with field testing and measurements of environmental factors. SECIS consists of five closely interlinked key techniques: (i) field testing of typical devices, (ii) measurement of SEU cross-section as a function of neutron energy (E_n) using mainly quasi-mono-energetic neutron beams [40–44] along with a necessary correction using the numerical simulation package CORIMS (developed for nuclear spallation and charge collection physics in the device) [45], (iii) measurement of the terrestrial neutron spectrum at a specific location, (iv) measuring geographic coordinates and terrestrial neutron dose in the field, and (v) a numerical simulation by CORIMS of field testing and accelerator testing of memory devices [38]. The ultimate goal of this system is to evaluate SER of devices directly by the simulator CORIMS. It is expected that repetition of the procedure from (i) to (v) converges the evaluated value of SER obtained by SECIS with a high degree of accuracy. In order to confirm the usefulness of SECIS, a comparison among SER values obtained by field testing, accelerator testing, and simulation is carried out. Figure 2.4 demonstrates the series of the SER values of low power consumption CMOS SRAM with 180 nm process technology at three different locations

Fig. 2.4 Altitude dependency of field SER measured in three locations in Japan. Accuracies of estimated field SER with (quasi-)mono-energetic neutron method and simulated field SER with the simulator CORIMS are demonstrated (© 2002 IEEE)



in Japan at altitudes of 86, 755 and 1988 m. The simulation results obtained by using CORIMS are also shown [38].

2.3.2 Basic Method in JESD89A

2.3.2.1 Spallation Neutron Methods

First, define the neutron energy range E_{\min} and E_{\max} of the accelerator. In JESD89A, $E_{\min} = 10$ MeV and $E_{\max} =$ maximum energy of the spallation neutron source. Second, obtain the effective SEU cross-section based on the test results:

$$\sigma_{\text{seu}}^{\text{eff}} = \frac{N_{\text{err}}}{\int_{E_{\min}}^{E_{\max}} \frac{\partial \varphi}{\partial E_n} dE_n} \quad (2.1)$$

where N_{err} : number of errors in the OUT for total neutron irradiation and φ fluence for neutron energy range between E_n and $E_n + dE_n$.

Finally, estimate real-time SER (RTSER) from

$$\text{RTSER} = \sigma_{\text{SEU}}^{\text{eff}} \times \phi(E_{\min}, E_{\max}) \quad (2.2)$$

where $\phi(E_{\min}, E_{\max})$ flux of neutron with energy range between E_{\min} and E_{\max} at the sea level in NYC. $E_{\min} = 10$ MeV is recommended in JESD89A.

2.3.2.2 (Quasi-)Mono-Energetic Neutron Test

The quasi-mono-energetic neutron test is applied, where neutron beams with a flux peak at specific neutron energy are exemplified in Fig. 2.5. Some of the neutron spectra have plateaus in the lower energy range, which is called as “tail.” The SEU cross-section σ_{seu} for the peak flux contribution is defined and obtained by

$$\begin{aligned} \sigma_{\text{seu}} &= \frac{N_{\text{err}}^{\text{peak}}}{\Phi_{\text{peak}}} = \frac{R_{\text{err}}^{\text{peak}}}{\phi_{\text{peak}}} \\ &= \frac{N_{\text{err}}^{\text{peak}}}{\Phi_{\text{total}}} \times C_{\text{peak}} \end{aligned} \quad (2.3)$$

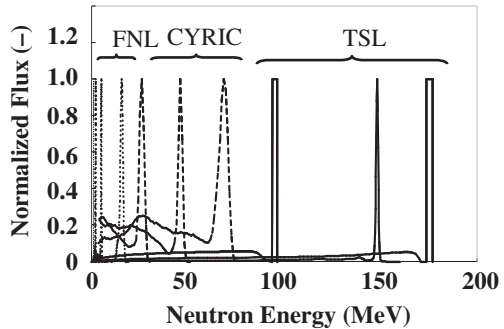
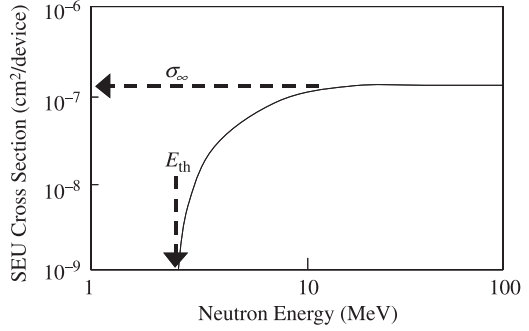


Fig. 2.5
Quasi-mono-energetic
neutron energy spectra in
various facilities (FNL,
CYRIC, and TSL)

Fig. 2.6 Typical conventional Weibull Fit curve



where $N_{\text{err}}^{\text{peak}}$: number of errors caused by neutrons in the peak flux area (errors); Φ_{peak} : fluence in the peak flux area (n/cm^2); $R_{\text{err}}^{\text{peak}}$: error rate caused by neutrons in the peak flux area (errors/h); ϕ_{peak} : flux in the peak flux area ($\text{n/cm}^2/\text{h}$); $N_{\text{err}}^{\text{total}}$: number of errors caused by total neutrons (errors); Φ_{total} total neutron fluence (n/cm^2); and C_{peak} : tail correction factor.

The tail correction factor eliminates the contribution of the tail to the total number of errors and can be obtained either by unfolding experimental data obtained for several (at least four) different energy peaks [42] or soft-error simulator CORIMS [41].

The SEU cross-section $\sigma_{\text{seu}}(E_n)$ is thus measured as a function of the neutron energy. The measured data are approximated by the Weibull Fit-type excitation function $\sigma_{\text{seu}}(E_n)$ as

$$\sigma_{\text{seu}}(E_n) = \sigma_{\infty} \left[1 - \exp \left\{ - \left(\frac{E_n - E_{\text{th}}}{W} \right)^S \right\} \right] \quad (2.4)$$

where σ_{∞} : saturation value of SEU cross-section (cm^2); E_n : neutron energy at the flux maximum (MeV); E_{th} : threshold energy (MeV); W : width factor (MeV); and S : shape factor (-).

Typical example of this type of excitation curve is described in Fig. 2.6. The curve starts from E_{th} and increases gradually to the saturation value σ_{∞} .

SER in any location on the Earth can be obtained from integration of the Weibull Fit and differential flux over the energy range from E_{th} .

$$\text{SER} = 10^9 \times \int_{E_{\text{th}}}^{\infty} \sigma_{\text{seu}}(E_n) \frac{\partial \phi(E_n)}{\partial E_n} dE_n \quad (2.5)$$

where SER: soft-error rate (FIT) and $\phi(E_n)$: neutron flux ($\text{n/cm}^2/\text{h}$).

Recently, extension of the Weibull Fit is found to be necessary and modified Weibull Fit (MWF) will be introduced in Section 2.7.

2.3.3 SEE Classification Techniques in Time Domain

Figure 2.7 shows the sequential test algorithm basically to classify the nature of SEU [16, 43]. One normal *write/read* cycle takes 8–9 s for all bits in a DUT. Two or more errors in the same sampling interval are basically regarded as MCU. Once the data in a certain bit is in an error, then the error classification algorithm is applied thereafter. If the data is recovered by re-reading, the error is regarded as a transient error. If the error is not a transient error, then compliment data is written to the bit in the phase II. If the bit is re-writable, then the error is regarded as “static soft error” part of which may be MCBI as discussed later or SEFI if it can be corrected by resetting. After all the bits are checked and if there are any error bits which are not re-writable or cannot be corrected by resetting, the DUT power is turned off and then turned on to see if the bit is re-writable in the phase III. If the bit is re-writable after power cycle, the errors are categorized as the “power cycle soft error” (PCSE) [6]. Non-destructive SEL may be among PCSE mode. If the errors cannot be corrected even by power cycle, then those errors may be classified as hard error (HE). I_{DD} current and device temperature are measured within a certain time interval independently.

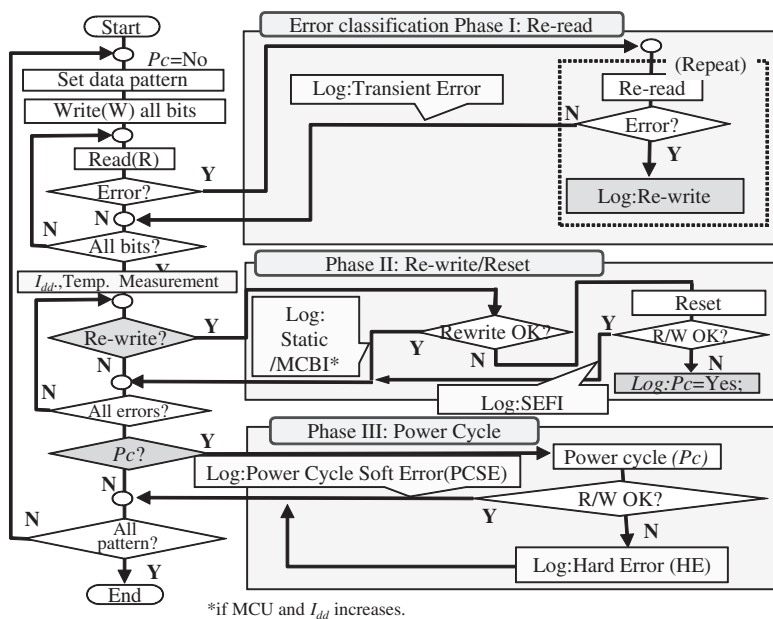


Fig. 2.7 Sequential classification algorithm of SEE in time domain (© 2006 IEEE)

2.3.4 MCU Classification Techniques in Topological Space Domain

A space-domain topological classification algorithm, which automatically identifies and classifies MCUs within a single sampling time window, is implemented in a specially designed program MUCEAC [43].

Figure 2.8 outlines the basic algorithms in MUCEAC. Any two errors within a certain distance along both BL and WL directions in the same time interval are regarded as contained in an MCU. If any two errors in different MCUs satisfy these criteria, the two MCUs make a single MCU. This procedure is continued until all the SEU/MCUs are isolated.

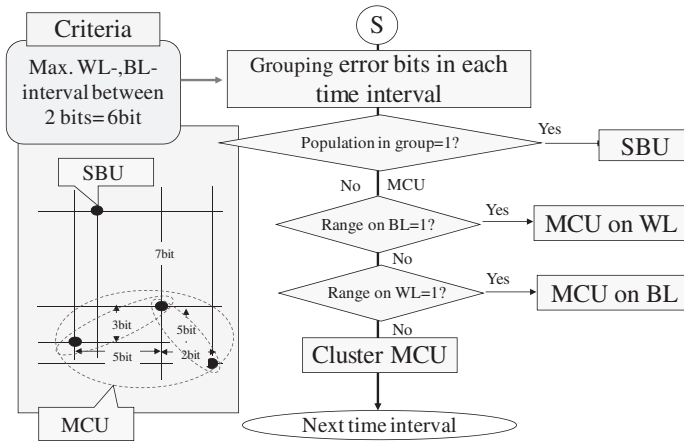


Fig. 2.8 Topological classification algorithm of MCU in space domain (© 2006 IEEE)

As proposed in the MCBI experimental analyses [16, 43], the following MCU classification rules are also applied in CORIMS:

- (1) MCU pattern is classified into three basic categories, like a single line along BL (category “b”), a single line along WL (category “w”), and cluster (an MCU that has two or more bits along both BL and WL directions; category “c”).
- (2) MCU code that can be almost uniquely relevant to physical address pattern in an MCU is given as:

$$C_N_1_N_2_N_3_N_4_P$$

where C: category (b/w/c); N_1 : MCU size(= $N_3 \times N_4$); N_2 : bit multiplicity in an MCU; N_3 : width in the BL direction (bits); N_4 : width in the WL direction (bits); and P: parity (A1: initial data in an MCU bits are all “1”; A0: initial data are all “0”; MX: initial data are a mixture of “0” and “1”).

Figure 2.9 depicts examples of MCU categories and codes. An MCU code can be almost uniquely assigned to a specific error bit pattern as far as MCU size is not so

Category	Code	Error bit pattern example
On single BL	B_2_2_2_1_ any parity	
On single WL	W_2_2_1_2_ any parity	
Cluster	C_4_2_2_2_ any parity	
	C_6_2_2_3_ any parity	
	C_6_2_3_2_ any parity	
	C_6_3_3_2_ any parity	
	C_8_2_4_2_ any parity	
	C_9_3_3_3_ any parity	

(A) MCBI for all
"1/0..." pattern
(B_10_10_10_1_A1)

 (B) MCBI for
checkerboard
pattern
(C_10_6_5_2_MX)

Fig. 2.9 Example of MCU codes and categories

large. MCU categories or codes can be very effective hints to identify the underlying mechanism. As for MCBI, all “high” (data “1”) nodes in the vicinity of the MCBI in the p-well fail so that very specific error bit patterns appear depending on the data pattern, (A) FF (all “1”) or (B) CHB, as illustrated in Fig. 2.9.

2.4 Evolution of Multi-node Upset Problem

Peculiar MCU mode was found in 130 nm 8 Mbit SRAM by 70 MeV quasi-mono-energetic neutron test in CYRIC [14] before its flux was intensified to world-top class in 2007 [44]. Most MCUs turned out to be two-bit MCUs in adjacent position along WL. More detailed study was carried out with 130 nm SRAMs in TSL. The new MCU mode was defined as multi-coupled bipolar interaction (MCBI) and threat of MNUs in logic devices due to MCBI was recognized.

2.4.1 MCU Characterization by Accelerator-Based Experiments

2.4.1.1 DUTs and Neutron Beams

For the irradiation test, 130-nm 16-Mbit SRAM is used. The layout and structure is schematically shown in Fig. 2.10. The test was carried out in Theodore Svedberg Laboratory (TSL) of Uppsala University [45] with neutron peak energies E_p of

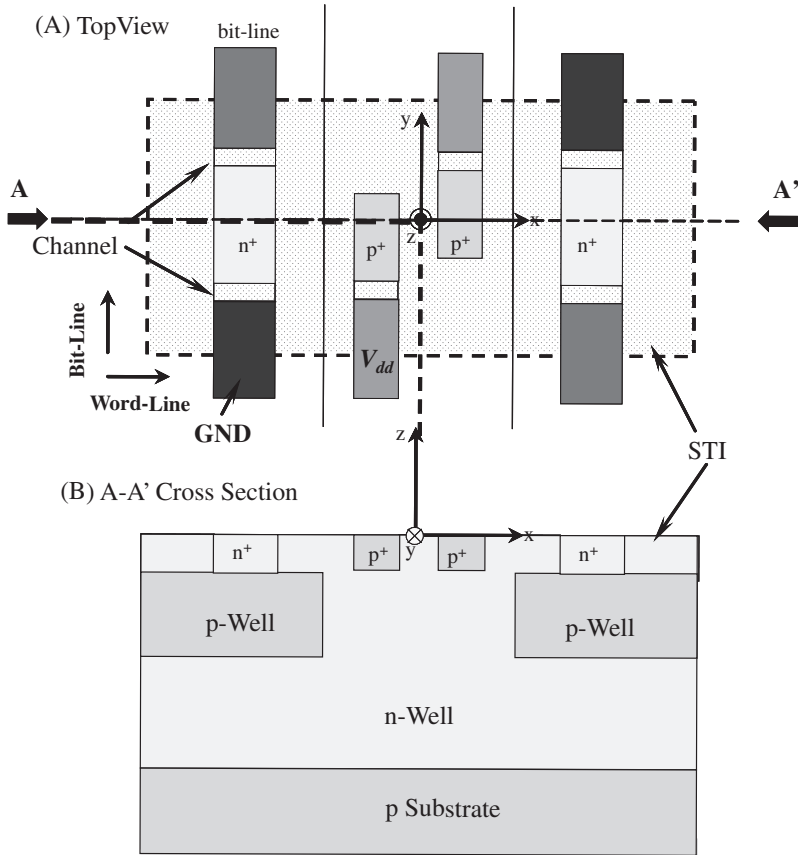


Fig. 2.10 Triple-well structure of the one-bit SRAM cell model (© 2005 IEEE)

21, 46, 96, and 176 MeV. Beam flux and energy peak in TSL are the highest so that better statistics is expected to be obtained with new MCU mode. The automatic data analysis sequences are applied in space and time domains as described in Section 2.3 [42].

2.4.1.2 MCU Patterns

Of MCUs 2564 were identified in total without any MBUs. All MCUs are found to be re-writable so that they are neither MCBI nor SEL. It was also found that all multiple errors along single word line were only two adjacent bits so that the new MCU mode cannot be any cause of failures by applying conventional interleaving with interval of three or more bits and ECC in memories. Based on topological analysis of MCUs, as partly exemplified in Fig. 2.9, the following implications are also obtained:

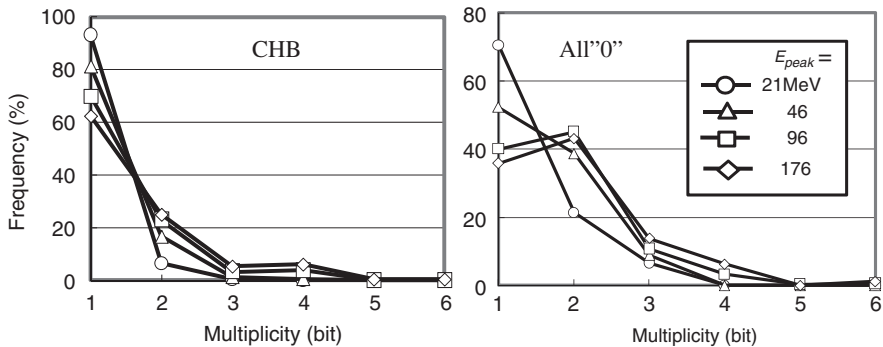


Fig. 2.11 Bit multiplicity of MCU in 130 nm SRAM measured at TSL (© 2006 IEEE)

- (1) For CHB/CHBc, MCU with two error bits aligns along with the word line (WL), as seen in (B) in Fig. 2.9.
- (2) As rare cases for CHB and CHBc, the clusters cover multi BLs and WLs.
- (3) For ALL0/ALL1, MCU normally makes a single successive straight line along BL, as seen in (A) in Fig. 2.9, which implies “high” nodes aligned in the same p-well are subject to fail. As many as 12 successive MCEs are observed at the maximum as in (A).
- (4) Likewise for CHB and CHBc, “high” nodes in p-well are subject to fail showing “leap-frog” cluster error bit pattern along a BL as triple leap-frog pattern in (B).

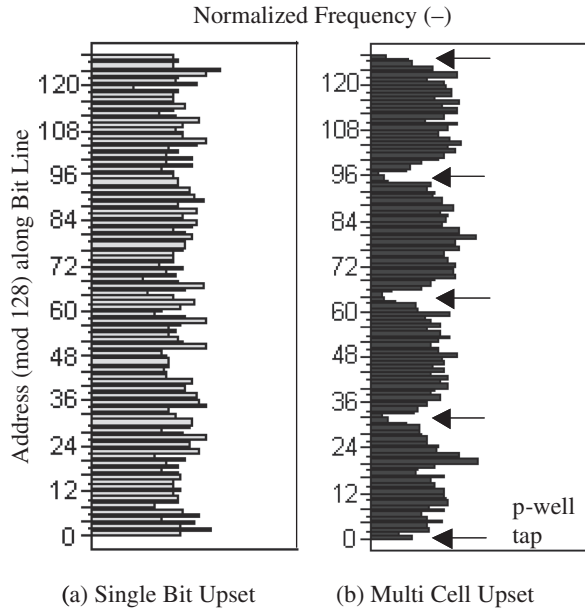
Figure 2.11 shows unnatural multiplicity observed in the test results. For all “0,” it is found that the number of double-bit error exceed those of single-bit error when the neutron energy becomes higher, while the trends for CHB seems rather normal. For CHB, there is a slight increase in quad-bit MCU, suggesting an increase in double leap-frog-type MCUs.

2.4.1.3 Influence of Tap Locations

Figure 2.12 shows error population of (a) single-bit upset (SBU) and (b) MCU errors along BL with modified address (Mod 128) to see the effects of tap locations [16]. Clear dependency with 32-bit intervals appears only on MCUs along BL direction, where tap for bias is located with 32-bit interval. This implies that

- (i) MCU probability is low at the 2–3-bit vicinity of the tap position, which implies that the resistance to the tap governs MCU.
- (ii) Major mechanism of MCUs is different from SBUs. For SBUs, major SEU mechanism may be attributed to charge collection–diffusion or simple snap-back mechanism, while that of MCUs must be related to bipolar action, where resistance between parasitic transistors and taps plays a major role.

Fig. 2.12 Distribution of SEUs along with bit line. Arrows indicate p-well tap locations where V_{SS} is supplied. (a) Single-bit upset (b) Multi-cell upset (© 2006 IEEE)



The other evidence indicating bipolar action is stepwise distribution of I_{DD} increase [16]. The number of discrete steps increases with the peak neutron energy and is believed to depend on the MCU bit-multiplicity.

2.4.1.4 MCU Category

Figure 2.13 shows the ratio of MCU categories as a function of neutron peak energy for CHB, CHBc, all “0” and all “1” data patterns. CHB and CHBc have almost the same trends, showing that MCU on WL is not changed so drastically with neutron energy, but MCU on BL decreases while cluster MCU increases. As for all “0” and all “1,” trends are also almost the same between two patterns. Almost all MCUs are MCUs on BL with a slight increase in cluster.

2.4.1.5 MCU Code

Figure 2.14 summarizes classification results by MCU code for MCUs of size 6 bits. It is seen that

- (i) Major codes for group A (CHB, CHBc) are C_&_3_3_2_MX and C_6_4_2_3_MX (correspond to double leap-frog patterns as shown in the left bottom of Fig. 3.14) and they increase as neutron energy increases.
- (ii) As for group B (all “0” and all “1”), no particular MCU code appears for the MCU size of 6 bits.

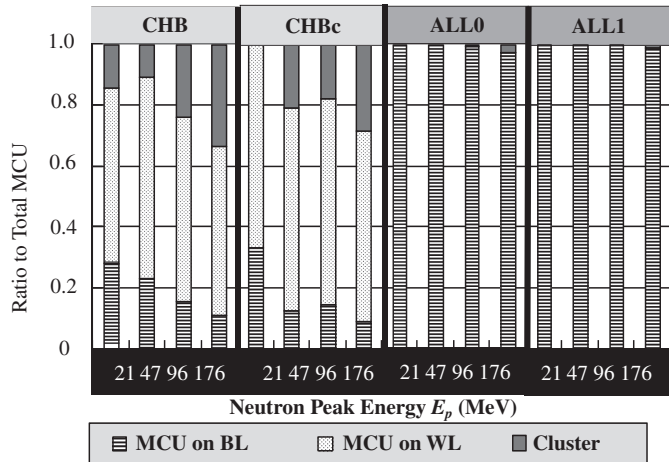


Fig. 2.13 Three categories identified in each run. For bars in each data pattern correspond to neutron energies of 21, 46, 96, 176 MeV, respectively, from left side (© 2006 IEEE)



Code	Data pattern							
	Group A				Group B			
	$E_p=$ 21	47	96	176	21	47	96	176
C_6_2_3_2_MX	1	1	1	2				
b_6_2_6_1_MX	1							
C_6_3_3_2_MX	1	15	49	77				
C_6_3_2_3_MX				2				
C_6_3_3_2_A0								1
C_6_3_3_2_A1								2
C_6_4_3_2_MX		7	57	100				
C_6_4_2_3_MX		1		3				
b_6_6_6_1_A0							1	2
b_6_6_6_1_A1								2
Typical Error pattern								
● (data = "1"), ○ (data = "0")	(C_6_4_3_2_MX)				(b_6_6_6_1_A1)			

Fig. 2.14 MCU code dependency in data pattern and neutron peak energy for group A (CHB) and group B (all 0)

2.4.2 Multi-coupled Bipolar Interaction (MCBI)

The error-bit pattern and IDD increase in the new MCU mode are clearly reproduced in multi-cell TCAD simulation and the mode is turned out to be parasitic thyristor effect triggered by single-event snapback in the p-well. The mechanism is

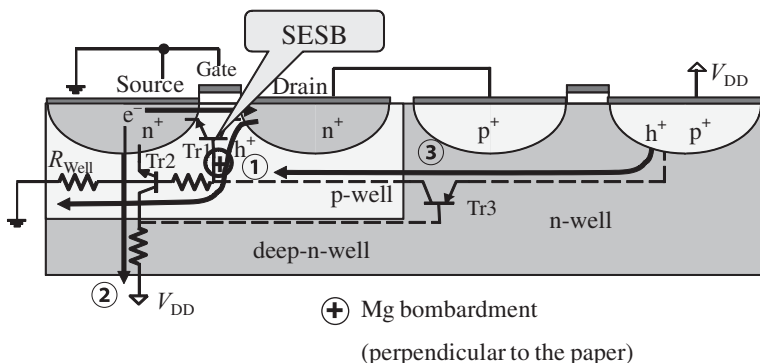


Fig. 2.15 Mechanism of MCBI (© 2005 IEEE)

illustrated in Fig. 2.15 [16]. When the secondary ion penetrates into pn-junctions surrounding the p-well, electrons produced in the ion track move outside the p-well, and the holes remain in the p-well to raise potential in the p-well and form a parasitic transistor Tr1. The potential increase turns on the transistor and high-state drain data flips. If holes continue to be supplied from the drain by impact ionization mechanism, high potential is kept to turn on the parasitic transistor Tr2. Electrons that flow into the deep *n*-isolation region reduces the potential in the *n*-region to turn on the parasitic transistor Tr3 to supply holes to the channel in Tr1, resulting in an increase in I_{DD} current. We call this mechanism multi-coupled bipolar interaction (MCBI). Figure 2.16 demonstrates that only MCBI can explain the MCU pattern

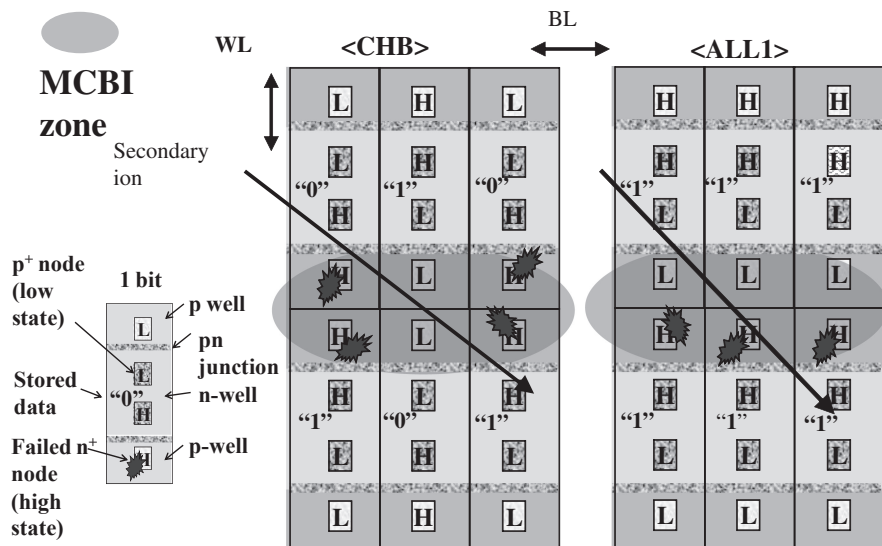


Fig. 2.16 Mechanism of error bit pattern dependency on data pattern

Table 2.1 Comparison of bipolar action mechanisms in CMOSFET device

Features	Single event latchup (SEL)	Multi-coupled bipolar interaction (MCBI)
Multiplicity	No limit over WL/BL direction (within peripheral circuit)	10–20 bits maximum mainly in one or adjacent well (s)
Correction method	Power cycle	Re-writing
I_{DD} current	High, 10–5 mA stepwise increase (2–3, three steps)	Low, 2–10 mA stepwise increase depending on multiplicity
Tap location dependency	High	High except for single bit upset
Mechanism	Direct switch-on of parasitic thyristor	Parasitic thyristor triggered by neutron-induced snapback

dependency on data pattern: p-wells are commonly owned by two adjacent memory cells. For CHB, two adjacent “high”-state storage nodes line up along WL with two-bit interval along BL. If a certain region in p-well is affected by MCBI, “high”-state storage nodes in the area flip to make leap-frog pattern. As for all “0” and all “1” data patterns, “high”-state nodes align continuously in one side of p-well to make a line of failed bit along BL.

Table 2.1 compares the features of bipolar actions, snapback, MCBI, and latchup. The biggest difference of MCBI from latchup is that MCBI is re-writable, neither destructive nor PCSE. Failures due to MCBI can be avoided by interleaving and ECC for memories. It has, however, potentially critical influences on the logic devices. MNU in logic gates can be caused by MCBI, resulting in failures in component/system with a number of logic gates.

2.5 Simulation Techniques for Neutron-Induced Soft Error

2.5.1 Overall Microscopic Soft-Error Model

In Fig. 2.3, a schematic of microscopic soft-error model for a SRAM cell is depicted. The SRAM has two n^+ nodes in the p-well and two p^+ storage nodes in the n-well. Two sets of adjacent n^+ and p^+ nodes correspond to two potential states “high” or “low.” The memory data “1” or “0” is assigned to the side (right or left) that has high potential. Once a ballistic neutron penetrates into the SRAM, nuclear spallation reaction may take place between the neutron and the nucleus (mostly Si) in the device. As a prompt reaction, nucleons (protons and neutrons) collide with each other in the nucleus. Some of the nucleons may escape from the nucleus when they have enough kinetic energies. This process is called as intra-nuclear cascade (INC) [46]. After this prompt process, light nuclei may be “evaporated” from the residual excited nucleus [47]. As a consequence, nucleons, light nuclei, and the residual nucleus run inside the SRAM cell producing electron-hole pairs along with the ion track. Energy necessary to produce one pair of electron and hole is 3.6 eV in Si.

When one of such secondary ions hit the storage nodes, some of the charges are collected to the storage node mainly through funneling effect [39] and drift/diffusion process. If the amount of charges exceeds the critical charge that can flip the logical state of the SRAM, a soft error takes place in the SRAM.

2.5.2 Nuclear Spallation Reaction Models

Monte Carlo single-event simulator, cosmic ray impact simulator (CORIMS) [14, 16, 36–38, 48], is equipped with numerical solutions for nuclear spallation reactions of silicon, ion track analysis in an infinite layout of memory cells in a semiconductor device, and charge collection to the diffusion layer of the device. The model of the nuclear spallation reaction is based on the intra-nuclear cascade (INC) model and the evaporation model by Weisskopf and Ewing. The INC model is applied to prompt collision process, where many-body collisions among nucleons (neutron and proton) are treated numerically as a cascade of relativistic binary collisions between two nucleons in the target nucleus. The evaporation model of light particles from excited nucleus is also applied for delayed nuclear reaction process, where nucleons (n and p), deuterons (^2H or D), tritons (^3H or T), helium and residual nucleus are released into the substrate. The inverse reaction cross-section necessary for determination of an evaporation channel (a set of evaporated light particle and residual nucleus) is calculated based on the GEM model [49]. Nucleus type, energy and direction of each secondary ion produced in a spallation reaction are thus determined and reaction locations are randomly set in the device model. The details of the nuclear reaction data are summarized elsewhere [38].

Accuracy of nuclear reaction model is validated through comparison of nuclear reaction data of high-energy proton and aluminum [50]. SER in the device under any neutron spectra can be simulated. In the case of simulation at a specific location at ground level on the Earth, the terrestrial neutron spectrum at the location is corrected in accordance with the geomagnetic latitude and the altitude based on the standard neutron spectrum at the sea level in New York City as shown in Fig. 2.2 [6].

Figure 2.17 shows an example of outputs from CORIMS for energy spectra of secondary ions produced directly from Si substrate with the neutron spectrum shown in Fig. 2.2. It is noteworthy that

- (i) Light particles such as proton and helium (or alpha particle) have high production rates and high energies up to a few hundreds to 1,000 MeV
- (ii) Heavier particles such as Mg and Al have also relatively high production rates but do not have high energies with maximum energies of 10–100 MeV.

2.5.3 Charge Deposition Model

Figure 2.18 shows calculated charge deposition density for the relevant ions based on the SRIM tables (<http://www.srim.org/>).

It is also noteworthy that

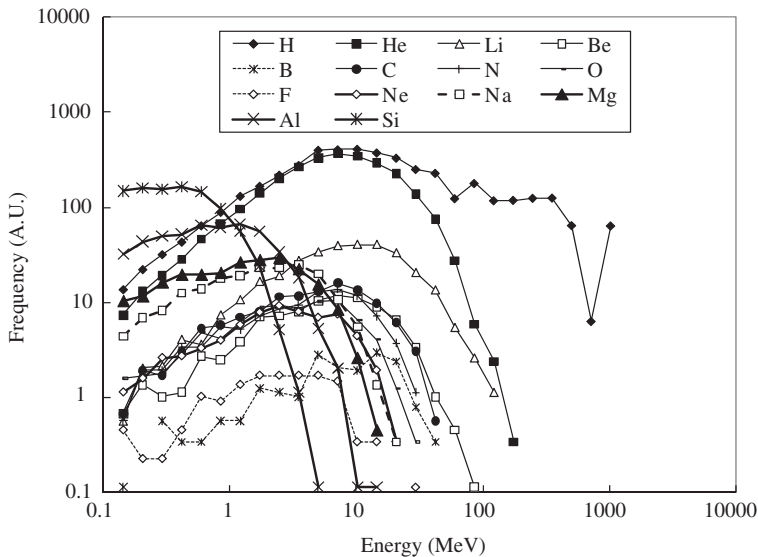


Fig. 2.17 Energy spectra of secondary ions produced from Si by neutron spallation reaction with neutron energy spectrum in NYC (© 2010 IEEE)

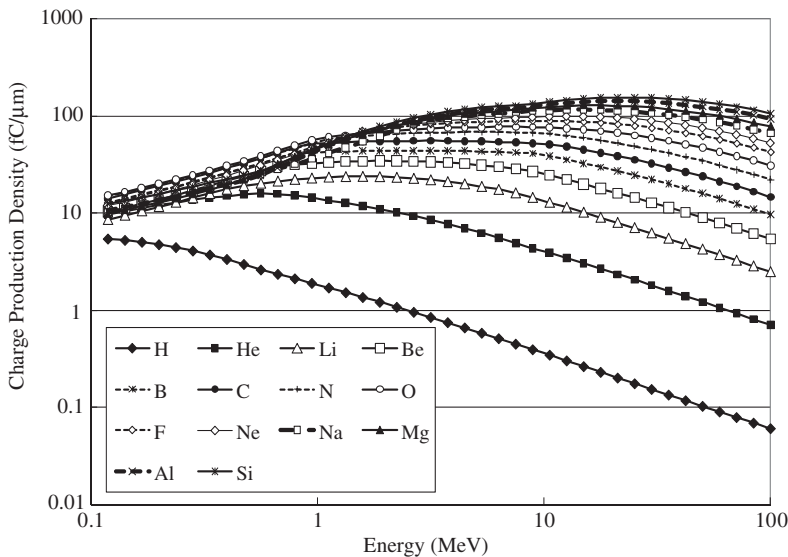


Fig. 2.18 Charge density spectra in Si of secondary ions as functions of energy (© 2010 IEEE)

(i) The charge production density by proton and alpha becomes lower when the energy is higher beyond 0.1–1 MeV. This implies that protons and alpha particles with high energy demonstrated do not have high contribution to soft error in SRAMs.

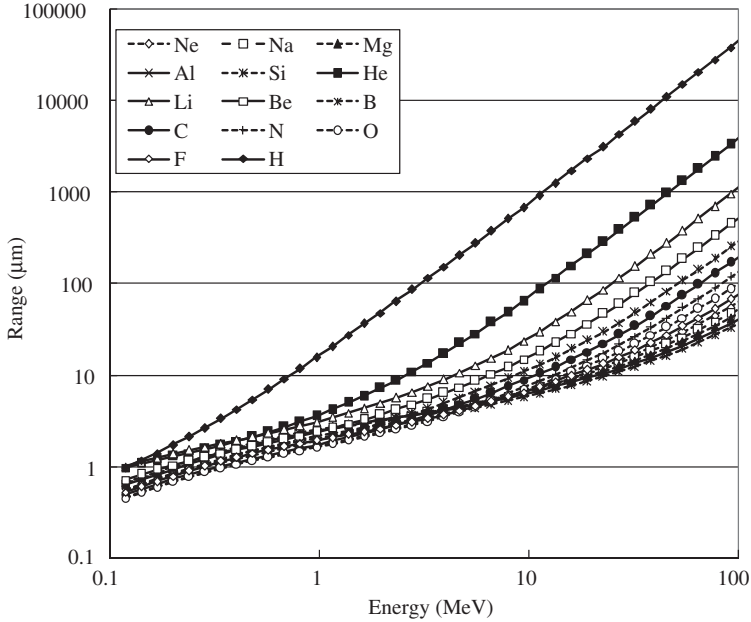


Fig. 2.19 Mean range of secondary ions in Si as functions of energy (© 2010 IEEE)

- (ii) The charge production density by heavier ions becomes larger when the ion energies increase in the relevant energy range.

Figure 2.19 shows the average range of ion as a function of kinetic energy also based on the SRIM tables.

It can be seen that

- (i) Light particles have as long range as 10–100 μm in Si substrate in the relevant energy range
- (ii) Heavier particles have much shorter ranges of 1–100 μm .

2.5.4 SRAM Device Model

The model layout of MOSFET SRAM cell is illustrated in Fig. 2.10. Since the active regions are isolated by STI oxide in lateral direction and wells line up across the word lines, charge collection in the lateral direction is tightly limited in the present device. Bits in a word are aligned along a word line so that MBUs in this device are tightly limited eventually. When an ion passes through the depletion layer under the storage node, the funneling model is applied to calculate the charge collected to the storage node. When the ion passes through the p–n junction at the bottom

of p-well, funneling also takes place so that the charge deposited in the p-well is distributed to the storage node and p-substrate below the p-well. The funneling effect becomes larger when the ion track runs along with the p-well (BL direction) because there is less probability that the ion passes through the other p-n junction in the p-well. Drift-diffusion layer of 100 nm thickness is assumed to be located under the storage node. When an ion passes through only the drift-diffusion layer, the amount of charges in the layer is assumed to be collected by the storage node. The charge deposited inside the storage node and oxide is assumed to recombine and not to contribute to soft error. Any 3-D device models, including SRAMs, can be constructed automatically from device layout data in GDS2 files [51] by using a specially designed tool. Ion tracks through components in a device are analyzed with the help of computer geometry techniques in CORIMS.

2.5.5 Cell Matrix Model

Naturally, a model with the fixed number of physical cell models may be applied to investigate MCU effects. Such a method, however, has inherent limitations on the memory and speed of the simulations. We have developed a dynamic cell-shift (DCS) method to overcome such limitations.

Figure 2.20 shows the basic idea of the dynamic cell-shift method. When an ion crosses a memory cell matrix along the line A–B–C–D, the track of the ion may be traced as long as the ion has a possibility to hit the sensitive components. This method requires a cell matrix that is wide enough compared to the ion range. The

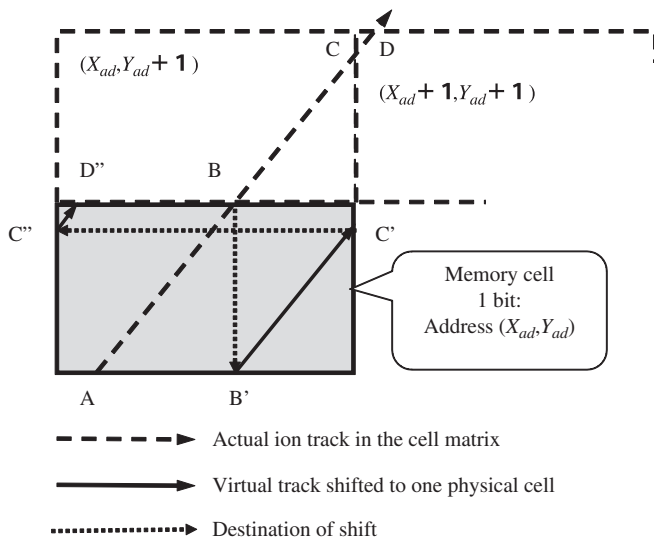


Fig. 2.20 Dynamic cell shift (DCS) method to track ion trajectory in the infinite cell matrix (© 2010 IEEE)

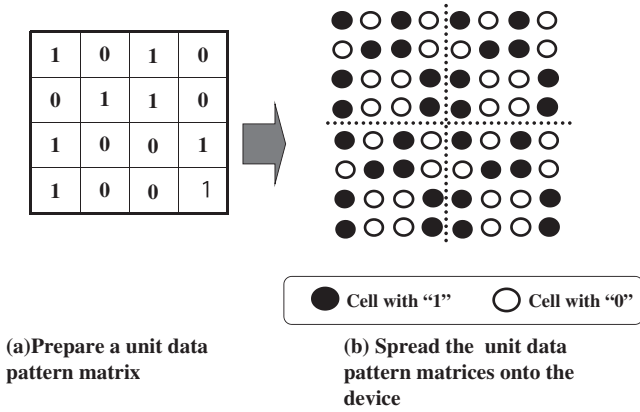


Fig. 2.21 Method to set any data pattern on the cell matrix

proposed method does not need an actual cell matrix. Instead, it utilizes only one physical cell model. When an ion reaches the boundary at B, for example, the track is virtually shifted to B'–C' by using a shift in the Y -coordinates and physical address of Y -direction Y_{ad} is incremented by 1 bit. Similarly, when the actual ion crosses C–D, virtual track is shifted to C'–D' and the physical addresses of X - and Y -directions are incremented by 1 bit from the original address. In this way, any ion track can be traced until it stops, regardless of the length of the ion's range. In the present device, the condition of data "1" or "0" corresponds to the position (left or right) of "high" node in one bit of SRAM and the layout of the SRAM is symmetry to its center, all "1" and all "0" have the same feature and susceptibility to neutron impacts.

To save the area penalty, some nodes connected to V_{DD} or V_{SS} are commonly shared between adjacent bits. In this case, the bit layout is folded symmetrically along the boundary between the two bits. This technique is sometimes called "mirroring." The DCS method implemented in CORIMS is applicable to this type of mirroring.

Any cyclic data pattern in a rectangular zone can be implemented in CORIMS. The basic idea is illustrated in Fig. 2.21. Once after the data "1" and/or "0" pattern is set in a unit rectangular zone, the unit is close-packed infinitely in the WL and BL directions. Interleaving effects with any bit layout in the same word can also be analyzed with CORIMS, which is desirable for ECC design.

2.5.6 Recycle Simulation Method

In extreme cases, CPU time may exceed several days. This makes parametric survey study difficult in wide scope. To cope with this problem, CORIMS saves the virtual single events with extremely low critical charge with a certain input conditions, and re-runs later to recycle them for parametric survey on the effects of different critical charge, data pattern, and interleaving within 1 h CPU time.

2.5.7 Validation of SRAM Model

SRAM models in CORIMS have been validated to have less than 20% variations from experimental data of 250–130 nm SRAMs in a wide variety of neutron fields like field tests [40] and accelerator tests in LANSCE [52], TSL [45] ,CYRIC [44], and FNL[53], as shown in Fig. 2.22. Figure 2.4 also demonstrates such an example of justification of 130-nm SRAM simulation with measured data in three locations with different altitudes in Japan [38].

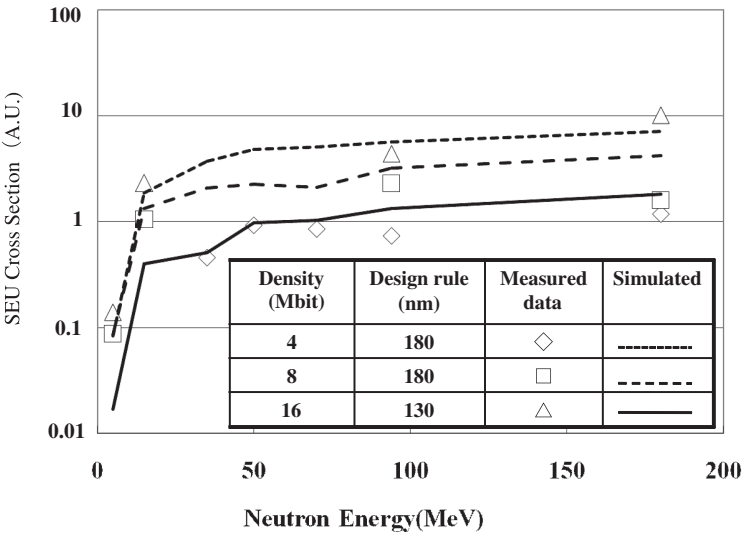


Fig. 2.22 Comparison of SEU cross-sections measured by (quasi-) monoenergetic neutron test and simulated by using CORIMS

2.6 Prediction for Scaling Effects Down to 22 nm Design Rule in SRAMs

2.6.1 Roadmap Assumption

Table 2.1 summarizes the typical roadmap parameters in 20–130 nm SRAM assumed based on ITRS2007 (<http://www.itrs.net/Links/2007ITRS/Home2007.htm>). Lateral two-dimensional scaling is assumed to reduce area by a factor of 2 by each generation. Depth profile is assumed to be constant due to lack in the roadmap information and also because of difficulty in making shallow profile. As parasitic capacitance is basically in proportion to device area, critical charge is also assumed to decrease by a factor of 2 by each generation. Although reduction in the supply voltage V_{DD} is preferable for reducing power consumption,

it is actually being limited in order to ensure enough margin from the upper bound of V_{th} variation [1] and, therefore, assumed to be constant. The critical charge will decrease more rapidly if the V_{DD} is reduced by generation, leading to increase in SER.

2.6.2 Results and Discussions

2.6.2.1 Overall Trends

Major simulation results are summarized in Tables 2.2 and 2.3 for data pattern of CB and all “1,” respectively. The maximum MCU size expands to the order of as many as million bits with the maximum MCU multiplicity of over 100 bits in 22–32 nm generations. The ratio of MCU to SEU will increase up to as high as about 50%. It is noteworthy that the maximum MCU size and multiplicity are statistically very rare case, showing only rough trends with generation (Table 2.4).

Table 2.2 Assumed roadmap of SRAM parameters

Design rule	SRAM property		
	Normalized cell area	Density	Normalized Q_{crit}
nm	AU	Mbit	AU
250	7.45	4	12.8
180	3.84	8	6.4
130	2.01	16	3.2
90	1.00	32	1.6
65	0.49	64	0.8
45	0.24	128	0.4
32	0.12	256	0.2
22	0.06	512	0.1

Source: (© 2010 IEEE)

Table 2.3 General trends obtained from simulation (CHB)

Design rule	Soft error rate			MCU maximum size	Maximum MCU multiplicity
			MCU ratio		
nm	Per device	Per Mbit	%	Bit	Bit
250	0.06	0.48	0	1	1
180	0.26	1.04	5.3	112	2
130	0.50	1.01	7	459	10
90	1.00	1.00	14.8	14,940	16
65	1.62	0.81	21.2	114,170	19
45	2.31	0.58	29.1	288,864	26
32	3.06	0.38	38.5	1932,765	52
22	3.53	0.22	46	463,638	175

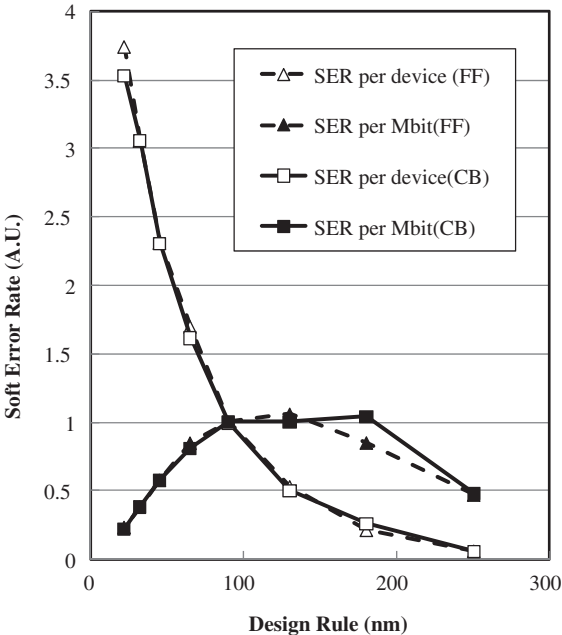
Source: (© 2010 IEEE)

Table 2.4 General trends obtained from simulation (All1)

Design rule	Soft error rate		MCU ratio	MCU maximum size	Maximum MCU multiplicity
	Per device	Per Mbit			
nm			%	Bit	Bit
250	0.06	0.47	0	1	1
180	0.21	0.85	3.6	5,472	4
130	0.53	1.06	6.6	396	4
90	1.00	1.00	12.2	8,096	11
65	1.70	0.85	18.4	31,860	29
45	2.31	0.58	27.8	84,525	27
32	3.06	0.38	34.7	77,216	39
22	3.75	0.23	44.7	3,659,296	87

Source: (© 2010 IEEE)

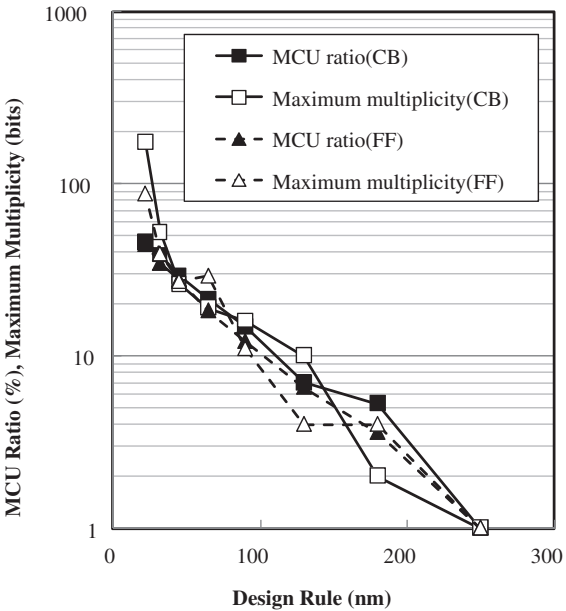
Fig. 2.23 Predicted trends in SER per device and Mbit (© 2010 IEEE)



Typical trends for SER/device and SER/Mbit are plotted for the data patterns CB and FF in Fig. 2.23. Trends in MCU ratio and the maximum MCU multiplicity are also plotted in Fig. 2.24 for the data patterns CB and FF. It is seen that

- (i) SER/Mbit increases drastically from 250 to 180 nm. This is quite consistent with the observation that SER in 4 Mbit SRAM increases drastically beyond

Fig. 2.24 Predicted trend in MCU ratio and maximum bit multiplicity in MCU (© 2010 IEEE)



- that in DRAMs, whose SERs have been problematic until late 1980s [38]. SER in SRAMs decreases mildly from 130 nm down to 22 nm. The decrease is also quite consistent with the recent experimental data [54].
- (ii) Although SER/Mbit decreases beyond 130 nm, SER/device increases by a factor of as much as 6–7 both for CB and all “1” due to an intense increase in density.
 - (iii) MCU ratio and multiplicity increase exponentially as scaling proceeds.
 - (iv) There are only minor differences between CB and FF data patterns.

Table 2.5 summarizes the trends in MCU categories for data patterns (A) CB and (B) FF. Typical MCU codes and the number of unique codes are also shown in the table. The figures in the cells are ratio to the total MCUs in percentage. Most MCU error patterns for MCU codes are shown before in Fig. 2.9. Some substantial differences can be seen between the data patterns:

- (i) The ratios of the category W (On single WL) for CB patterns are higher than those for FF patterns by a factor of about 2. This is due to the fact that two “high” nodes locate in the same p-well of two adjacent bits in WL direction for CB patterns so that two adjacent bits in WL direction are easily corrupted. This is also seen in the ratios of the MCU code W_2_2_1_2_any parity.
- (ii) The ratios of the code C_4_2_2_2_A1 for FF patterns are substantially higher than those for CB patterns.
- (iii) The differences between the ratios of categories seem to be clear for larger generations (180 and 130 nm). This has been clearly observed in our preceding

Table 2.5 Major predicted categories and MCU codes

(A) Data pattern CB	Design (nm)									
	250	180	130	90	65	45	32	22		
Total MCU even ^a										
Category										
	0	11	49	215	475	980	1,697	2,478		
On single BL (B)	0	36.4	12.2	16.7	16.1	14.7	12.0	10.8		
On single WL (W)	0	182	16.3	14.9	14.6	10.5	9.4	8.0		
Cluster (C)	0	45.5	71.4	68.4	69.2	74.8	78.6	81.2		
Code ^b										
C 4 2 2 2 A1	0	18.2	6.1	4.7	2.1	3.6	2.7	2.2		
C 4 2 2 2 A0	0	0.0	12.2	3.3	3.3	2.3	1.6	2.2		
B 2 2 1 MX	0	36.4	12.2	11.6	11.7	10.5	9.1	7.7		
C 6 2 3 2 MX	0	9.1	4.1	6.0	2.9	3.1	1.9	2.5		
W 2 2 1 2 MX	0	18.2	12.2	14.0	12.1	9.3	7.7	6.7		
C 12 2 4 3 MX	0	0.0	0.0	1.9	1.0	0.9	1.1	0.4		
C 6 2 3 MX	0	0.0	2.0	1.4	2.5	1.6	1.5	1.3		
Number of unique codes	1	8	30	107	243	483	917	1457		
(B) Data pattern FF	Design (nm)									
	250	180	130	90	65	45	32	22		
Total MCU even ^a										
Category										
	0	10	49	177	436	932	1,526	2,554		
On single BL (B)	0	30.0	22.4	11.3	11.9	9.8	9.4	7.6		
On single WL (W)	0	0.0	12.2	11.3	8.0	4.5	5.2	5.3		
Cluster (C)	0	70.0	65.3	77.4	80.0	85.7	85.4	87.0		
Code ^b										
C 4 2 2 2 A1	0	0.0	18.4	7.3	11.7	9.4	7.5	6.0		
C 8 2 4 2 A1	0	0.0	0.0	3.4	2.1	1.7	1.2	1.8		
B 2 2 1 A1	0	20.0	14.3	7.3	7.3	6.3	6.3	5.3		
C 6 2 3 A1	0	10.0	8.2	5.6	7.1	4.8	5.1	4.1		
W 2 2 1 2 A1	0	0.0	8.2	9.6	6.0	3.2	3.7	3.5		
C 9 3 3 A1	0	0.0	4.1	2.3	0.5	2.5	1.0	1.1		
C 6 2 3 A1	0	0.0	2.0	2.8	2.3	1.7	2.7	1.3		
Number of unique codes	1	8	27	96	220	508	837	1,440		

^a Total number of neutrons reacted: 58,003
^b Code = Category(Initial)_MCU size_Multiplicity_BL width_WL width_Parity of initial data (A0:all"0", A1:all"1", MX:mixture)
Source: (© 2010 IEEE)

work for 180 nm SRAMs [14]. The differences are getting unclear for smaller generations. This may be due to the fact that the SRAM cells are easily corrupted by the charge deposited only in the depletion layer as the critical charge becomes smaller and the memory cells are more tightly packed in the smaller generations. The directional effects become weak for smaller generation, since the contribution from charge collection by the directional funneling effects as mentioned before becomes smaller.

The result that MCU ratio drastically increases as scaling proceeds means that multi-node upset (MNU) in which multiple logical nodes of sequential or combinational logic device are corrupted must increase as well. This may cause serious impacts in reliability design of logic devices, since MNUs would make error detection impossible. This would make the redundancy SER mitigation techniques extremely vulnerable to MNU.

2.6.2.2 Charge Deposition Density for Secondary Ions

The frequencies of charge deposition density per unit track length at the boundary of the storage node by secondary ions are shown in Fig. 2.25 for proton, alpha particle, heavier particles (atomic number is 10 or more) and total particles. Basically, there are no differences in the shape of spectra with generation, with the maximum deposition density of about $110 \text{ fC}/\mu\text{m}$. This means that any device which can tolerate the density of $110 \text{ fC}/\mu\text{m}$ can be perfectly soft-error immune. Heavy ions cause high density ($10\text{--}110 \text{ fC}/\mu\text{m}$) charge deposition but their frequencies are relatively

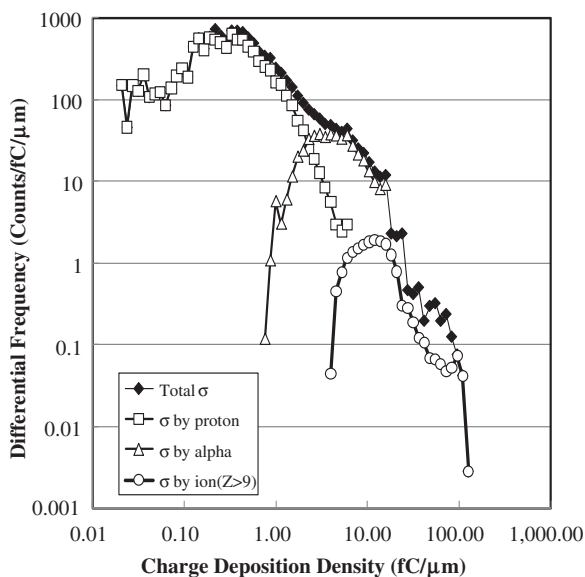


Fig. 2.25 Charge deposition density spectra when secondary ions penetrate the storage node (© 2010 IEEE)

low. Lighter particles (proton and alpha particle) play major roles for the deposition density below 10 fC/ μ m.

2.6.2.3 Total Charge Collected to Storage Node

Figure 2.26 shows the spectra of the total charge collected to the storage nodes for 22 and 130 nm SRAMs. When the collected charge excess the critical charge, SER takes places. In contrast to the charge deposition density, there are differences among different generations. The maximum collected charge decreases from 130 nm SRAM (36 fC) to 22 nm SRAM (20 fC), though the difference may not be so significant (16 fC).

In contrast, the soft-error susceptibility improves only slightly when the critical charge increases from 5 fC to 10 fC for 130 nm, but the change in the critical charge of 1 \rightarrow 2 \rightarrow 4 \rightarrow 10 fC improves the susceptibility by one order of magnitude for each step for 22 nm SRAM, since protons and alpha particles play major role when the critical charge is relatively low. The range in the collected charge becomes lower as scaling proceeds.

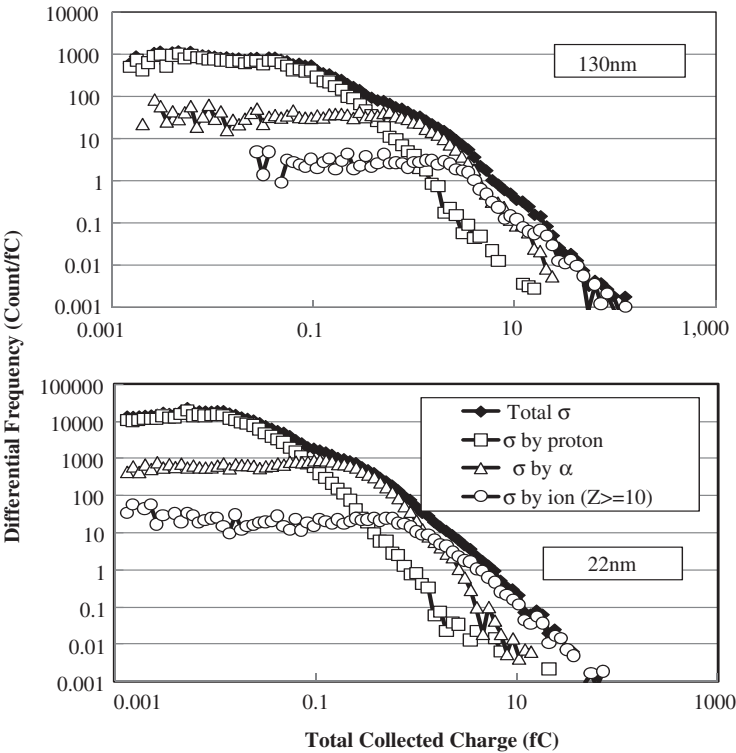


Fig. 2.26 Total collected charge spectra for 130 and 22 nm process SRAM (© 2010 IEEE)

2.6.2.4 Failed Bit Map (FBM)

Figure 2.27 shows the distribution of total failed bit map in the BL (perpendicular axis) and WL (vertical axis) address space when about 58,000 nuclear reactions take place in the four bits near the origin for the data pattern CB. It is seen that the area densely affected drastically increases from 130 nm (about 50×50 bits) to 22 nm (about 500×500). The automatic MCU classification tool, MUCEAC, has been introduced to make the statistic calculations from a number of MCUs and demonstrated for mainly 130 nm SRAM test results [16]. The extremely widened range of FBMs, however, would make the statistic calculations for MCU in neutron accelerated testing for 45–22 nm SRAM very painful or almost impossible task unless any ultra-high-speed automatic classification tool is developed.

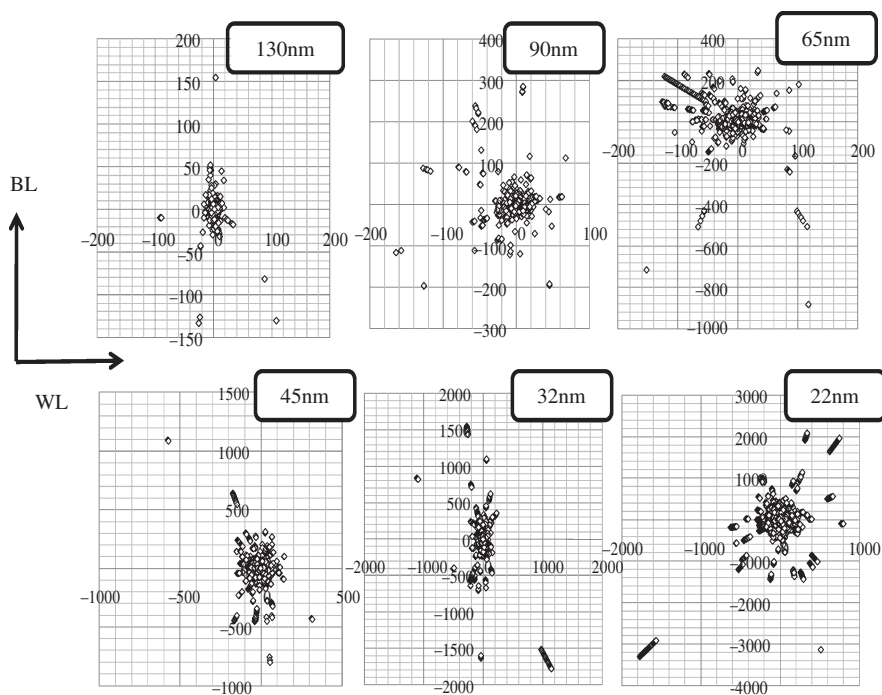


Fig. 2.27 Failed bit map for 58,000 nuclear spallation reaction with NYC sea level neutron spectrum from 130 nm SRAM to 22 nm SRAM (© 2010 IEEE)

2.6.2.5 Energy Dependency of SEU/MCU Cross-Section

SEU and MCU cross-sections for each generation are shown as a function of neutron energy in Figs. 2.28 and 2.29, respectively.

As scaling proceeds, the contribution of neutrons with energy lower than 10 MeV drastically increases due to increase in contribution of lighter particles as scaling

Fig. 2.28 Change in SEU cross-section curves from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE)

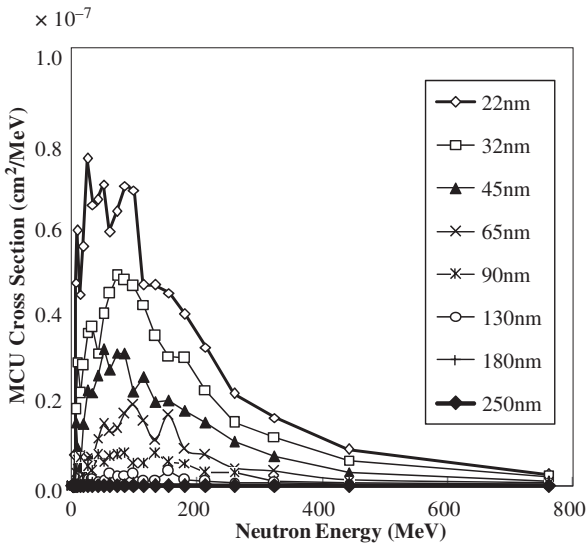
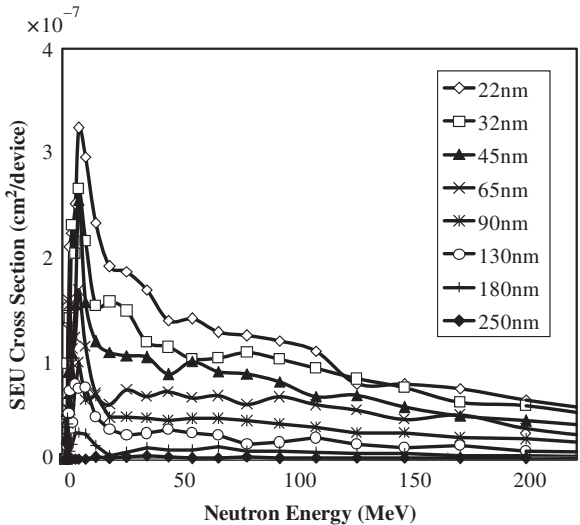
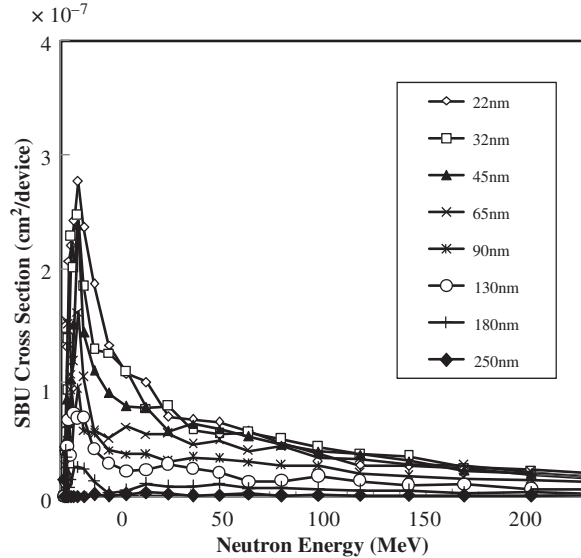


Fig. 2.29 Change in MCU cross-section curves from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE)

proceeds. Recent experimental results with low-energy protons showed quite consistent trends with the predicted trends, where SEU cross-section has sharp peak for protons with energies lower than 10 MeV [57, 58]. This implies that two essential changes may be needed in the standard methods including JESD89A to estimate SER from accelerator-based testing, namely

Fig. 2.30 Change in SBU cross-section curves from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE)



- (1) to include the contribution of neutrons with energy lower than 10 MeV to avoid large error in SER estimation when the spallation neutron sources are used;
- (2) the ordinary excitation function with saturated cross-section should be modified to have a sharp peak at low neutron energy when the (quasi-) mono-energetic neutron sources are used.

In contrast, there are no essential changes in MCU cross-section shapes. This can be understood from the fact that the contribution of lighter particle to MCU is relatively low. Instead, the sharp peak is understood to originate from single-bit upset (SBU) as shown in Fig. 2.30. The cross-section curve for SBU can be obtained by subtraction of MCU cross-section in Fig. 2.29 from the SEU cross-section in Fig. 2.28.

2.6.2.6 Trends in MCU Ratio

Figure 2.31 shows the trends in MCU ratio to the total SEU. The ratio generally increases as neutron energy increases and scaling proceeds. When the neutron energy increases, heavy ions with higher energy are produced, flipping multiple memory cells. If the memory cells are packed more densely, the number of flipped MCU bits is naturally increased. The maximum ratio exceeds as high as 0.5 for 22 nm SRAM, indicating the MCU and MNU impacts become more serious.

2.6.2.7 Trends in MCU Multiplicity Distribution

Figure 2.32 shows the changes in MCU multiplicity distributions. It is seen that the multiplicity shifts to larger number of bits as scaling proceeds. The ratios of SBU

Fig. 2.31 Change in MCU ratio as a function of neutron energy from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE)

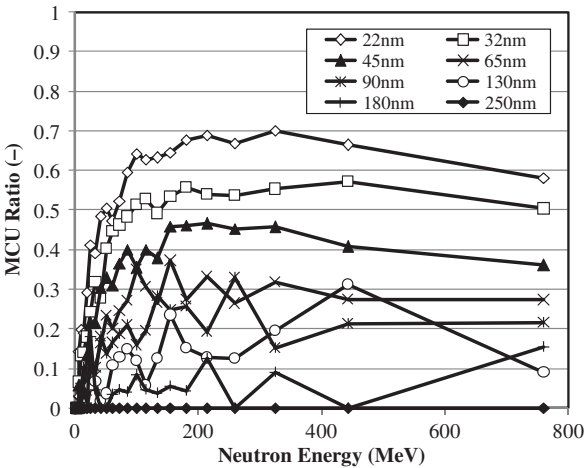
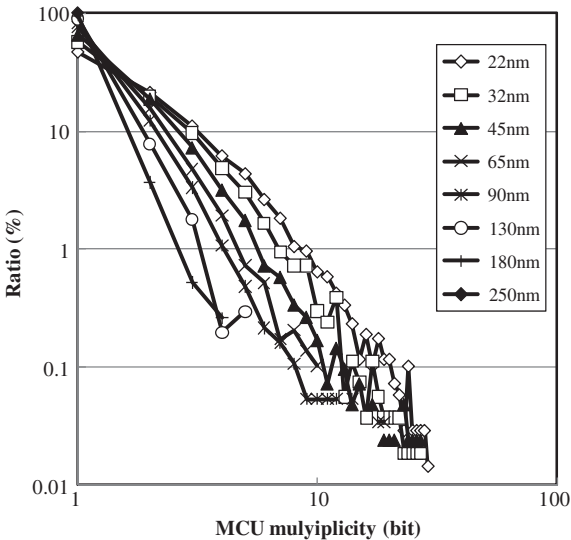


Fig. 2.32 Change in MCU bit multiplicity from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE)



and lower multiplicity MCUs reduce correspondingly. The maximum multiplicity is well beyond tens of bits when scaling proceeds beyond 32 nm as mentioned before.

2.6.3 Validity of Simulated Results

In the present model, the depth profile of impurities and the maximum funneling length are fixed for all generation. But in reality, depth profile will be shallower and funneling length will also be shorter as concentration of impurities become higher.

These effects would work for suppressing SER. On the other hand, operation voltage may be reduced in reality as scaling proceeds. This works for worsening SER.

Change in the material in the device would make wider variation in the prediction. If the high- k material is used for gate oxide like HfO_2 , the critical charge is increased to result in lower SER. Meanwhile, if the low- k material is used for inter-layer oxide, parasitic capacitance is reduced, resulting in lower critical charge and higher SER.

The bipolar effects, which are not implemented in CORIMS at present, are somewhat in the trade-off relationship with the charge collection mode. When the operation voltage is reduced, the bipolar mode would decrease. When p-well size is shrunk, charge collection mode would be minor but bipolar mode would be activated due to shrinkage of distance of p-n junctions. Even when the bipolar effects are implemented into the CORIMS model, the total trends may not differ so significantly. This point will be more clearly shown in the future work.

2.7 SER Estimation in Devices/Components/System

2.7.1 Standards for SER Measurement for Memories

Reliability of CMOS devices are being impaired by environmental radiation sources such as alpha-ray emitting impurities in device packages and terrestrial high-energy neutrons. In late 1990s, terrestrial neutron-induced soft error in SRAMs has become one of the major concerns in reliability issues, overwhelming concerns in DRAM soft errors and alpha-ray-induced soft-errors [5]. In around 2000, data corruption in SRAMs in network components has emerged as serious threats for network reliability [55, 56]. Establishing standard testing methods was urgent for the device vendors and users to make databases for reliable design. JESD89 has been established in 2002 in order to fulfill this requirements based on in-depth discussions among experts in relevant fields. JESD89A [6] has been issued in 2003 as the revised version of JESD89, in which alpha-ray, thermal neutron [57], spallation neutron [52, 58–61], (quasi-mono) energetic neutron [44, 45, 53], and high-altitude/underground field tests [41, 62–66] are described in a more reasonable way compared to the original JESD89. SERs in logic devices and field programmable gate arrays (FPGAs) were discussed to a certain degree but test methods were not defined.

As the devices scaled down below 130–90 nm, concerns in alpha-ray-induced soft errors are rebooted mainly due to decrease in the critical charge Q_{crit} . Evidences in SERs in logic devices such as peripheral circuits in DRAMs are emerging as well.

2.7.2 Revisions Needed for the Standards

Recent works [36, 37, 67–71] show that SEU cross-section has high peak below 10 MeV due to secondary low-energy protons and the peak height continues to be higher as devices scale down. Such examples in a simulation work are shown in

Fig. 2.33 Example of simulated excitation function of the 90 nm SRAM and fitted curve with sum of two (for proton and heavier ions) modified Weibull Fit curves

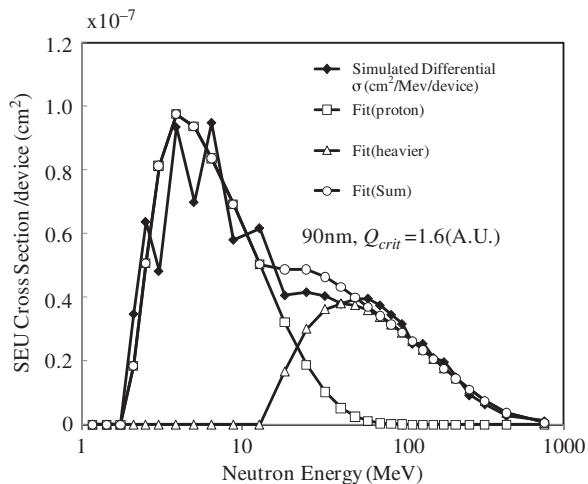


Fig. 2.33 [36, 37]. Compared to the shape of excitation function shown in Fig. 2.6, obvious large peaks appeared in the energy range below 10 MeV. Two peaks correspond to proton and alpha contributions that emerged from nuclear spallation reaction of neutron and silicon nucleus. It is seen that the peak heights get higher and threshold energies get lower as feature size becomes smaller, mainly due to decrease in the critical charge. E_{\min} less than 10 MeV should be used in Eqs. (2.1) and (2.2) for devices with design rule smaller than 90 nm. The validation for the reason why the range is applicable has to be shown quantitatively. The range may differ depending on the combination of the object under test (OUT) and spallation neutron sources.

In quasi-mono-energetic test, approximation function of excitation function in Eq. (2.4) must be changed. The following function may be applied:

$$\sigma_{\text{SEU}}(E_n) = \sigma_{\infty} \exp(-\lambda E_n) \left[1 - \exp \left\{ \left(\frac{E_n - E_{\text{th}}}{W} \right)^s \right\} \right] \quad (2.6)$$

where λ is a decay constant (1/MeV).

Equation (2.4) in JESD89A is the simplest case with $\lambda = 0$. As shown in Fig. 2.33, two or more curves are recommended to fit proton/alpha and heavier secondary ion contributions. Sum of those curves can give overall excitation function. The excitation function may be given in the style of a look-up table also.

Logic gates (inverters, AND, OR, NOR, adder, ...) chain as shown in Fig. 2.34 with FFs in-between irradiated in neutron field can be used to obtain raw SERs in combinational and sequential logic gates [23–26]. Raw SER can be obtained after corrections for masking effects and errors in FF themselves are made.

Current major stream in the system SER evaluation focuses on the masking effects to obtain mean system SER value accurately [72].

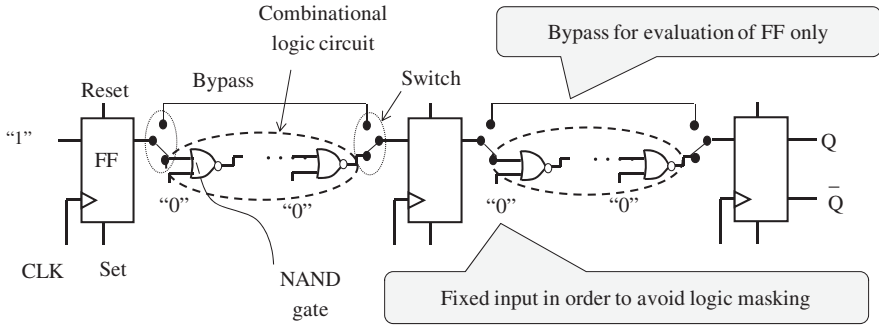


Fig. 2.34 Chain of NAND gates with FFs in-between to measure gate-level SER in NAND and FFs. By-pass is used by switching to measure SER in FF only

2.7.3 Quantification of SER in Logic Devices and Related Issues

Quantification in the chip-level SER evaluation may start with total raw SER of the system as expressed in Eq. (2.7):

$$SER_{UB} = \sum_j (SER_j^G \times N_j^G) + \sum_i (SER_i^M \times N_i^M) \quad (2.7)$$

where SER_j^G : SER of a j th gate; N_j^G : number of j th gates; SER_i^M : SER of a i th memory and N_i^M : number of i th memories.

Contribution of combinational (inverters, AND, OR, NOR, adder, ...) and sequential (FF and latch) logic gates to the chip-level SER can be twofold: (a) direct incidence sequential gates from inside, clock or set/reset channel and (b) indirect incidence from input as indicated in Fig. 2.35. As for indirect incidence, SET noise may not be latched to the flip/flops due to three masking mechanisms such as window (timing), logic, and electric masking. Electric masking refers decay effect of pulse height by which the logical state of SET pulse is changed. Window masking refers non-active duration of FF input relevant to clock timing and clock

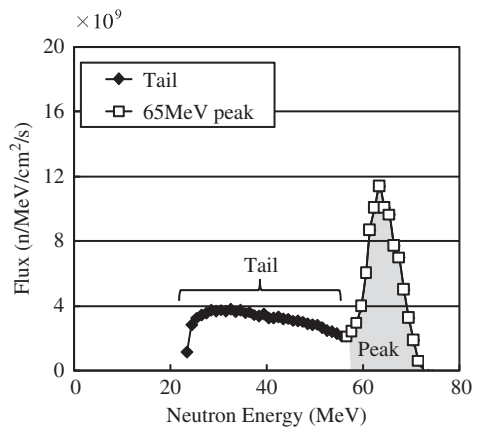


Fig. 2.35 Neutron spectrum used for the partial irradiation test in CYRIC. Peak flux is obtained at about 65 MeV
(© 2010 IEEE)

width. Logical masking refers the effect of priority input in multi-input gate, by which SET pulse is disregarded.

- (1) Methods to measure SER_j^M are almost established as in [6]. Some further development may be needed for MCU or bipolar effects except for the usage of MWF.
- (2) Methods to measure SER_j^G have not been fully established, but logic gates chain methods, as typically shown in Fig. 2.34, are gaining popularity and seem attractive. The chain with FFs connected in-between can be used to obtain raw SERs in combinational and sequential logic gates. Usually, tremendous types of gates are implemented in a ULSI chip so that obtaining all SER_j^G by irradiation experiments is inevitably impossible. Instead, simulation tools like CORIMS validated in field can be used to evaluate SER_j^G .
- (3) Quantification and mitigation methods for global control lines (clocks, SET/REST). In gate chain tests, dual-interlocked cell (DICE) is used assuming SER immune FFs. But this is not true at present. Some mitigation techniques are proposed for DICE-type FFs as mentioned before.
- (4) More direct quantification by chip/board-level irradiation tests are also pursued [73–76]. An example of this type of test is described in Section 2.9. This method is quite straightforward, but time and cost consumption cannot be avoided. Some effective guidelines are needed for this type of tests to generalize the test results.

2.8 An Example of Chip/Board-Level SER Measurement and Architectural Mitigation Techniques

2.8.1 SER Test Procedures for Network Components

2.8.1.1 Full and Partial Board Irradiation Test

System-level neutron irradiation test was proposed first by Ibe et al. in 2005 [77] in order to identify problematic system first and then problematic components in the system. Full-chip irradiation test has been done with microprocessors, servers, and routers [73–75]. Partial board irradiation test for routers is first carried out by Shimbo et al. [76].

Merits and demerits are summarized in Table 2.6 for partial and full-board irradiation tests, respectively.

Table 2.6 Merits and demerits of full and partial board irradiation

	Full board irradiation	Partial board irradiation
Merit	-Can simulate natural terrestrial neutron radiation environments	-Can pinpoint susceptible components
Demerit	-Difficult to pinpoint susceptible components -Wide neutron beam is required	-Test results for the components may vary from the full board irradiation test

2.8.1.2 Neutron Facility

The quasi-mono-energetic neutron facility at CYRIC (cyclotron radio-isotope center) of Tohoku University [44] was utilized for the irradiation tests with neutron peak energy of 65 MeV. The neutron energy spectrum is shown in Fig. 2.35. Tail and peak parts are indicated in the figure. Neutron beams with other energy peaks are not utilized due to limit of machine time. The parameters summarized in Table 2.7 for the Weibull Fit are estimated from the 130 nm generation SRAM experimental data measured at neutron energies 1, 2, 5, 15 MeV in FNL [45], 30, 65 MeV in CYRIC [44], and 95, 170 MeV in TSL [54]. σ_{∞} is fixed so that the Weibull Fit curve goes through the measured SEU cross-section at 65 MeV. Error in estimated SER due to this simplified procedure will be evaluated in Section 2.8.2.3. Figure 2.36 shows a schematic of irradiation room connected to the No. 3 TR 32 line. High-energy protons are bombarded to thin Li target from which neutron in the Li nuclei with almost same energy as the protons are evolved. Neutron beams are collimated by the concrete collimator into 10 cm \times 10 cm square cross-section.

Figure 2.37 illustrates the layout of the test equipment. The board under test (BUT) is set up perpendicular to the neutron beam whose center is at 125 cm high from the floor surface and 40 cm apart from the aperture of the neutron collimator.

Table 2.7 Parameters used for conventional Weibull Fit and their possible ranges

Weibull Fit parameter	This study	Minimum	Maximum
σ_{∞}	Fitted to 65 MeV data	\leftarrow	\leftarrow
E_{th}	2	1	5
W	18.9	10	20
S	1.4	1	2

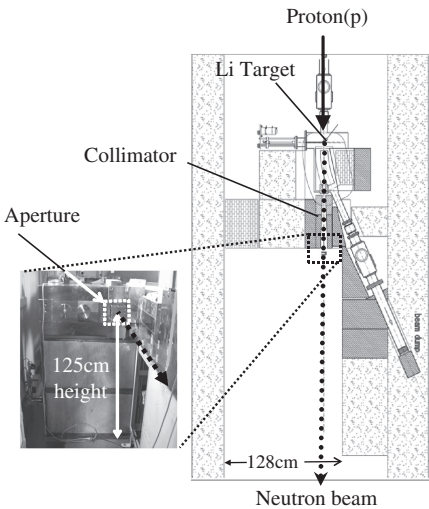


Fig. 2.36 Layout of irradiation room and a photograph of neutron beam aperture (© 2010 IEEE)

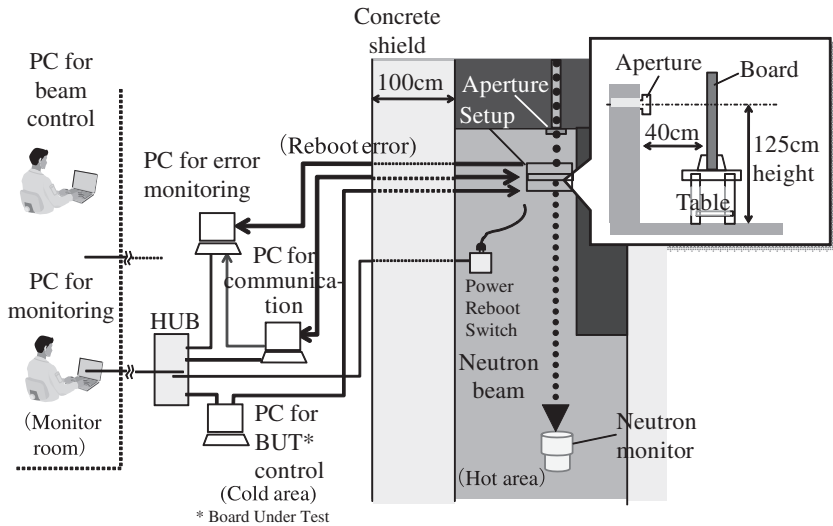


Fig. 2.37 Board setup and conceptual layout of experimental components (© 2010 IEEE)

The position of the table on which the BUT is set up is changed according to the part to be irradiated.

The failures are monitored with a PC placed in the cold (no neutrons) area just outside of 100 cm thick concrete wall. PCs for communication and BUT control are also placed in the same area. The signals from these PCs are connected to an Ethernet hub and monitored in the air-conditioned monitor room. A power rebooting switch is placed apart from neutron beam center and covered by Pb blocks in the irradiation room so as to minimize the influence on the switch from neutrons.

2.8.1.3 Architecture of Test Component

An FPGA chip, a CPU chip, and memory (SRAMs and SRAMs partially replaced by DRAMs) chip are chosen as partial irradiation parts on the board because they are believed to be the most vulnerable parts to neutron-induced soft error which can be recognized as system rebooting. The mechanisms of rebooting through stack, bus stack, and parity error are illustrated in Fig. 2.38.

Layout of parts in the board is shown in Fig. 2.39. The neutron beam areas for three chips are also shown in Fig. 2.39. Figure 2.40 shows the front view of the casing (430 mm high \times 700 mm width \times 40 mm thickness) where the main board (285 mm height \times 400 mm width) is located. Two types (sets A and B) of memory architectures are prepared as shown in Fig. 2.40. The CPU consists of 16 micro engines (MEs). Each ME contains an ME core and 32 KB internal memory. Part of SRAMs (10 MB) is not irradiated because of layout limit.

Fig. 2.38 Selection of critical components and mechanisms that cause rebooting the BUT (© 2010 IEEE)

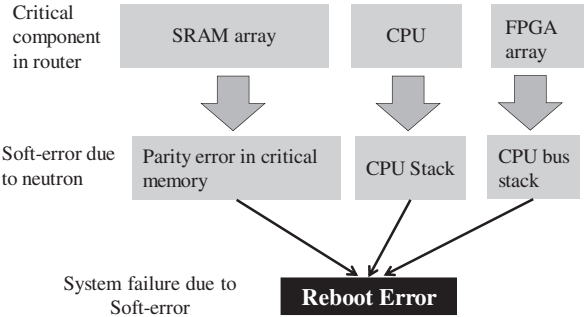


Fig. 2.39 Critical chip layout and irradiation area on the BUT (© 2010 IEEE)

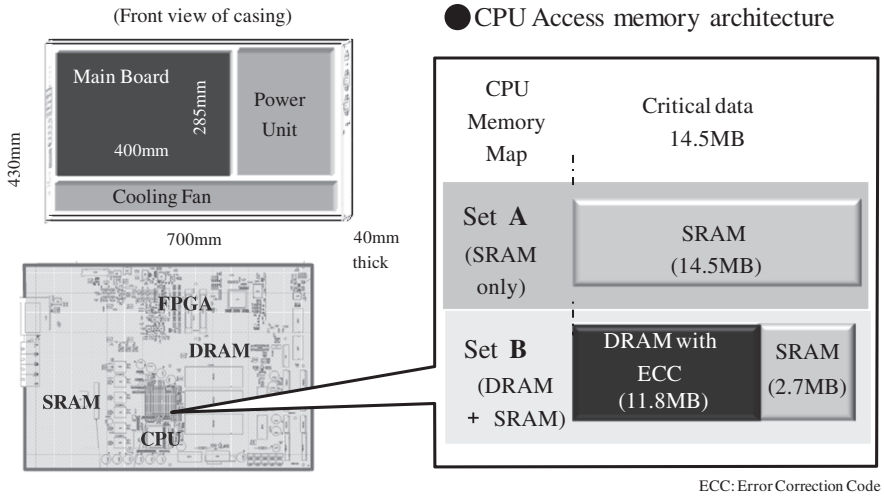
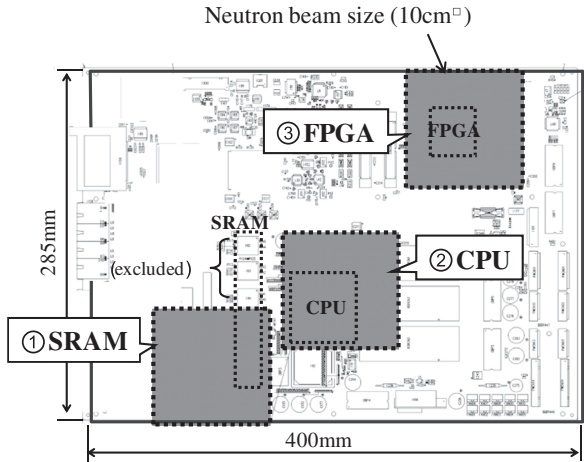


Fig. 2.40 Board casing and CPU access memory map for set A and set B (© 2010 IEEE)

In the memory chip, all 48 MB memory cells are SRAMs for the set A, while 12.5 MB memory cells for timer information which does not require high-speed operation are replaced by DRAMs in the set B. The rest 25.5 MB SRAM memory cells are unchanged because they are utilized to handle the session information and high-speed operation is required. Overall performance is almost equivalent between the sets A and B. Actual size of SRAMs in the test application are 14.5 and 2.7 MB for sets A and B, respectively. Contribution of DRAMs to overall failures is neglected because it is believed to be low enough compared to SRAMs [75].

2.8.1.4 Test Procedures

Direct error detection in each chip is not made, since only BUT failures, namely rebooting, can be commonly used for soft-error susceptibility among three types of chips. System rebooting is found automatically by a PC for error monitoring outside the shielding wall, as shown in Fig. 2.37. Figure 2.41 shows the flowchart of the test procedure. First, the location of the BUT is adjusted to make the neutron beam located on the target chip. A red laser light is used for accurate positioning. After the communication between the BUT and the monitor room is established by using a test program, neutron beam is turned on. Immediately after the neutron beam is on, the timer is turned on to measure time to failure (TTF). When a reboot takes place, error-log and BUT status data are collected. The present BUT is supposed to reboot itself automatically for self-testing if rebooting is successfully done. If automatic

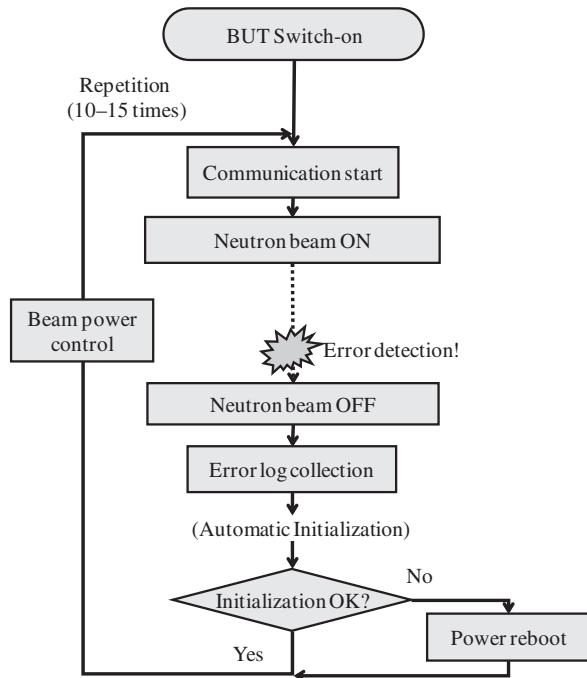


Fig. 2.41 Flowchart of irradiation test (© 2010 IEEE)

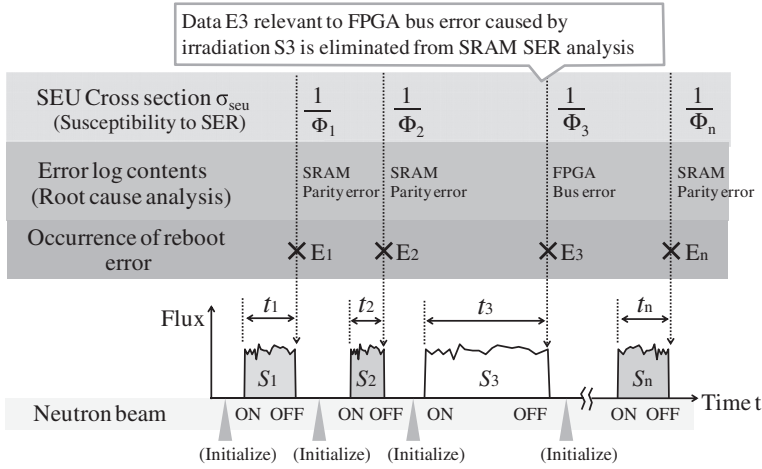


Fig. 2.42 Image of data acquisition and handling (© 2010 IEEE)

reboot is not done due to error in the BUT, BUT is forced to reboot by the rebooting switch.

This procedure is repeated about 10 times to obtain the average cross-section for each chip. Figure 2.42 illustrates an image of data acquisition. Neutron flux is roughly stable as shown in the bottom. The neutron beam is shut off when rebooting takes place due to, for example, parity error in SRAMs and its fluence Φ_i in i th irradiation period is estimated. Here, we define Φ_i as (i th) fluence to failure (FTF). Only if the neutron flux ϕ is very stable (this is not the case in many neutron facilities), FTF can be calculated by

$$\text{FTF} = \phi \text{TTF} \quad (2.8)$$

Otherwise, FTF is estimated from total proton charge bombarded to the Li target to i th TTF. If rebooting is found through root cause analysis to be caused by other parts, for example, FPGA bus error as shown in Fig. 2.42, that are not directly irradiated, the data is eliminated from data analysis for the relevant chip.

As each irradiation cycle corresponds to one failure, mean SEU cross-section σ_{seu} can be obtained in the following manner:

First, mean FTF (MFTF) can be calculated by

$$\text{MFTF} = \frac{1}{n} \sum_{i=1}^n \Phi_i. \quad (2.9)$$

Then,

$$\sigma_{\text{seu}} = \frac{1}{\text{MFTF}} \quad (2.10)$$

where n is the total number of cycles for the relevant chip or board.

2.8.2 Results and Discussions

2.8.2.1 Test Results

Test results of estimated SER in Tokyo sea level are summarized in Table 2.8 for total, SRAM, CPU, and FPGA in sets A and B, respectively. The RTSER (system reboot) measured in Tokyo sea level for about 1 year is also shown for sets A and B in the table.

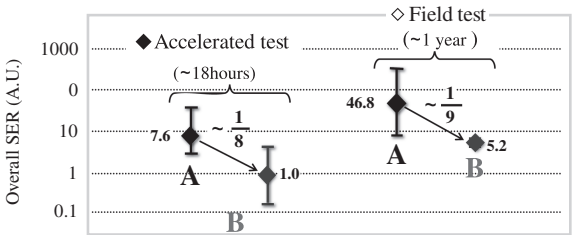
Table 2.8 Test results of SER normalized at Tokyo sea level for set A and B in accelerated and field tests

Set	SRAM Density Use (MB)	Field Test Board	SER Estimated at Tokyo sea level (AU)			
			Accelerated Test			
			Board	Chip	SER	Ratio (%)
A	14.5	46.8	7.6	SRAM	7.22	95
				CPU	0.38	5
				FPGA	—	—
B	2.7	5.2	1.0	SRAM	0.96	96
				CPU	0.03	3
				FPGA	0.01	1

Source: (© 2010 IEEE)

The architectural mitigation method is found to be effective and it can reduce SER in the BUT by a factor of about 8–9. As also shown in Fig. 2.43, this reduction ratio is consistent between the field and accelerator tests.

Fig. 2.43 Comparison of estimated SER in accelerator test and measured SER in field for sets A and B (© 2010 IEEE)



2.8.2.2 Efficacy of Partial Board Irradiation Test

It is seen that the most vulnerable part among three types of parts is identified as SRAM (about 95% of total rebooting events) by partial board irradiation test. Vulnerability in CPU seems to be low but care must be taken that vulnerability depends on the run in CPU and the number of FPGAs actually operated. In the present BUT, the number and operating ratio of FPGAs are relatively small.

Total irradiation duration in accelerated test is only 18 h, showing the efficacy of partial irradiation test compared to 1 year field test.

2.8.2.3 Correlation Between the Irradiation Test and Field Data

It is seen that the architectural mitigation method can reduce SER consistently in field and accelerator tests by a factor of about 10. The absolute values, however, are not consistent with each other: the SER in the field is higher than that in the accelerator test by a factor of 6 or 7.

Three factors that may cause this discrepancy are evaluated below:

- (i) SER estimation error from the accelerator test due to possibly over-simplified procedure is explained in Section 2. Possible range of Weibull Fit parameters S , W , E_{th} are estimated empirically based on 130 nm generation SRAM data as also summarized in Table 2.7. Possible range of the error is estimated according to the parameter range. Maximum error in estimated SER is turned out to be about 15% so that the discrepancy seems to be difficult to explain due to this mechanism.
- (ii) Difference in applications run on the CPU: The application applied to the accelerator test is simple once-write-and-read-many type operation. There is a possibility that the timing of start irradiation was too early compared to the timing by which the critical data (that cause rebooting) in SRAMs are stabilized and the number of SRAMs with critical data may be less than expected. Meanwhile, the application applied to the field is for normal commercial operation. The discrepancy may be explained by this kind of operating rate and more detailed study will be made in future.
- (iii) Effect of low-energy neutrons.

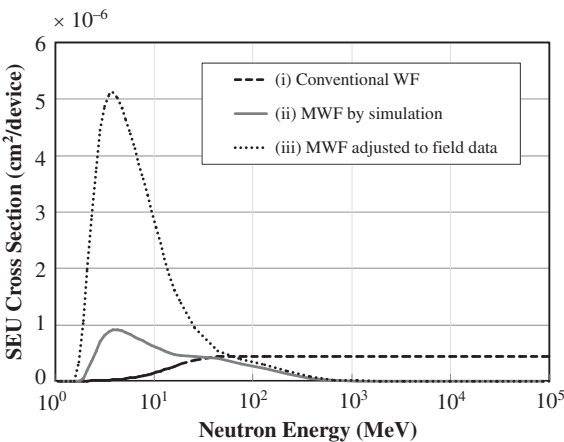
Recent study made by Ibe et al. revealed that contribution of low-energy (1–10 MeV) neutron to SER is surprisingly enhanced as device scaling proceeds from 90 to 22 nm [36, 37], and revision of the Weibull Fit is obviously necessary. Experimental data for low-energy proton and some theoretical works that support the prediction are accumulating rapidly [67–71].

Typical SEU excitation curve simulated for a 90 nm SRAM is shown with a very high low-energy peak in Fig. 2.33, which is clearly different from the curve shown in Fig. 2.6. The low-energy peaks appeared in proton experiments are much higher (one or two orders of magnitude higher than higher energy part) than that predicted in the simulation. The simulation may under-estimate for some reason related to the device layout, structure, and electrical properties including Q_{crit} .

The simplified method assumes the conventional Weibull Fit curve using 3.5 MeV neutron data and eventually ignores the low-energy peak. This deficit may result in the discrepancy. As also indicated in Fig. 2.33, the simulation curve can be fitted by overlapping two newly proposed modified Weibull Fits (MWFs).

By using the MWF curve, the discrepancy can be reduced to a factor of three. As mentioned above, the simulation curve is obtained for our known design SRAMs. Actual layout, structure, and electrical properties, including Q_{crit} of the SRAMs in BUT, are not known and are very likely different from our known device to give a different MWF. Figure 2.44 shows (i) the conventional WF curve, (ii) a fitted MWF curve to the simulation results, and (iii) the MWF curve whose parameters in Eq. (2.6) are intentionally adjusted to cancel the discrepancy. Compared to the height for low-energy peak in the excitation function for the proton experiments, the peak height in the curve (iii) seems acceptable.

Fig. 2.44 Conventional WF curve, an MWF curve shown in Fig. 3.12, and an MWF curve adjusted to make SER estimate based on Eq. (2.3) consistent with the field data (© 2010 IEEE)



2.9 Hierarchical Mitigation Strategies

2.9.1 Basic Three Approaches

From a reliability viewpoint, mitigation design based on the average chip-level SER estimation methods mentioned in Section 2.7, however, somewhat dangerous if the variation due to circuits and applications (i.e., masking effects) is large as exemplified in Fig. 2.45a. Without certain knowledge of the variation (not necessarily

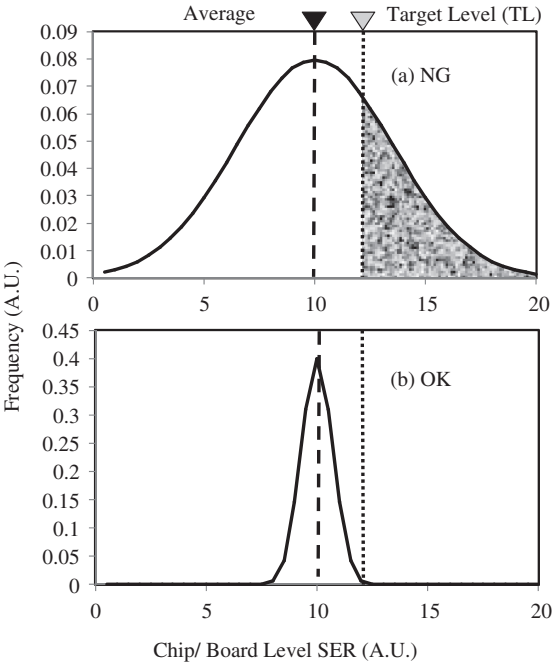


Fig. 2.45 Concept of availability of tolerable level set for chips. Availability depends significantly on the range of variation (© 2010 IEEE)

Poisson distribution) one may design an electronic product with too low SER tolerable level, which leads to under design.

If the variation is small enough, the margin can be small, as shown in Fig. 2.45b. Mitigation strategies can, therefore, be threefold as summarized in Table 2.9. First, current major strategy is design on the average (DOA), which determines the target SER level without the knowledge of variation. Second one is design on average with knowledge of variation (DOAV). Just design (cost, power, speed, and reliability) may be realized through this approach. This strategy including evaluation of logic-masking (or derating) is, however, quite difficult and time/cost consuming to realize because of possible wide variation depending on the circuits and applications.

Assuming Poisson distribution for memory errors, upper limit of device-level SER, SER_{ul} is given by the following equation [6]:

$$SER_{ul} = \frac{\chi_{(\alpha/2):k}^2}{2NT_r} \times 10^9 \quad (2.11)$$

where $\chi_{(\alpha/2):k}^2$: chi-square value given according to parameters α and k ; α : ratio of population outside of the Poisson distribution, depending on the confidence level (CL). If CL = 95%, $\alpha = 0.1$ since CL = $1 - \alpha/2(\%)$; k : degree of freedom = $2(N_{err} + 1)$; N_{err} : number of errors found at the time T_r (h); and N : number of devices tested.

As for chip-level SER, the variation is originated from circuits and applications. Since it is not a random process, this kind of statistical theory seems to be very difficult to establish.

The third strategy believed to be worthwhile to pursue is design on the upper bound (DOUB).

2.9.2 Design on the Upper Bound (DOUB)

The entire scope of DOUB is summarized in Fig. 2.46. Upper bound chip-level SER can be given by the simple summation of all raw SERs of gates and memories as already shown in Eq. (2.5). If the sum SER for a chip is acceptable from reliability viewpoint, no further action is needed for the chip. If not, simple countermeasure (simple exchange of weak gates/memory devices to stronger ones based on the raw SER database) would be applied stepwise.

If the contribution of memories to total chip-level SER is high, ECC with interleaving is effective mitigation technique. If the contribution of logic parts is high, more precise evaluation of the upper bound may be necessary first. Upper bound of masking effects or effects of some other factors independent of circuits and application may be implemented to the Eq. (2.5). Depth of pipe-line, number of bits in a word, number of cache layers maybe such factors.

Table 2.9 Concepts of mitigation design of chip-level SER

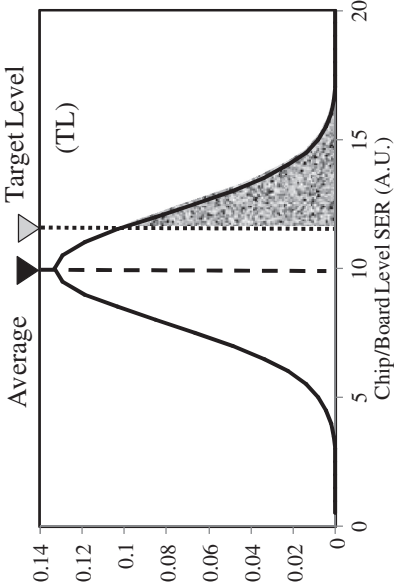
Class	Concept	Merit	Demerit
Design on average (DOA)		<ul style="list-style-type: none">• Comparatively simple	<ul style="list-style-type: none">• Risk of under design• Depends on circuits and application

Table 2.9 (continued)

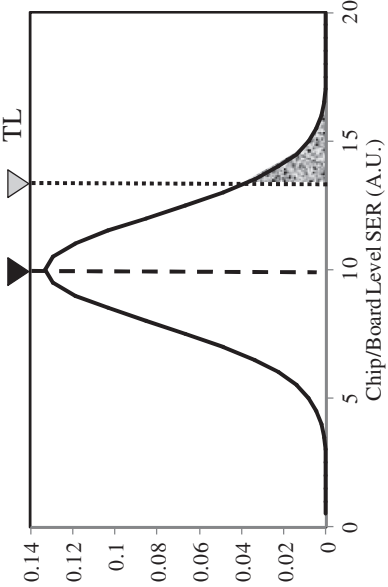
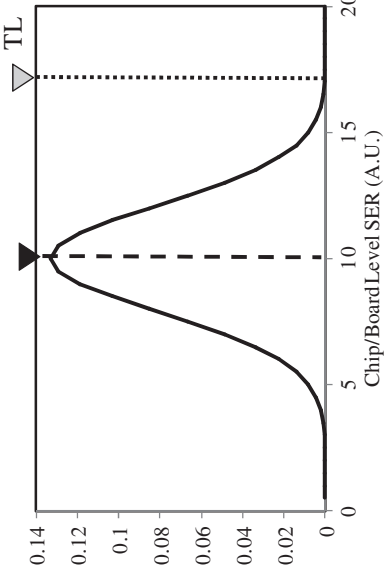
Class	Concept	Merit	Demerit
Design on average and variation (DOAV)		<ul style="list-style-type: none">• Just design	<ul style="list-style-type: none">• Depends on circuits and applications• High cost

Table 2.9 (continued)

Class	Concept	Merit	Demerit
Design on upper bound (DOUB)		<ul style="list-style-type: none">• Simple• Does not depend on circuits and application• Low cost	<ul style="list-style-type: none">• Risk of over design

Source: (© 2010 IEEE)

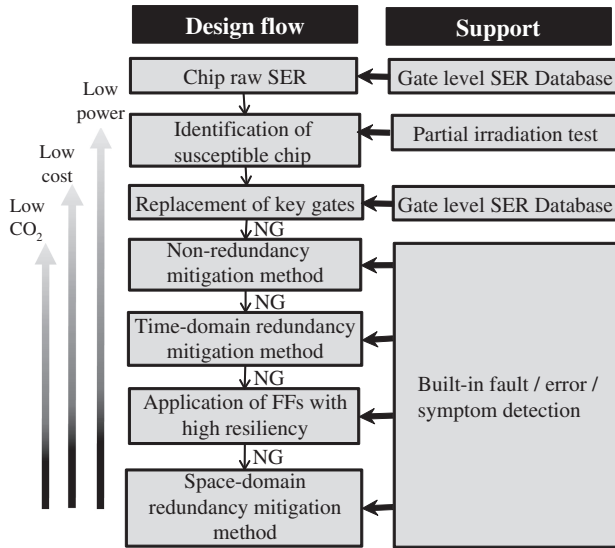


Fig. 2.46 General design flow of stepwise reduction in SER under the design on upper bound concept. Power consumption, cost, and global warming are key issues (© 2010 IEEE)

Upper bound masking factor, whose underlying physics is not necessarily the same as the conventional average masking factor and can be much more simple, may be defined and implemented. Operations that do not require high speed can be carried out with slower but more resilient gates or memories. Architectural countermeasure considering the best matches in trade-offs is one of the steps. The mitigation method described in Section 2.8 is one of such examples.

Further steps are applications and optimization of non- or small-redundancy mitigation method, time domain redundancy methods, and robust FF to SEUs and MNUs. Space redundancy methods may cause high cost and power dissipation, so that application of such techniques has to be avoided or limited to very small portion. Moreover, power consumption of network systems including data centers is becoming one of the top priority issues for future world-wide infrastructure to reduce carbon oxide. As high as 10% of total power consumption will be dedicated to network systems until 2020 unless effective countermeasures are applied (<http://www.gimmithescoop.com/data-center-power-consumption-global-warming-will-the-web-crash>). Fault/error/symptom detection device or circuits may be effective for recovery if they are built-in at design phase. One of such recovery scheme LABIR is introduced in the following section.

2.10 Inter Layer Built-In Reliability (LABIR)

Even if space redundancy techniques are applied, they are intrinsically vulnerable against MNUs as mentioned before. Effective countermeasure listed in Fig. 2.47

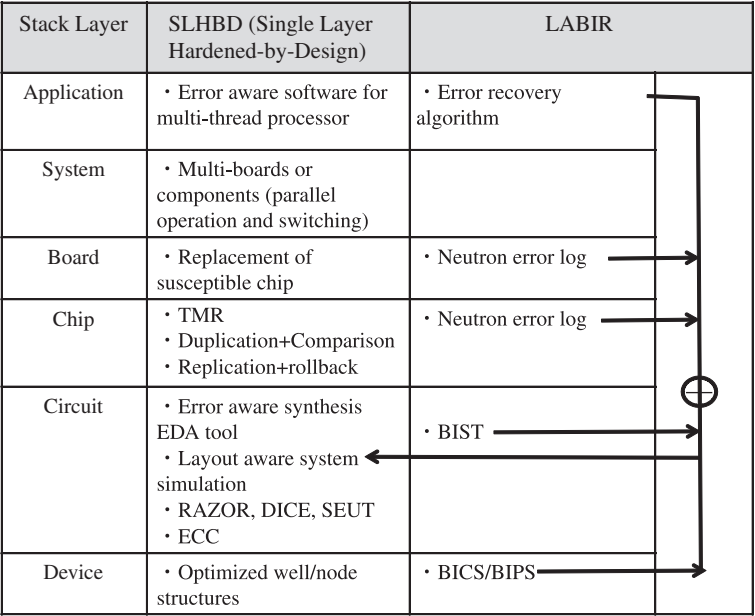


Fig. 2.47 Single layer hardened-by-design and examples of LABIR

and implemented in a single stack layer (device, chip, board, . . .) seems to be almost impossible as the device scaling proceeds.

Obviously, MNU cannot be controlled in the device layer. Specially designed items that make reliability-related communication and action possible between two or more layers may be effective for overall reliability. We call this kind of our approach as LABIR. Concept of a similar approach has been introduced in SELSE VI [78].

LABIR concept is also illustrated in Fig. 2.47. LABIR proposes interactive or communicative mitigation techniques in which a recovery action such as rollback to the checkpoint ignited when a layer finds any error symptom, not necessarily error or fault itself. Built-in self-test (BIST) [79–81], built-in current (pulse) sensor (BICS [82], BIPS)) can be used for such kind of technique. By using BIPS, a pulse propagated from a multi-coupled bipolar interaction (MCBI) [16] zone in p-well is supposed to be detected and ignite the rollback operation in the ULSI chip.

2.11 Summary

Trends in terrestrial neutron-induced soft error in SRAMs down to 22 nm process are predicted by using the Monte-Carlo simulator CORIMS, which is validated to have less than 20% variations from experimental data in a wide variety of neutron

fields like the low and high-altitude field tests and the accelerator tests in LANSCE, TSL, and CYRIC.

The following results are obtained:

- (1) Soft-error rates per device in SRAMs will increase 3–7 times from 130 nm to 22 nm process.
- (2) As SRAM is scaled down to smaller size, SEU is dominated more significantly by low-energy neutrons (<10 MeV). But MCU does not change drastically.
- (3) The area affected by one nuclear reaction spreads well beyond 1 M bits area and multiplicity of multi-cell upset become as high as 100 bits and more.

The discussions are extended to the MNUs of logic devices/systems and counter-measures to them. New bipolar SEU mode is investigated by (quasi-)mono-energetic neutron test and Monte-Carlo and TCAD simulations. The mode turned out to be caused by penetration of secondary ions through p–n junctions (not necessarily storage nodes) and be a parasitic thyristor action triggered by single-event snapback in p-well. The mode can also cause MNU with high probability.

Recent novel trends and data with device scaling below 100 nm are reviewed and the following shortages in current SER test standards are pointed out:

- (1) Contributions of neutrons with energies lower than 10 MeV are becoming significant as predicted by simulation mentioned above. The energy range for the spallation neutron tests has to be reconsidered. The shape of SEU excitation function is also subject to be revised.
- (2) Standard test methods for logic gates should be determined. Effects of SETs in the global control line for FFs (clock, set/reset lines) have to be taken into account.
- (3) MNUs in combinational logic device have to be taken into consideration.
- (4) Chip or board-level SER tests may be included with mitigation strategies in new SER standards.

A novel chip-level to board-level SER evaluation method for network routers is introduced by using 65 MeV quasi-mono-energetic neutron beams. Architectural mitigation technique against terrestrial neutron SER for the router is demonstrated. The method is based on the replacement of SRAMs to DRAMs in a chip where speed is not first priority considering operating ratio and showed about 10 times reduction in board-level SER. This reduction ratio is consistent with the field data for about 1-year commercial operation. The absolute SER level estimated from the accelerated test is, however, 6–7 times lower than the field data. Low-energy neutron contribution is pointed out as the most probable root of this discrepancy.

A generic strategy for low cost and low power consumption mitigation of chip and board-level SER based upon the stepwise upper bound reduction is proposed. Partial irradiation method is one of key techniques in this strategy. Inter-layer built-in reliability (LABIR) in which communicative mitigation techniques are applied

to among stack layers is also proposed as another key technology. LABIR can be robust against multi-node upsets (MNUs) in logic parts with low overhead in power, speed, cost, and area.

References

1. N. Sugii, R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, K. Torii, and S. Kimura, "Comprehensive Study on V_{th} Variability in Silicon on Thin BOX (SOTB) CMOS with Small Random-Dopant Fluctuation: Finding a Way to Further Reduce Variation," *IEDM, San Francisco, December 15–17*, pp. 249–253 (2008).
2. R. Duarte, L. Martins-Filho, G. Knop, and R. Prado, "A Fault-Tolerant Attitude Determination System Based on COTS Devices," *IOLTS 2008, Greece, July 6–9, 2008*, No.4.3, pp. 85–92 (2008).
3. D. Villanueva, A. Pouydebasque, E. Robillart, T. Skotnicki, E. Fuchs, and H. Jaoue, "Impact of the Lateral Source/Drain Abruptness on MOSFET Characteristics and Transport Properties," *2003 IEDM, Washington, DC, December 7–10, 2003*, No.9.4 (2003).
4. H.-S. P. Wong, "Beyond the Conventional Transistor," *IBM J. Res. Develop.*, Vol. 46, No. 2/3, pp. 133–168 (2002).
5. E. Ibe, "Current and Future Trend on Cosmic-Ray-Neutron Induced Single Event Upset at the Ground Down to 0.1-Micron-Device," *The Svedberg Laboratory Workshop on Applied Physics, Uppsala, May 3, 2001*, No.1 (2001).
6. JEDEC, "Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices: JESD89A," *JEDEC STANDARD, JEDEC Solid State Technology Association, Arlington, VA., USA*, No.89, pp. 1–85 (2006).
7. JEITA, "JEITA SER Testing Guideline," *EIAJ EDR-4705, Tokyo, Japan*, pp. 1–62 (2005).
8. IEC, "Part 38: Soft Error Test Method for Semiconductor Devices with Memory," *Semiconductor Devices. Mechanical and Climatic Test Methods*, IEC60749-38, Edition 1.0, pp. 1–9 (2008).
9. Automotive Electronics Council, "Failure Mechanism Based Stress Test Qualification for Integrated Circuits," *AEC-Q100-Rev.G*, May 14 (2007).
10. T. Heijmen, E. Ibe, P. Roche, F. Vermunt, and A. Bougerol, "Panel:SER in Automotive: What is the Impact of the AEC-Q100-G Spec?," *IOLTS 2008, Greece, July 6–9, 2008*, No.S3, p. 161 (2008).
11. D. Radaelli, H. Puchner, P. Chia, S. Wong, and S. Daniel, "Investigation of Multi-Bit Upsets in a 150 nm Technology SRAM Device," *Trans. Nucl. Sci.*, Vol. 52, No. 6, pp. 2433–2437 (2005).
12. O. Musseau, Gardic P. Roche, T. Corbiere, R.A. Reed, S. Buchner, et al., "Analysis of Multiple Bit Upsets in a CMOS SRAM," *Trans. Nucl. Sci.*, Vol. 43, No. 6, pp. 2879–2888 (1996).
13. J. Maiz, S. Hareland, K. Zhang, and P. Armstrong, "Characterization of Multi-Bit Soft Error Events in Advanced SRAMs," *2003 IEEE International Electron Devices Meeting, Washington, DC, December 7–10, 2003*, No.21.4 (2003).
14. E. Ibe, H. Kameyama, Y. Yahagi, K. Nishimoto, and Y. Takahashi, "Distinctive Asymmetry in Neutron-Induced Multiple Error Patterns of 0.13 μm Process SRAM," *The 6th International Workshop on Radiation Effects on Semiconductor Devices for Space Application, Tsukuba, October 6–8, 2004*, pp. 19–23 (2004).
15. N. Seifert, and V. Zia, "Assessing the Impact of Scaling on the Efficacy of Spatial Redundancy Based Mitigation Schemes for Terrestrial Applications," *SELSE3, Austin, TX, April 3, 4, 2007* (2007).
16. E. Ibe, S. Chung, S. Wen, H. Yamaguchi, Y. Yahagi, H. Kameyama, S. Yamamoto, and T. Akioka, "Spreading Diversity in Multi-Cell Neutron-Induced Upsets with Device Scaling," *2006 CICC, San Jose, CA, September 10–13*, pp. 437–444 (2006).

17. K. Pagiamtzis, N. Azizi, and F. Najm, "A Soft-Error Tolerant Content-Addressable Memory (CAM) Using An Error-Correcting-Match Scheme," *Idem.*, pp. 301–304 (2006).
18. B.D. Olson, D. Ball, K.M. Warren, L.W. Massengill, N.F. Haddad, S.E. Doyle, and D. McMorro, "Simultaneous Single Event Charge Sharing and Parasitic Bipolar Conduction in a Highly-Scaled SRAM Design," *Trans. Nucl. Sci.*, Vol. 52, No. 6, pp. 2132–2136 (2005).
19. O.A. Amusan, L.W. Massengill, B.L. Bhuva, P.R. Fleming, and M.L. Alles, "Charge Collection and Sharing in a 130 nm CMOS Technology," *Trans. Nucl. Sci.*, Vol. 53, No. 6, pp. 3253–3258 (2006).
20. O.A. Amusan, L.W. Massengill, M.P. Baze, B.L. Bhuva, A.F. Witulski, J.D. Black, A. Balasubramanian, M.C. Casey, D.A. Black, J.R. Ahlbin, R.A. Reed, and M.W. McCurdy, "Mitigation Techniques for Single Event Induced Charge Sharing in a 90 nm Bulk CMOS Process," *IRPS 2008, Phoenix, Arizona, April 27–May 1*, No.5A.1 (2008).
21. K. Osada, K. Yamaguchi, Y. Saitoh, and T. Kawahara, "Cosmic-Ray Multi-Error Immunity for SRAM, Based on Analysis of the Parasitic Bipolar Effect," *Symp. VLSI Circuits Dig.*, pp. 255–256 (2003).
22. T. Nakauchi, N. Mikami, A. Oyama, H. Kobayashi, H. Usui, and J. Kase, "A Novel Technique for Mitigating Neutron-Induced Multi-Cell Upset by Means of Back Bias," *IRPS 2008, Phoenix, Arizona, April 27–May 1, 2008*, No.2F.2, pp. 187–191 (2008).
23. M. Baze, J. Wert, J. Clement, M. Hubert, A. Witulski, O.A. Amusan, L. Massengill, and D. McMorro, "Propagating SET Characterization Technique for Digital CMOS Libraries," *Trans. Nucl. Sci.*, Vol. 53, No. 6, pp. 3472–3478 (2006).
24. V. Ferlet-Cavrois, V. Pouget, D. McMorro, J.R. Schwank, N. Fel, F. Essely, R.S. Flores, P. Paillet, M. Gaillardin, D. Kobayashi, J.S. Melinger, O. Duhamel, P.E. Dodd, and M.R. Shaneyfelt, "Investigation of the Propagation Induced Pulse Broadening (PIPB) Effect on Single Event Transients in SOI and Bulk Inverter Chains," *Trans. Nucl. Sci.*, Vol. 55, No. 6, pp. 2842–2853 (2008).
25. E.H. Cannon, and M., Cabanas-Holmen, "Heavy Ion and High Energy Proton-Induced Single Event Transients in 90 nm Inverter, NAND and NOR Gates," *Trans. Nucl. Sci.*, Vol. 56, No. 6, pp. 3511–3518 (2009).
26. T. Makino, D. Kobayash, K. Hirose, D. Takahashi, S. Ishii, M. Kusano, S. Onoda, T. Hirao, and T. Ohshima, "Soft-Error Rate in a Logic LSI Estimated from SET Pulse-Width Measurements," *Idem.*, pp. 3180–3184 (2009).
27. T. Calin, M. Nicolaidis, and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology," *Trans. Nucl. Sci.*, Vol. 43, No. 6, pp. 2874–2878 (1993).
28. S. Mitra, M. Zhang, N. Seifert, T. Mak, and K.S. Kim, "Built-In Soft Error Resilience for Robust System Design," *ICICDT2007, Austin, TX, May 18–20*, pp. 263–268 (2009).
29. T. Uemura, Y. Tosaka, H. Matsuyama, K. Shono, K. Takahisa, M. Fukuda, and K. Hatanaka, "Robust Against Soft-Error Latch for Protecting SEU by Charge Sharing and SET on Inter-Clock," *IRPS 2010, Anaheim, CA, USA, May 2–6* (2010).
30. H.-H. Lee, K. Lilja, and S. Mitra, "Design of a Sequential Logic Cell Using LEAP: Layout Design Through Error Aware Placement," *SELSE6, Stanford University, Stanford, CA, USA, March 23, 24* (2010).
31. M. Cabanas-Holmen, E.H. Cannon, A. Kleinosowski, J. Ballast, J. Killens, and J. Socha, "Clock and Reset Transients in a 90 nm RHBD Single-Core Tilera Processor," *Trans. Nucl. Sci.*, Vol. 53, No. 6, pp. 3505–3510 (2009).
32. N. Seifert, B. Gill, M. Zhang, V. Zia, and V. Ambrose, "On the Scalability of Redundancy Based SER Mitigation Schemes," *ICICDT2007, Austin, TX, May 18–20*, No.G2, pp. 197–205 (2007).
33. A. Lesea, and K. Castellani-Coulie, "Experimental Study and Analysis of Soft Errors in 90 nm Xilinx FPGA and Beyond," *2007 RADECS, Deauville, France, September 10–14*, No.DWL-13 (2007).
34. D. Skarin, and J. Karlsson, "Software Mechanisms for Tolerating Soft Errors in an Automotive Brake-Controller," *WDSN, Estoril, Lisbon, Portugal, June 29, 2009*, pp. D34–D38.

35. S. Wen, A. Silburt, and R. Wong, "IC Component SEU Impact Analysis," *SELSE4, University of Texas at Austin, Austin, TX, March, 26, 27* (2008).
36. E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Scaling Effects on Neutron-Induced Soft Error in SRAMs Down to 22 nm Process," *WDSN, Estoril, Lisbon, Portugal, June 29* (2009).
37. E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of Scaling on Neutron-Induced Soft Error in SRAMs from a 250 to a 22 nm Design Rule," *IEEE Trans. Electron Devices*, Vol. 57, No. 7, pp. 1527–1538 (2010).
38. T. Nakamura, M. Baba, E. Ibe, Y. Yahagi, and H. Kameyama, "Terrestrial Neutron-Induced Sift-Errors in Advanced Memory Devices," *New Jersey, World Scientific* (2008).
39. C. Hu, "Alpha-Particle-Induced Field and Enhanced Collection of Carriers," *IEEE Electron Device Lett.*, EDL-3, No. 2, pp. 31–34 (1982).
40. E. Ibe, Y. Yahagi, F. Kataoka, Y. Saito, A. Eto, and M. Sato, "A Self-Consistent Integrated System for Terrestrial-Neutron Induced Single Event Upset of Semiconductor Devices at the Ground," *2002 ICITA, Bathurst, Australia, November 25–28, 2002*, No.273–221 (2002).
41. Y. Yahagi, E. Ibe, Y. Saito, A. Eto, and M. Sato, "Self-Consistent Integrated System for Susceptibility to Terrestrial-Neutron Induced Soft-Error of Sub-quarter Micron Memory Devices," *2002 International Integrated Reliability Workshop, Stanford Sierra Camp, S. Lake Tahoe, CA*, pp. 143–143 (2002).
42. E. Ibe, S. Chung, S. Wen, Y. Yahagi, H. Kameyama, S. Yamamoto, T. Akioka, and H. Yamaguchi, "Valid and Prompt Track-Down Algorithms for Multiple Error Mechanisms in Neutron-Induced Single Event Effects of Memory Devices," *RADECS, Athens, Greece, September 27–29, 2006*, No. D-2 (2006).
43. K. Johansson, P. Dyreklev, B. Granbom, N. Olsson, J. Blomgren, and P-U. Renberg, "Energy-Resolved Neutron SEU Measurements from 22 to 13.0 MeV," *Trans. Nucl. Sci.*, Vol. 45, No. 6, pp. 2519–2526 (1998).
44. A.V. Prokofiev, O. Bystrom, C. Ekstrom, V. Ziemann, J. Blomgren, U.S. Pomp, S., M. Osterlund, and U. Tippawan, "The TSL Neutron Beam Facility," *10th Symposium on Neutron Dosimetry, Uppsala, Sweden, June 12–13, 2003*, Lecture A1–4 (2006).
45. M. Baba, H. Okamura, M. Hagiwara, T. Itoga, S. Kamada, Y. Yahagi, and E. Ibe, "Installation and Application of An Intense $^7\text{Li}(p,n)$ Neutron Source for 20–90 MeV Region," *Radiat. Prot. Dosimetry*, Vol. 123, No. 1–4, pp. 13–17 (2007).
46. H.W. Bertini, A.H. Culkowski, O.W. Hermann, N.B. Gove, and M.P. Guthrie, "High Nenergy ($E < 100$ GeV) Intranuclear Cascade Model for Nucleons and Pions Incident on Nuclei and Comparisons with Experimental Data," *Phys. Rev. C*, Vol. 17, No. 4, pp. 1382–1394 (1978).
47. I. Dostrovsky, Z. Fraenkel, and G. Friedlander, "Monte Carlo Calculations of Nuclear Evaporation Process. III. Applications to Low-Energy Reactions," *Phys. Rev.*, Vol. 113, No. 3, pp. 3.83–702 (1959).
48. E. Ibe, Y. Yahagi, H. Kameyama, and Y. Takahashi, "Single Event Effects of Semiconductor Devices at the Ground," *Ionizing Radiat*, Vol. 30, No. 7, pp. 263–281 (2004).
49. S. Furihata, "Parameters Used in GEM", Thesis for PhD, Tohoku University, pp. 18–20 (2002)
50. F. Bertland, and R. Peele, "Complete Hydrogen and Helium Particle Spectra from 30- to 60-MeV Proton Bombardment of Nuclei with $A=12$ to 209 and Comparison with the Intranuclear Cascade Model," *Phys. Rev. C*, Vol. 8, No. 3, pp. 1045–1064 (1973).
51. K.M. Warren, J.D. Wilkinson, R.A. Weller, B.D. Sierawski, R.A. Reed, M.E. Porter, M.H. Mendenhall, and R.D. Schrimpf, L.W. Massengill, "Predicting Neutron Induced Soft Error Rates: Evaluation of Accelerated Ground Based Test Methods," *IRPS 2008, Phoenix, AZ, April 27–May 1*, No.5A.2, pp. 473–477 (2008)
52. P.W. Lisowski, "The Los Alamos National Laboratory Spallation Neutron Sources," *Nucl. Sci. Eng.*, Vol. 103, pp. 208–218 (1990).
53. M. Baba, M. Takada, T. Iwasaki, S. Matsuyama, T. Nakamura, H. Ohguchi, T. Nakao, T. Sanami and N. Hirakawa, "Development of Monoenergetic Neutron Calibration Fields

- Between 8 keV and 15 MeV," *Nucl. Instrum. Methods Phys. Res. A*, Vol. 376, pp. 115–123 (1996).
54. A. Dixit, R. Heald, and A. Wood, "Trends from Ten Years of Soft Error Experimentation," *SELSE 5, Stanford University, Stanford, CA, March 24, 25 (2009)*.
 55. S. Wen, "Systematical Method of Quantifying SEU FIT," *IOLTS 2008, Greece, July 6–9, 2008*, pp. 109–116 (2008).
 56. G. Schindlbeck, and C. Slayman, "Neutron-Induced Logic Soft Errors in DRAM Technology and Their Impact on Reliable Server Memory," *SELSE3, Austin, TX, April 3, 4, 2007 (2007)*.
 57. R.C. Baumann, and E.B. Smith, "Neutron-Induced Boron Fission as a Major Source of Soft Errors in Deep Submicron SRAM Devices," *2000 IEEE Int'l Reliability Physics Symposium Proceedings, San Jose, CA, April 10–13*, pp. 152–157 (2000).
 58. E.W. Blackmore, "Development of a Large Area Neutron Beam for System Testing at TRIUMF," *2009 IEEE Radiation Effects Data Workshop, Quebec City, Canada, July 20–24*, pp. 157–160 (2009).
 59. A.V. Prokofiev, J. Blomgren, R. Nolte, S. Rottger, S.P. Platt, and A.N. Smirnov, "Characterization of the ANITA Neutron Source for Accelerated SEE Testing at The Svedberg Laboratory," *Idem.*, pp. 166–173 (2009).
 60. H. Sakai, H. Okamura, H. Otus, T. Wakasa, S. Ishida, N. Sakamoto, T. Uesaka, Y. Satou, S. Fujita, and K. Hatanaka, "Facility for the (p,n) polarization transfer measurement," *Nucl. Instrum. Methods Phys. Res., Section A*, Vol. 369, pp. 120–134 (1996).
 61. S.P. Platt, and Z. Torok, "Charge-Collection and Single-Event Upset Measurements at the Isis Neutron Source," *2007 RADECS, Deauville, France, September 10–14, 2007*, No.F-2 (2007).
 62. H. Kobayashi, H. Usuki, K. Shiraishi, H. Tsuchiya, N. Kawamoto, G. Kase, and J. Merchant, "Comparison Between Neutron-Induced System-SER and Accelerated-SER in SRAMs," *2004 IRPS, April 25–29, Phoenix, AZ*, pp. 288–293 (2004).
 63. A. Lesea, and J. Fabula, "Continuing Experiments on Atmospheric Neutron Effects on Deep Sub-micron Integrated Circuits," *RADECS, Athens, Greece, September 27–29, 2006*, No.D-4 (2006).
 64. J-L. Autran, P. Roche, J. Borel, C. Sudre, C., Castellani-Coulie, D. Muntean, T. Parrassin, G. Gasiot, and J-P. Schoellkopf, "Altitude SEE Test European Platform (ASTEP): Project Overview, First Results in CMOS 130 nm and Perspectives," *Idem.*, No.D-5 (2003).
 65. J.L. Autran, P. Roche, S. Sauze, G. Gasiot, D. Munteanu, P. Loaiza, M. Zampaolo, J. Borel, S. Rozov, and E. Yakushev, "Combined Altitude and Underground Real-Time SER Characterization of CMOS Technologies on the ASTEP-LSM Platform," *ICICDT2007, Austin, TX, May 18–20*, pp. 113–120 (2009).
 66. Y. Tosaka, R. Takasu, T. Uemura, H. Ehara, H. Matsuyama, S. Satoh, A. Kawai, and M. Hayashi, "Simultaneous Measurement of Soft Error Rate of 90 nm CMOS SRAM and Cosmic Ray Neutron Spectra at the Summit of Mauna Kea," *IRPS 2008, Phoenix, AZ, April 27–May 1, 2008*, No.SE01, pp. 727–728 (2008).
 67. B.D. Sierawski, J.A. Pellish, R.A. Reed, R.D. Schrimpf, K.M. Warren, R.A. Weller, M.H. Mendenhall, A.D. Tipton, M.A. Xapsos, R.C. Baumann, X. Deng, M.J. Campola, M.R. Friendlich, H.S. Kim, A.M. Phan, and C.M. Seidleck, "Impact of Low-Energy Proton Induced Upsets on Test Methods and Rate Predictions," *Trans. Nucl. Sci.*, Vol. 56, No. 6, pp. 3085–3092 (2009).
 68. B.D. Sierawski, K.M. Warren, R.A. Reed, R.A. Weller, M.M. Mendenhall, R.D. Schrimpf, and R.C. Baumann, "Contribution of Low-Energy Neutrons to Upset Rate in a 65 nm SRAM," *IRPS, Anaheim, CA, USA, May 2–6, 2010*, No.197 (2010).
 69. D.F. Heidel, P.W. Marshall, J.A. Pellish, K.P. Rodbell, K.A. LaBe, J.R. Schwank, S.E. Rauch, M.C. Hakey, M.D. Berg, C.M. Castaneda, P.E. Dodd, M.R. Friendlich, A.D. Phan, C.M. Seidleck, M.R. Shaneyfelt, and M.A. Xapsos, "Single-Event Upsets and Multiple-Bit Upsets on a 45 nm SOI SRAM," *Trans. Nucl. Sci.*, Vol. 56, No. 6, pp. 3499–3504 (2009).
 70. R.K. Lawrence, J.F. Ross, N. Haddad, D. Albrect, R.A. Reed, and M.A. McMahan-Norris, "Soft Error Sensitivities in 90 nm Bulk CMOS SRAMs," *2009 IEEE Radiation Effects Data Workshop, July 20–24, Quebec, Canada*, pp. 123–126 (2009).

71. C. Slayman, "Accuracy of Various Broad Spectrum Neutron Sources for Accelerated Soft Error Testing," *SELSE6, Stanford University, Stanford, CA, March 23, 24* (2010).
72. H. Chapman, E. Landman, A. Margalitlovich, Y.-P. Fang, A.S. Oates, D. Alexandrescu, and O. Lauzeral, "A Multi-Partner Soft Error Rate Analysis of an Infini Band Host Channel Adapter," *SELSE6, Stanford University, Stanford, CA, March 23, 24* (2010).
73. H. Ando, and S. Hatanaka, "Accelerated Testing of a 90 nm SPARC3.4 V Microprocessor for Neutron SER," *SELSE3, Austin, TX, April 3, 4* (2007).
74. A.L. Silburt, A. Evans, I. Perryman, S.-J. Wen, and D. Alexandrescu, "Design for Soft Error Resiliency in Internet Core Routers," *Trans. Nucl. Sci.*, Vol. 56, No. 6, pp. 3551–3555 (2009).
75. L. Borucki, G. Schindlbeck, and C. Slayman, "Comparison of Accelerated DRAM Soft Error Rates Measured at Component and System Level," *IRPS 2008, Phoenix, AZ, April 27–May 1*, No.5A.4 (2008).
76. K. Shimbo, T. Toba, E. Ibe, and K. Nishi, "Correlation of Mitigation of Soft-Error Rate of Routers Between Neutron Irradiation Test and Field Soft-Error Data," *IEICE Tech. Rep.*, Vol. 109, No. 317, 318, pp. 51–55 (2009) (In Japanese).
77. E. Ibe, H. Kameyama, Y. Yahagi, and H. Yamaguchi, "Single Event Effects as a Reliability Issue of IT Infrastructure," *ICITA, July 3–7, 2005, Sydney*, Vol. I, pp. 555–53.0 (2005).
78. N. Carter, "Cross-Layer Reliability," *SELSE6, Stanford University, Stanford, CA, March 23, 24* (2010).
79. A. Sanyal, S. Alam, and S. Kundu, "A Built-In Self-Test Scheme for Soft Error Rate Characterization," *IOLTS 2008, Greece, July 6–9, 2008*, No.3.3, pp. 65–72 (2008).
80. S. Prejean, "Neutron Soft Error Rate Testing of AMD Microprocessors," *SELSE6, Stanford University, Stanford, CA, March 23, 24, 2010* (2010).
81. A. Balasubramanian, B.L. Bhuvu, L.W. Massengill, B. Narasimham, R.L. Shuler, T.D. Loveless, and W. T. Holman, "A Built-In Self-Test (BIST) Technique for Single-Event Testing in Digital Circuits," *Trans. Nucl. Sci.*, Vol. 55, No. 6, pp. 3130–3135 (2009).
82. T. Wang, Z. Zhang, L. Chen, A. Dinh, and R. Shuler, "A Novel Bulk Built-In Current Sensor for Single-Event Transient Detection," *SELSE6, Stanford University, Stanford, CA, March 23, 24* (2010).

Dependability in Electronic Systems
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2011, XXV, 204 p., Hardcover

ISBN: 978-1-4419-6714-5