

# Contents

<b>1</b>	<b>Introduction</b>	1
1.1	Trends	1
1.1.1	Application Requirements	1
1.1.2	Implementation and Design	3
1.1.3	Time and Cost	4
1.1.4	Summary	5
1.1.5	Example System	6
1.2	Requirements	9
1.2.1	Scalability	10
1.2.2	Diversity	10
1.2.3	Composability	11
1.2.4	Predictability	13
1.2.5	Reconfigurability	14
1.2.6	Automation	15
1.3	Key Components	16
1.4	Organisation	18
<b>2</b>	<b>Proposed Solution</b>	19
2.1	Architecture Overview	19
2.1.1	Contention-Free Routing	21
2.2	Scalability	22
2.2.1	Physical Scalability	23
2.2.2	Architectural Scalability	23
2.3	Diversity	24
2.3.1	Network Stack	25
2.3.2	Streaming Stack	25
2.3.3	Memory-Mapped Stack	26
2.4	Composability	28
2.4.1	Resource Flow-Control Scheme	28
2.4.2	Flow Control and Arbitration Granularities	29
2.4.3	Arbitration Unit Size	32
2.4.4	Temporal Interference	32

2.4.5	Summary .....	33
2.5	Predictability .....	33
2.5.1	Architecture Behaviour .....	34
2.5.2	Modelling and Analysis .....	34
2.6	Reconfigurability .....	35
2.6.1	Spatial and Temporal Granularity .....	35
2.6.2	Architectural Support .....	37
2.7	Automation .....	37
2.7.1	Input and Output .....	38
2.7.2	Division into Tools .....	38
2.8	Conclusions .....	39
<b>3</b>	<b>Dimensioning .....</b>	<b>41</b>
3.1	Local Buses .....	41
3.1.1	Target Bus .....	41
3.1.2	Initiator Bus .....	44
3.2	Atomisers .....	46
3.2.1	Limitations .....	47
3.3	Protocol Shells .....	47
3.3.1	Limitations .....	49
3.4	Clock Domain Crossings .....	49
3.5	Network Interfaces .....	50
3.5.1	Architecture .....	51
3.5.2	Experimental Results .....	54
3.5.3	Limitations .....	55
3.6	Routers .....	56
3.6.1	Experimental Results .....	58
3.6.2	Limitations .....	60
3.7	Mesochronous Links .....	60
3.7.1	Experimental Results .....	62
3.7.2	Limitations .....	62
3.8	Control Infrastructure .....	62
3.8.1	Unified Control and Data .....	63
3.8.2	Architectural Components .....	64
3.8.3	Limitations .....	67
3.9	Conclusions .....	67
<b>4</b>	<b>Allocation .....</b>	<b>69</b>
4.1	Sharing Slots .....	73
4.2	Problem Formulation .....	76
4.2.1	Application Specification .....	76
4.2.2	Network Topology Specification .....	79
4.2.3	Allocation Specification .....	81
4.2.4	Residual Resource Specification .....	82

4.3	Allocation Algorithm .....	84
4.3.1	Channel Traversal Order .....	85
4.3.2	Speculative Reservation .....	86
4.3.3	Path Selection .....	89
4.3.4	Refinement of Mapping .....	93
4.3.5	Slot Allocation .....	93
4.3.6	Resource Reservation .....	97
4.3.7	Limitations .....	98
4.4	Experimental Results .....	99
4.5	Conclusions .....	101
<b>5</b>	<b>Instantiation .....</b>	<b>103</b>
5.1	Hardware .....	104
5.1.1	SystemC Model .....	105
5.1.2	RTL Implementation .....	106
5.2	Allocations .....	107
5.3	Run-Time Library .....	108
5.3.1	Initialisation .....	109
5.3.2	Opening a Connection .....	111
5.3.3	Closing a Connection .....	113
5.3.4	Temporal Bounds .....	115
5.4	Experimental Results .....	115
5.4.1	Setup Time .....	116
5.4.2	Memory Requirements .....	117
5.4.3	Tear-Down Time .....	118
5.5	Conclusions .....	119
<b>6</b>	<b>Verification .....</b>	<b>121</b>
6.1	Problem Formulation .....	124
6.1.1	Cyclo-static Dataflow (CSDF) Graphs .....	125
6.1.2	Buffer Capacity Computation .....	127
6.2	Network Requirements .....	128
6.3	Network Behaviour .....	129
6.3.1	Slot Table Injection .....	129
6.3.2	Header Insertion .....	130
6.3.3	Path Latency .....	131
6.3.4	Return of Credits .....	131
6.4	Channel Model .....	132
6.4.1	Fixed Latency .....	132
6.4.2	Split Latency and Rate .....	134
6.4.3	Split Data and Credits .....	134
6.4.4	Final Model .....	134
6.4.5	Shell Model .....	135
6.5	Buffer Sizing .....	135

6.5.1	Modelling the Application .....	136
6.5.2	Synthetic Benchmarks .....	137
6.5.3	Mobile Phone SoC .....	139
6.5.4	Set-Top Box SoC .....	139
6.6	Conclusions .....	140
<b>7</b>	<b>FPGA Case Study .....</b>	<b>143</b>
7.1	Hardware Platform .....	144
7.1.1	Host Tile .....	145
7.1.2	Processor Tiles .....	146
7.2	Software Platform .....	147
7.2.1	Application Middleware .....	147
7.2.2	Design Flow .....	148
7.3	Application Mapping .....	149
7.4	Performance Verification .....	151
7.4.1	Soft Real-Time .....	151
7.4.2	Firm Real-Time .....	152
7.5	Conclusions .....	154
<b>8</b>	<b>ASIC Case Study .....</b>	<b>157</b>
8.1	Digital TV .....	157
8.1.1	Experimental Results .....	159
8.1.2	Scalability Analysis .....	162
8.2	Automotive Radio .....	165
8.2.1	Experimental Results .....	166
8.2.2	Scalability Analysis .....	167
8.3	Conclusions .....	168
<b>9</b>	<b>Related Work .....</b>	<b>171</b>
9.1	Scalability .....	171
9.1.1	Physical Scalability .....	171
9.1.2	Architectural Scalability .....	172
9.2	Diversity .....	173
9.3	Composability .....	174
9.3.1	Level of Composability .....	175
9.3.2	Enforcement Mechanism .....	175
9.3.3	Interference .....	176
9.4	Predictability .....	177
9.4.1	Enforcement Mechanism .....	177
9.4.2	Resource Allocation .....	177
9.4.3	Analysis Method .....	178
9.5	Reconfigurability .....	178
9.6	Automation .....	179

<b>10</b>	<b>Conclusions and Future Work</b>	181
10.1	Conclusions	181
10.2	Future Work	183
<b>A</b>	<b>Example Specification</b>	185
A.1	Architecture	186
A.2	Communication	187
	<b>References</b>	191
	<b>Glossary</b>	201
	<b>Index</b>	205



<http://www.springer.com/978-1-4419-6496-0>

On-Chip Interconnect with aelite  
Composable and Predictable Systems  
Hansson, A.; Goossens, K.  
2011, X, 210 p., Hardcover  
ISBN: 978-1-4419-6496-0