

Preface

Analog components appear on 75% of all chips, and cause 40% of the design effort and 50% of the design errors detected after first silicon measurements, reported *EDA Weekly* on March 21, 2005. Due to increasing functional complexity of system-on-chips, the difficulties in analog design and the lack of design automation support for analog circuits continually increase the bottleneck character of analog components in chip design. Design methodology and design automation for analog circuits therefore is a crucial problem for future system-on-chips.

Eminently critical is the layout synthesis part of the analog design flow. Although there have been a lot of very good works from universities over the years, some of which even found their way to commercial EDA tools, industrial application of analog layout synthesis is still in its infancy when it is compared to its digital counterpart! The industrial point of view even says that practicable EDA tools for analog layout synthesis did not exist.

But it seems that this situation is about to change. In the face of increasing circuit complexity and high performance SoC designs, the once-sleepy analog EDA market is experiencing an increasing shift from single vendor solutions to design tool integration via alliances between many players. The attempt to create an inter-platform reference, such as the Interoperable PDK Libraries (IPL) alliance, where analog layouts made with a tool can be imported error-free to different frameworks, is an example. Many EDA start-ups as well as major leaders are already announcing key automated layout tools for the analog designer intended to boost his/her productivity.

In this exciting scenario, academia continues to strive for new, more efficient, and complementary approaches to this task and to the existing tools, and has recently produced some very interesting new solutions. The intention of this book has two parts. On the one hand, it summarizes and presents these latest results. On the other hand, it is dedicated to give an introduction to advanced analog layout methods on the graduate level.

The book is structured in three parts. The first part with three chapters covers recent approaches to topological placement of analog circuits. The second part treats the problem of routing. The third part with three more chapters deals with layout in the design flow, namely, with the problem of retargeting an existing layout for a new technology, with integrating layout in the sizing process, and with constraint management in the design flow.

The first chapter starts with an introduction to the different ways of approaching in CAD tools device-level placement problems for analog layout. It is elaborated how the structural representation of the layout in the algorithm is crucial for the efficiency and efficacy of the placement process. Besides the classical way of using absolute coordinates for the module placement and slicing structures for topological representations, which encode the relative positioning between cells, it describes how the sequence-pair and tree-based topological representation can be applied to dramatically reduce the search space to the tiny fraction, which satisfies the inherent symmetry constraints in analog circuits. It further develops sufficient conditions to ensure the symmetry constraints during the successive moves of a placement algorithm and, based on these ideas, presents several topological algorithms that perform the exploration process very efficiently.

The second chapter furthers the ideas presented in the first chapter and extends them to a hierarchical module clustering. The analog devices can be hierarchically clustered into groups according to models, circuit functionalities, or signal/current flows. Following the B*-tree, a hierarchical B*-tree (HB*-tree) placement representation is developed to model this circuit hierarchy and symmetry and proximity constraints among modules and across the hierarchy. This hierarchical representation is fed into a placement algorithm to generate optimum device placements that meet all device layout constraints. Performing a simulated annealing algorithm, the placement of the device modules in different device groups belonging to different clustering hierarchies is simultaneously optimized.

The third chapter first introduces a method to automatically derive the circuit hierarchy and the resulting symmetry, proximity, and matching constraints from a netlist. A deterministic algorithm is then presented that computes the shape function of different aspect ratios of the circuit placement by a recursive bottom-up approach through the derived circuit hierarchy starting from basic modules such as current mirrors or differential pairs. For each hierarchy level, the shape function is determined by combining the placements of the next-lower hierarchy. These are stored as so-called enhanced shape functions that include the corresponding B*-trees of each individual shape. Algorithms are proposed to generate the vertical and horizontal sum of two B*-Trees of placements while provably complying with the constraints. As the algorithm bounds the enumeration according to the circuit hierarchy and the constraints, it generates results very fast, while being deterministic without any tuning parameter.

The second part of the book deals with analog routing. It gives a tutorial on routing methods and corresponding placement and routing representations, including constraints, for instance, for symmetry or crosstalk. A review of different routing strategies and the corresponding state of the art follows. Early routing approaches inspired from digital design, cost-driven approaches, and parasitic-driven approaches (including, e.g., performance sensitivities), as well as the A* algorithm are covered. The connection to placement through templates and other integration approaches is discussed afterward. Then, the partitioning of routing into global and detailed routing, as in digital design, is described. The chapter concludes with specialized routing approaches for RF circuits and analog arrays.

The third part of the book addresses analog layout issues arising from the ambient design flow.

In Chap. 5, the task of retargeting an existing layout, including placement and routing, is examined. Specific algorithms for layout retargeting may be beneficial if the involved layout modifications are moderate or to extract and conserve the knowledge contained in a layout. After a short introduction to the preparatory steps of layer mapping, constraint generation and device recognition, the main algorithmic step of retargeting, i.e., layout compaction, is described in detail. Based on the linear programming approach to its solution, a graph-based simplex method is presented with full details. The different types of constraints, the complexity of the algorithm, and practical issues are discussed as well.

Chapter 6 is dedicated to the problem of integrating layout effects into the circuit sizing process, to avoid unnecessary iterations between electrical and physical synthesis as much as possible. This has been called parasitic-aware synthesis. This chapter reaches from the very basics (what is it, and why and when is it really necessary) to a practical implementation of this type of synthesis process. Different methods to carry it out as well as their pros, cons, and trade-offs (mainly efficiency vs. completion time) will be explained. A technique will be presented that uses a combination of simulation-based optimization, procedural layout generation, exhaustive geometric evaluation algorithms, and several mechanisms for parasitic estimation, to comprehensively incorporate the layout-induced parasitic into electrical synthesis.

Chapter 7 concludes the book with a discussion of the management of the crucial factor in analog layout — the constraints. It provides a problem formulation for the classification, representation, transformation, and verification of constraints in a top-down design flow, as well as a formulation of a constraint engineering system, including its impact on the design flow and its algorithms.

This bow from placement to routing to the design flow, drawn by the structure of the book, invites the reader to start from the beginning and read one chapter after the other. At the same time, the chapters are self-contained and may be accessed individually and independently. In any way she or he approaches the book, the reader will gain a deep insight into the tasks of analog layout and into the actual solution approaches.

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