Preface

In the early computer era, unreliable components made fault-tolerant computer design mandatory. Dramatic reliability gains in the VLSI era restricted the use of fault-tolerant design in critical applications and hostile environments. However, as we are approaching the ultimate limits of silicon-based CMOS technologies, these trends have been reversed. Drastic device shrinking, very low operating voltages, increasing complexities, and high speeds made circuits increasingly sensitive to various kinds of failures. Due to these trends, soft errors, considered in the past as a concern for space applications, became during the past few years a major source of system failures of electronic products even at ground level. Consequently, soft-error mitigation is becoming mandatory for an increasing number of application domains, including networking, servers, avionics, medical, and automotive electronics. To tackle this problem, chip and system designers may benefit from several decades of soft error related R&D from the military and space. However, as ground-level applications concern high-volume production and impose stringent cost and power dissipation constraints, process-based and massive-redundancy-based approaches used in military and space applications are not suitable in these markets.

Significant efforts have therefore been made during the recent years in order to benefit from the fundamental knowledge and engineering solutions developed in the past and at the same time develop new solutions and tools for supporting the constraints of ground-level applications. After design for test (DFT), design for manufacturability (DFM), and design for yield (DFY), the design for reliability (DFR) paradigm is gaining importance starting with design for soft error mitigation. Dealing with soft errors is a complex task that may involve high area and power penalties, as copying with failures occurring randomly during system operation may require significant amounts of redundancy. As a consequence, a compendium of approaches is needed for achieving product reliability requirements at low area and power penalties. Such approaches include:

- Test standards for characterizing the soft-error rate (SER) of the final product and of circuit prototypes in the terrestrial environment. Such standards are mandatory for guarantying the accuracy of test results and for having a common

reference when comparing the SER, measured in terms of Failure in Time (FIT), of devices provided by different suppliers.

- SER-accelerated testing platforms, approaches, and algorithms for different devices, including SRAMs, DRAMs, TCAMs, FPGAs, processors, SoCs, and complete systems.
- SER-accelerated testing platforms, approaches, and algorithms for cell libraries.
- Software/hardware methodologies and tools for evaluating SER during the design phase. Such tools become increasingly important for two major reasons. Characterizing SER during the design phase is the only way for avoiding bad surprises when the circuit prototype or the final product is tested, which could lead to extra design and fabrication cycles and loss of market opportunities. Interactive SER estimation during the design cycle is the only way for making the necessary tradeoffs, determining the circuit critical parts and selecting the most efficient mitigation approaches for meeting a reliability target at minimal cost in terms of power, speed, and area. Software and hardware tools at various levels are required such as:
  - TCAD tools for characterizing the transient current pulses produced by alpha particles and secondary particles.
  - Cell FIT estimation tools to guide the designers of memory cells and cell libraries for meeting their SER budget at minimal cost, and for providing the cell FIT to the higher level SER estimation tools.
  - Spice-level FIT estimation, usually for evaluating the impact of transient pulses in sequential cells and in combinational logic.
  - Gate-level FIT estimation tools for characterizing IP blocks: based on exact, statistical or probabilistic approaches; considering the logic function only (for logic derating computation) or both the logic function and the SDF files (for combined logic and time derating computation).
  - RTL FIT estimation.
  - SoC FIT estimation, for taking into account the functional derating at the SoC level.
  - Fault injection in hardware platforms for accelerating the FIT estimation task at IP level and SoC level.
- Soft-error mitigation approaches at hardware level including: error detecting and correcting codes, hardened cells, self-checking circuits, double sampling approaches, instruction-level retry.
- Soft-error mitigation approaches at software level, operating system level, as well as check-pointing and rollback recovery.

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