Chapter 2
Single Event Effects: Mechanisms and Classification

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Single Event Effects (SEEs) induced by heavy ions, protons, and neutrons become an increasing limitation of the reliability of electronic components, circuits, and systems, and have stimulated abundant past and undergoing work for improving our understanding and developing mitigation techniques. Therefore, compiling the knowledge cumulated in an abundant literature, and reporting the open issues and ongoing efforts, is a challenging task. Such a tentative should start by discussing the fundamental aspects of SEEs before reviewing the different steps that are necessary for creating comprehensive prediction models and developing efficient mitigation techniques.

SEE occurs when the charge resulting from the carriers (holes and electrons) liberated by an ionizing particle (heavy ion, alpha particle, recoils of nuclear interaction between a neutron and an atom of the die, ...), and collected at a junction or contact, is greater than the charge carrying an elementary information in the component.

One way to understand the effects is to use a top-down approach to describe the successive steps involved in the perturbation mechanism:

- Interaction of radiation with matter
- Ionization mechanisms and track structure
- Collection of charges
- Description and calculation of effects on semiconductor structure (junction, device)
- Description and calculation of effects on semiconductor circuits and systems

The main difficulty is that each step is situated in a different physical/description domain and involves different people with different skills (nuclear and solid state physicists, process engineers, circuit designers, system engineers...). So bridges

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between these domains must be built to allow an efficient collaboration between the experts mastering them.

This chapter presents a review of the main aspects of SEEs on digital electronics. Analog and power electronics are not considered in this chapter.

2.1 Introduction

Single Event Effects (SEEs) are induced by the interaction of an ionizing particle with electronic components. Ionizing particles can be primary (such as heavy ions in space environment or alpha particles produced by radioactive isotopes contained in the die or its packaging), or secondary (recoils) created by the nuclear interaction of a particle, like a neutron or a proton with silicon, oxygen or any other atom of the die. SEEs become possible when the collected fraction of the charge liberated by the ionizing particle is larger than the electric charge stored on a sensitive node. A sensitive node is defined as a node in a circuit whose electrical potential can be modified by internal injection or collection of electrical charges. Usually, an information bit is associated with a voltage level.

Today, these effects are considered as an important challenge, which is strongly limiting the reliability and availability of electronic systems, and have motivated abundant research and development efforts in both the industry and academia.

These studies involve a broad domain of physics such as natural radiation environment modeling, radiation interaction mechanisms, ion energy depositions in insulators and semiconductors, charge transport and collection in elementary semiconductor devices such as PN junctions or elementary MOS transistors. The studies involve also electronic engineers that analyze perturbation mechanisms and effects in various cells (gates, flip-flops, registers, and memory cells), perturbation effects in complex integrated circuits with the possibility of multiple errors and single event functional interrupt (SEFI).

Designers must also consider analog components either CMOS or Bipolar that can also be upset (operational amplifiers, regulators, comparators, oscillators).

Finally, system level engineers must investigate the global effects of single events on electronic systems and develop mitigation techniques and test methods to establish and verify the robustness of these systems.

The aim of this chapter is to describe the physical mechanisms that induce SEEs and to define and classify the different ways they alter circuit operation. A top-down presentation will be given from environment to effects in complex function.

First, the natural radiation environment at ground level and in the atmosphere will be quickly recalled. A recall of nuclear physics, interaction mechanisms, and energy deposition, is given.

Then, solid-state physics and semiconductor physics are considered in order to develop transient photocurrent models related to the collection of carriers in junctions.

Finally, the effects observed in electronic devices will be defined and classified.

2.2 Background on Environment, Interaction Mechanisms, and Recoil Energy Loss

2.2.1 Natural Radiation Environment

At high altitudes in the atmosphere and at ground level, nuclear radiation can be found within a broad domain of energies. This radiation includes primary radiation from galactic or extragalactic origin with a low flux and secondary radiation resulting from the interaction of the primary radiation with the atmosphere content (nitrogen, oxygen, carbon dioxide, rare gas).

When galactic cosmic ray (GCR) particles reach the earth's atmosphere, they collide with the nuclei of nitrogen and oxygen atoms and create cascades of secondary radiation of different kinds, including leptons, photons, and hadrons.

At the time of writing this book, the neutrons are considered as the most important source of radiation as far as SEEs are considered. Nevertheless, we must also remember that protons and pions can also induce SEEs, and direct ionization of protons may be a concern in future electronics as circuits are further shrinking and become increasingly sensitive to SEE.

The flux of neutrons varies with altitude (the atmosphere attenuates both the cosmic rays and the neutron flux), latitude (due to the variation of the earth's magnetic field shielding efficiency from equator to the poles), and to a lesser extent with longitude. The flux of neutrons can be modulated by solar activity and solar eruptions.

Recently, analytical models describing these variations have been presented in Jedec JESD89A [1] and discussed in Chap. 3.

Measurements have been performed using different monitors or spectrometers.

The energy spectrum is generally considered to be independent of altitude. It extends from thermal energies up to 10 GeV. In first approximation, the differential energy spectrum $\mathrm{d}n/\mathrm{d}E$ can be considered to be proportional to $1/E$. This means that we get about the same number of neutrons in the energy range 1–10 MeV, 10–100 MeV, and 100 MeV–1 GeV. For $E > 1$ GeV, the slope $\mathrm{d}n/\mathrm{d}E$ can be considered with a good approximation to be proportional to E^{-2}.

More precisely, the neutron spectrum has three major peaks, thermal energy peak, evaporation peak around 1 MeV, and cascade peak around 100 MeV.

More information on the shape of the spectrum can be found in [2, 3]. The recently developed QARM model is described in [4].

The reference flux is taken at New York City at sea level [1] to be 13 n/cm^2 for $E > 10$ MeV. More details are given in Chap. 3.

An other important contribution to soft errors comes from alpha particles (helium nucleus built with two neutrons and two protons) emitted by radioactive elements found at trace levels in different materials close to the sensitive nodes of the electronic devices. These alpha emitters are elements from the three natural decay chains called Thorium, Radium, and Actinium decay chains. Secular

equilibrium[1] is sometimes assumed, but this hypothesis may not apply in practical cases if purification methods are applied to eliminate some elements in the radioactive chain. The energy of alpha particles is in a domain between 3 MeV and 9 MeV. Alpha emitters from the Thorium decay chain are given in the following table.

Elements	232Th	228Th	224Ra	220Rn	216Po	212Bi	212Po
Energy (MeV)	4.08	5.52	5.79	6.40	6.91	6.21	8.95
Half lifetime	1.410^{10} years	6.75 years	3.63 days	55.6 s	0.145 s	60.55 mn	299 ns

Important efforts are involved in reducing the impurities concentration and characterizing the alpha emission rate from materials used in packaging. Alpha sensitivity is calculated for a flux of 10^{-3} alpha/cm^2/h.

2.2.2 *Neutron Interaction with Matter: Production of Energetic Recoils*

Neutrons can interact with the nucleus either by elastic and nonelastic interaction and give a part of its energy as kinetic energy to the recoils. In some materials such as ^{10}B low energy neutron capture will give an exoenergetic reaction, but generally energy is either conserved (elastic collisions) or a fraction of it is changed in mass so that the total kinetic energy of the recoils is lower than the kinetic energy of the incident neutron.

2.2.2.1 Interaction Probability

The interaction probability per nucleus is given by the cross-section expressed usually in barn/nucleus. The cross-section is the effective area of the nucleus for interaction with a neutron. One barn equals 10^{-24} cm^2. In silicon, the total neutron cross-section decreases from 1.95 barn at $E = 40$ MeV–0.6 barn at $E = 200$ MeV.

To obtain the mean free path without interaction of neutrons in silicon, the number n of nucleus per cm^3 is first calculated. By considering the density d in g/cm^3, the atomic mass 28 g of 1 Avogadro of nucleus $d = 2.33$ g/cm^3, and the Avogadro number $N = 6.02 \times 10^{23}$, we find $n = 6.02 \times 10^{23}/(28/2.33) = 5 \times 10^{22}$ A/cm^3.

For an interaction cross-section value of one barn the mean free-range is:

$$1/\left(10^{-24} \times 510^{22}\right) = 20\,\text{cm}.$$

[1]The state where the quantity of a radioactive isotope remains constant because its production rate (due, e.g., to decay of a parent isotope) is equal to its decay rate.

So, as it is well known, neutrons can cross an important thickness of matter without interacting. The cross-section of interaction of one neutron with an energy of about 100 MeV (with $\sigma = 1$ barn), in a small cube with a side of 1 μm is then:

$$V \times n \times \sigma = 10^{-12} \times 510^{22} \times 10^{-24} = 510^{-14}\,\mathrm{cm}^2.$$

This value gives the order of magnitude of the upset cross-section per bit that will be obtained for SEU in SRAMs.

Because silicon is the main constituent of electronic devices, we can consider that silicon is the main target material. But for more accurate estimations, we need to take into account all the materials that may exist in the structure of an electronic device. As it is discussed later, we need to consider all the recoils that may come close to or pass through a sensitive node. These recoils must be produced at a distance from the sensitive node that is lower than their range.

2.2.2.2 Elastic Interaction

In the elastic process, the recoil nucleus is identical to the target nucleus. In the collision, the total kinetic energy and the momentum of the neutron-target nucleus system are conserved. A fraction of the energy of the neutron is given to the nucleus. The maximum energy that can be given to the recoil is:

$$E_{\max} = 4 \times E \times \frac{A}{(A+1)^2},$$

where A is the atomic number of the target nucleus. The probability to give a given energy between 0 and $E_{\max}$ is obtained by the differential elastic cross-section.

Most of the silicon recoils produced by elastic collisions have a low energy. For example, with an initial neutron energy $E_n = 125$ MeV, only 5% of the interactions give a recoil with energy larger than 0.27 MeV and 0.1% give a recoil energy larger than 1.5 MeV.

2.2.2.3 Nonelastic Interaction

Nonelastic interactions group all the interactions that result in a fragmentation of the nucleus in two or more recoil fragments. Generally, the lighter recoil is indicated to describe the reaction: (n,p), (n,α), (n,d). The heavier element is obtained by the equilibrium of the number of neutrons and protons before and after the reaction. With ^{28}Si as the target nucleus, (n,p) reaction results in a proton and Al recoil, (n,α) reaction results in He and Mg recoils.

The incident energy of the neutron diminished by the mass variation is shared between the secondary particles and the main recoil nucleus. These reactions require that the incident neutron energy is larger than the threshold energy of

each reaction. For a given neutron energy, different reactions are possible but their relative probability varies with the neutron energy.

2.2.2.4 Inelastic Collision: (n,n′)

In this reaction, the incident neutron is absorbed in the target nucleus and a short time later a neutron is ejected with a lower energy, sharing a part of the total kinetic energy with the recoil target nucleus. The emission is considered to be isotropic.

Most of recoils with $E_r > 2$ MeV come from nonelastic collision as shown by Chadwick [5, 6].

2.2.2.5 Pion Creation

Above about 250 MeV, neutrons can interact directly with nucleons in the silicon nucleus to form pions. Charged pions lose energy through ionization and by reacting with additional silicon nuclei or decaying in about 10^{-28} s to form charged secondary particles that also deposit charge in the silicon.

When more than two fragments are created, the repartition of energies and angles can be difficult to evaluate (multibody reactions). More details are given in Chap. 4.

2.2.2.6 Nuclear Data Base

The atmospheric neutron energy spectrum covers a broad energy range from meV (10^{-3} eV) to 10 GeV. A detailed knowledge of the recoil products is needed to calculate the range and density of ionization. So the energy spectrum is divided in different energy bins. For each neutron energy, the distribution of the nature and the energy of the different recoils are calculated.

In this way, a database is built to allow further use by Monte–Carlo Sampling in this distribution.

To build the database, a Monte–Carlo interaction code is needed. These codes must calculate the energy and direction of all the recoils. Wrobel [7] has developed the code MC-RED to develop such a data base. Chadwick [5, 6] has performed the extension of MCNP code previously limited to 20–150 MeV.

Data bases must be built for all the materials that can be met in the vicinity of the sensitive node. In each SEEs prediction codes, the data base is one of the most important parts that define the precision of the prediction. Usually, Si and O target nucleus are considered, but W used in vias and Cu used in metalization layers are also considered.

Tukamoto [8] has detailed in such a way that database can be obtained in the full spectrum energy domain. He used the JENDL-3.3 library to obtain the double-differential cross-sections (DDXs) for light charged particles (p and α) and

all recoils(^{24,25}Mg, ^{27,28}Al, and ^{27,28}Si) in the n+ ^{28}Si reaction at energies between 2 and 20 MeV. The data for energies between 20 and 150 MeV were taken from the LA150 library [5, 6] in which the DDXs of all recoils are included. Tukamoto has calculated the cross-sections for energies above 150 MeV using the QMD code [9] plus statistical decay model (GEM [10]) calculation.

The total deposited energy, in terms of kinetic energy transferred to recoils, is also an important parameter. This term was considered initially in the Burst generation rate (BGR) method to predict the Soft Error Rate (SER) [11]. It represents a worst case approach for SER calculation because all the energy transferred to recoils is assumed to be transformed in ionization and totally collected at the sensitive node.

The energies of the recoils are for a large part lower than 5 MeV.

If for 100 MeV neutrons, ^{28}Si recoil due to nonelastic collision is considered, it can be shown that 90% of the silicon recoils have their energy lower than 2.5 MeV and 99% their energy lower than 5 MeV. But light particles such as He nucleus (Alpha particles) have a higher energy. For 100 MeV neutrons, 10% of recoils have their energy greater than 16 MeV, and 1% have their energy greater than 31 MeV.

For $E_n = 20$ MeV, the emitted recoils are separated in light recoils (protons (n,p), deutons (n,d), tritons(n,t), ^{3}He, ^{4}He (n,α)), and heavy recoils (^{21}Ne, ^{27}Al, ^{28}Al, ^{24}Mg, ^{25}Mg, ^{26}Mg, ^{28}Si, ^{24}Na). No recoils with $5 < A < 21$ are produced. For higher energies, most of the isotopes with A values from 1 to 28 are present.

The creation of a nuclear data base is one of the most important steps in establishing a prediction tool to calculate the sensitivity of devices.

The nuclear data base gives also the angle of emissions when multiple particles are generated in a single interaction. The energies and emission directions are correlated to the incident neutron energy and direction.

A complete nuclear data base would give information on recoils resulting from all the materials that are at a distance from the sensitive zone lower than the maximum range of the recoils.

In particular recoils from oxygen (in SiO_2), W used in plugs, Cu in metalization, and also high K dielectrics used in the gate of MOS transistors, must be considered. Their relative contribution to the SER of a device is related to the technology used (number and thickness of metalization levels, structure of the cells, ...).

One important problem is the way to use the important volume of data generated in the data base and to calculate the sensitivity of the devices.

2.2.3 *Recoils: Ionization and Ranges*

The different recoils produced in an interaction extend from proton or neutron to the nucleus of the target atom. Neutrons produced in the reaction are not considered since their probability of interaction in the vicinity of their creation is very small.

The ions lose their energy by coulomb interaction with the electrons of the target atoms and at the end of their range by elastic collisions with the atoms [48].

The energy loss as a function of energy is given by codes such as SRIM [12] or MSTAR [13].

The most important parameters are the total or projected range of the ion, the energy loss by unit length, the velocity of the ion and finally the transverse profile of the ionization density in the ion track.

The ion range will determine the volume around a sensitive node where a neutron interaction may create a recoil able to reach this node.

The energy loss per unit length gives the density of the electron-hole pairs that can be collected in the space-charge layer and diffusion length of a PN junction

The transverse profile of the track is to be compared to the junction width or the channel length of a device.

2.2.3.1 Ranges of Recoils

We must separate the light ions (alpha, protons) which have generally a higher energy and a very long range from the heaviest ions (Si, Al, Mg). Range of silicon recoils, in a silicon lattice, with an energy <10 MeV, calculated with SRIM2008 [12] is given below. For $E < 5$ MeV, the range is less than 3 µm.

This range is short but much larger than the dimensions of transistor dimensions in recent technology nodes so that even heavy recoils can reach several sensitive nodes (Fig. 2.1).

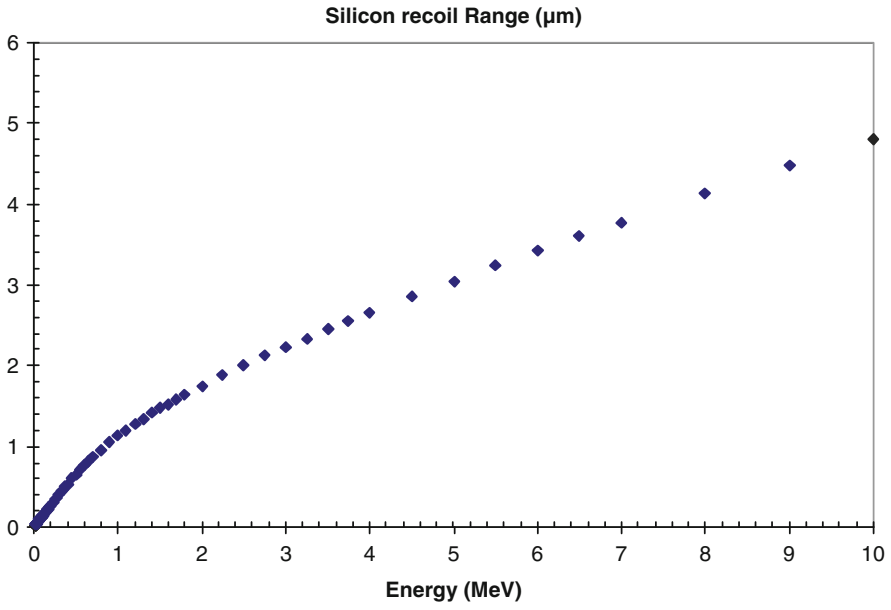

Fig. 2.1 Range of silicon recoil in a silicon lattice

2.2.3.2 Velocity of Ions

In the energy range of recoils produced by atmospheric neutrons, classical theory can apply and the velocity is related to energy by $v = \mathrm{SQRT}(2E/m)$ with $m = A \times \mathrm{AMU}$, A being the atomic number and AMU the Atomic Mass Unit.

1 AMU $= 1.66054 \times 10^{-27}$ Kg.

For 1 MeV Si ion, $v = 1.3$ μm/ps, and for 1 MeV alpha particle $v = 3.47$ μm/ps.

2.2.4 Ionization

Ionization is due to coulomb interaction with the electrons of silicon atoms of the recoil ions with effective charge Zeff. High energy electrons (δ rays) are created which lose their energy by further ionization or phonon excitation in times of 1–100 fs.

Finally, a mean of 3.6 eV (1 eV $= 10^{-19}$J) is needed to create a free hole-electron pair in silicon. The energy transfer (LET) is the energy deposited per unit length given in MeV $\times$ cm^2/mg, and describes the average energy loss by the ion per unit length of the transverse material. The LET can be converted in charge per unit length (pC/μm or fC/μm) to use units more convenient to the electronic designer because they can be compared to physical dimensions of the device and to the charge stored at critical nodes.

To perform this conversion, first the energy loss per unit length is calculated. In silicon (silicon density equals 2.32 g/cm^3), we have:

$$1\,\mathrm{MeV}/\mu\mathrm{m} = 4.31\,\mathrm{MeV}/\mathrm{mg}/\mathrm{cm}^2.$$

Then, substituting 1 MeV/mg/cm^2 by 10 fC/μm we obtain:

$$1\,\mathrm{MeV}/1.610^{-19} \times 10^6/3.6\mathrm{C}/\mu\mathrm{m} = 44\,\mathrm{fC}/\mu\mathrm{m}.$$

For each recoil, the LET varies with its energy. First, the LET increases with recoil energy until reaching a maximum called the *Bragg peak* and then decreases with increasing energy. For the different ions that may result from the spallation of silicon atoms, the highest LET is obtained for silicon which is the heaviest possible recoil in a silicon target. The max LET can reach 15 MeV/mg/cm^2 at the Bragg peak. This value is often used as a rough criteria to separate devices sensitive to neutrons (threshold LET < 15) from devices that are not sensitive (threshold LET > 15), by using heavy ions test results. But this approach can be in error if heavier recoils (from Cu metalization or W plugs) can reach the sensitive nodes (Fig. 2.2).

LET is an important parameter to quantify the sensitivity of devices.

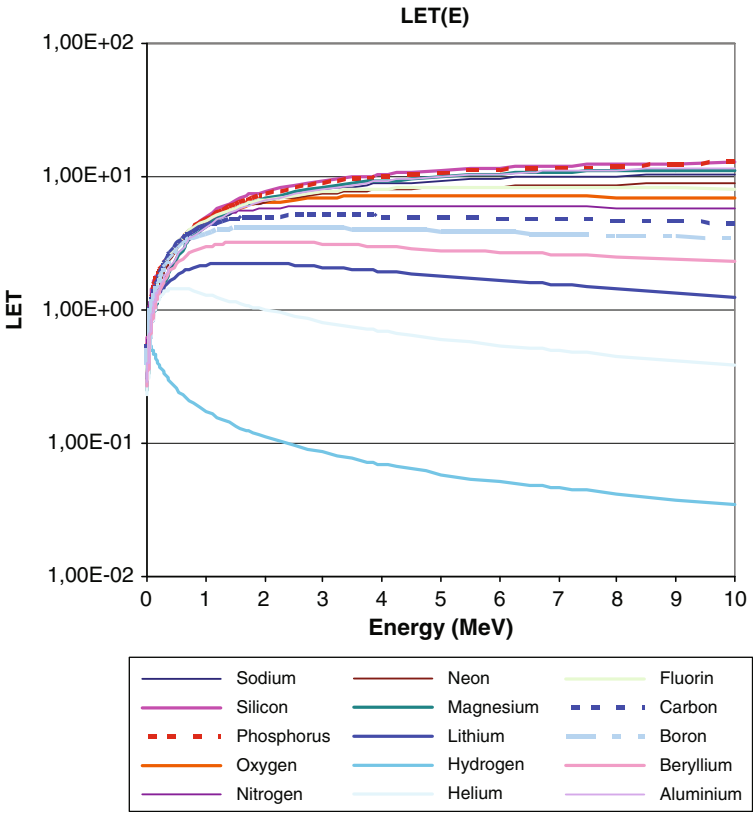

Fig. 2.2 LET(E) in MeV × cm^2/mg of recoils ($Z = 1, 15$) in silicon for $E < 10$ MeV

The range is related to the initial energy E and the LET by the relation:

$$R = \int_{E_{\max}}^{0} \frac{\mathrm{d}x}{\mathrm{d}E} \mathrm{d}E$$

When a recoil is created at a distance d from a sensitive node, the energy of the particle when it reaches the vicinity of the node is given by:

$$E_d = E_0 - \int_0^d \frac{\mathrm{d}E}{\mathrm{d}x} \mathrm{d}x$$

If the initial energy is greater than the Bragg peak energy, the LET increases along the track until the Bragg peak energy is reached and then decreases.

Table 2.1 Energy and LET at the Bragg peak for recoils with $Z = 1$–8

Element	H	He	Li	Be	B	C	N	O
Energy (MeV)	0.05	0.45	1.65	2	2.1	2.8	3.9	5
LET (MeV × cm^2/mg)	0.538	1.45	2.26	3.24	4.19	5.13	6.04	7.17
LET (fC/μm)	5.49	14.8	23.1	33.1	42.8	52.4	61.6	73.2

This effect can be important for protection layers against alpha particles. If the layer is not thick enough to stop the particle, the LET may be greater near a sensitive node than without protective layer.

The energy of different recoils at the Bragg peak in silicon and the associated LET are given in Table 2.1.

For protons (H nucleus), at the Bragg peak (situated at very low energy near 50 keV), the LET reaches 5.5 fC/μm. Then, it decreases rapidly to 2.6 fC/μm at 500 keV and 1.8 fC/μm at 1 MeV. So protons may contribute to upset by direct ionization at low energy when the collection length is greater enough (>200 nm) and when the critical charge is less than 1 fC. This point will be discussed for SRAM devices.

2.2.4.1 Track Diameter

The initial radial variation of electron-hole pair density along the ion track is an important input in the semiconductor-simulation codes to calculate the collected charge at the sensitive nodes. Generally, a Gaussian shape is assumed with an initial diameter that will broaden with time. In the past, when devices dimensions were in the micron range, the precise knowledge of the track diameter at $1/e^2$ value was not necessary. But with 60 nm or 45 nm design rules a precise knowledge of the radial variation becomes mandatory.

In a recent work, Murat et al. [14] use Monte–Carlo techniques to study ion transport and secondary electron transport up to a remaining kinetic energy of 1.5 eV (very close to the energy gap of 1.12 eV) but their work concerns high energies >10 MeV/AMU, that is >280 MeV for silicon recoils and > 40MeV for alpha particles. Kobayashi [15] performed similar calculations with the code GEANT4 but with a higher value for electron energy cut-off limit. Zhu [16] has found that the maximum range of secondary electrons (δ rays) is about 20 nm for 1.5 MeV alpha particles. More work is needed in this domain to accurately describe the ionization track from its creation to the first picoseconds.

2.2.4.2 Generation Time Profile

The generation of free carriers follows the ion penetration (at a velocity related to its energy and its mass), but sometimes it is considered as instantaneous with the implicit assumption that the response of the device is much slower than the carrier generation time. As shown by Zhu [16], this assumption must be verified and

eventually modified for low energy ions for recoils generated by ^{10}B fission with thermal neutrons.

2.2.5 Conclusion

Radiation is present in the natural environment. The flux of particles varies with altitude, latitude, and to a lesser extent with longitude. The particles have a broad energy spectrum and present several interaction mechanisms that result in energy deposition in the materials. Some impurities present in semiconductors or package materials are radioactive and emit alpha particles that can reach sensitive zones.

In electronic devices, single particles may deposit enough ionizing energy to upset components. To understand SEEs, the particle interaction mechanisms must be quantified and the recoils that are produced by the nuclear spallation reactions must be well identified by their nature, energy, and direction. The loss of energy of these recoils per unit length and the ionization density along the radius of the track are important input parameters for accurate modeling of SEEs.

2.3 Single Event Effects in Electronic Devices and Systems

2.3.1 Single Event Effects Definition

SEEs in Electronic Devices group all the possible effects induced by the interaction of one nuclear particle with electronic components.

These effects are classified in hard errors and soft errors as already presented in Chap. 1.

Hard errors are non-recoverable errors. Soft errors may be recovered by a reset, a power cycle or simply a rewrite of the information.

Hard errors concern Single Event Burnout (SEB) in power MOS, IGBT or power bipolar transistors, dielectric breakdown in gates (SEGR) or in capacitors, microdose-induced threshold voltage variation in MOS transistors.

These hard errors are not discussed in this chapter, but they represent also an important issue in SEEs. These effects were recently reviewed by Sexton [17].

Soft errors include a great variety of manifestations depending upon the device considered.

In analog devices, Single Event Transients (SETs) also called Analog Single Event Transients (ASETs) are mainly transient pulses in operational amplifiers, comparators or reference voltage circuits.

In combinatorial logic, SETs are transient pulses generated in a gate that may propagate in a combinatorial circuit path and eventually be latched in a storage cell (e.g., a latch or a flip-flop).

In memory devices, latches, and registers, single events are mainly called Single Event Upsets (SEU). This corresponds to a flip of the cell state. When for one

particle interaction many storage cells are upset, a Multi-Cell Upset (MCU) is obtained. If more than one bit in a word is upset by a single event, a (Multi-Bit Upset (MBU) is obtained.

For complex integrated circuits, loss of functionality due to perturbation of control registers or clocks is called SEFI. These SEFIs may give burst of errors or long duration loss of functionality. Functionality may be recovered either by a power cycle, a reset or a reload of a configuration register.

In bulk CMOS technology, PNPN parasitic structures may be triggered giving a Single Event Latch-up (SEL). SEL is associated with a strong increase of power supply current. SEL can be destructive by over heating of the structure and localized metal fusion. A SEL needs a power cycle to be deactivated.

2.3.2 Soft Error Rate

The SER is the rate at which soft errors appear in a device for a given environment.

When the particular environment is known or for a reference environment (NYC latitude at sea level), the SER rate can be given in FIT. In semiconductor memory, the sensitivity is often given in FIT/Mb or in FIT/device. One FIT (Failure In Time) is equal to a failure in 10^9 h.

The FIT value is either predicted by simulation or is the result of an experimental error measurement near a neutron generator representing as accurately as possible the real neutron energy spectrum.

The cross-section can be used to calculate SER. If, with a total fluence of N neutrons/cm^2, n errors are obtained in one device, the cross-section is $\sigma = n/N$. With ϕ the particle flux in the real environment, expressed in n/cm^2/h, the FIT value is: FIT value $= (n/N) \times \phi \times 10^9$.

With a cross-section of 5×10^{-14} cm^2 per bit, and $\phi = 13$ n/cm^2/h, the number of FIT/Mb is $5 \times 10^{-14} \times 10^6 \times 13 \times 10^9 = 650$ FIT.

2.3.3 Critical Charge Criteria

The sensitivity of a device must be described by a parameter that allows to simply evaluate the sort of recoils that can disturb the electronic function.

The simplest parameter to consider is the charge collected at a given node and to compare its value to the minimum charge needed to upset the function. This minimum charge is called the *critical charge*.

The simplest approach is to consider the critical charge as the product of the total capacity Ci at a given node by the power supply voltage Vdd: Qc = Ci × Vdd. This approach is very useful to obtain a rough estimation of the critical charge.

In this crude approximation, the collection of charges is considered as instantaneous and the rest of the circuit has no time to react. This approximation can be wrong in particular when carrier collection occurs by a diffusion process.

Considering an inverter, during the time of collection, the ON transistor delivers some current that partially compensates the collected current. This effect was first taken into account by Palau [18] to develop an enhanced model.

A more precise approach to obtain the critical charge is to use a circuit simulator such as SPICE Code and to describe the collected charge by a double exponential current generator of short duration applied at the sensitive node:

$$I_{\text{exp}} = \frac{Q_{\text{tot}}}{\tau_f - \tau_r} \times \left(\exp\left(-\frac{t}{\tau_f} \right) - \exp\left(-\frac{t}{\tau_r} \right) \right).$$

But this current pulse has peak amplitude independent of the voltage at the sensitive node and thus the free carrier collection and function of the voltage is not accurately described.

A best approach but much more complex and time consuming is to use a device simulator working either in full 3D for the complete circuit to be simulated (e.g., 6T SRAM cell) or mixed mode simulation with only one transistor described with a device simulator and the remaining transistors described with a circuit simulator.

These approaches to obtain the critical charge have been described in detail by Dodd [24, 19] and Yamagushi [20].

The charge is calculated by integration of the current pulse crossing the junction. The time limits for the integration are related to the circuit upset mode and the charge must be integrated to a time value that is either the recovery time (when no upset occurs) or the upset time when the device changes state.

The critical charge variation as a function of the time duration of the current pulse has been considered by Jain [21] for a rectangular waveform (Fig. 2.3).

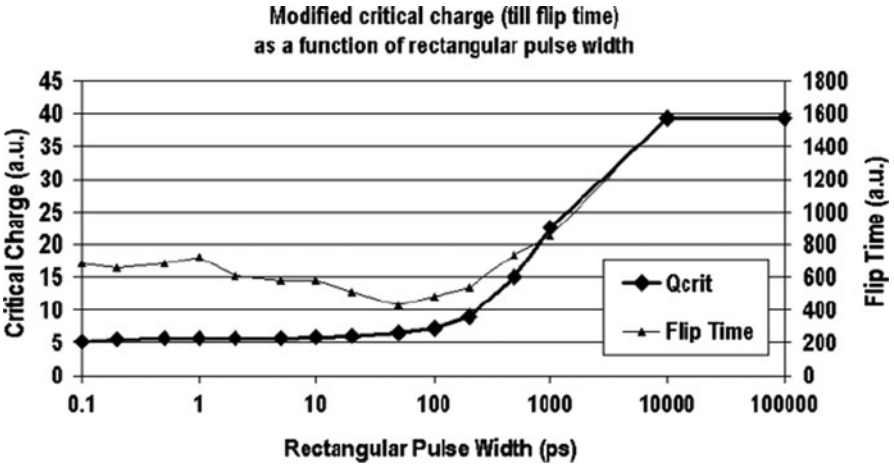

Fig. 2.3 From Jain [21] variation of the critical charge and the flip time as a function of pulse duration. For this particular technology node, the critical charge and flip time increase for $t > 100$ ps

2.3.3.1 Orders of Magnitude of Critical Charge

The total capacity at a given node is related to the technology. In CMOS technology, this capacity at the drain-substrate junction is the sum of gate-drain capacity and drain-substrate capacity. As will be seen later for SRAM devices, the critical charge is reduced to 1–2 fC in most recent technology nodes.

For DRAM and SDRAM, the critical charge remains roughly constant due to sense amplifier limits to 20–30 fC.

2.3.4 Description of Current Pulses for Circuit Simulation

A mathematical equation with a double exponential was given above to describe the waveform of the current pulse in circuit analysis codes. This waveform is arbitrary and mostly adapted to facilitate convergence in the codes. In practice, several waveforms can be obtained depending upon the location and length of the track.

The effects of the free carrier generation along the recoil(s) track(s) can be investigated by studying device response from the simple PN junction to complex devices response with device simulators.

In a PN Junction (such as drain-substrate or drain-well), the current pulse is due to separation of hole-electron pairs by the electric field of the space charge layer (drift component) and by the diffusion of minority carriers toward the space charge layer boundaries where they are accelerated by the electric field.

When the recoil track crosses the depletion layer, some field modification along the track may enhance the collection length by extending the space charge layer in the neutral zone. The so called *funneling effect* is only important for high LET and low doped neutral zones.

When the track does not cross the depletion layer, only diffusion process occurs and gives a slower current pulse. Diffusion is related to the gradient of carriers, and so diffusion of carriers is effective toward all the junctions for which the neutral zone where the track is located is one side of the junction. Analytical expressions of the diffusion component are detailed in Chap. 4.

During diffusion time, a fraction of the generated free carriers recombine before reaching the limits of space charge layers.

To perform a detailed calculation of the current pulse waveform a device simulator is needed. Presently, most of the device simulators use the conventional drift-diffusion equation but more complex treatment will be required in future devices as outlined by Munteanu [22].

The shape of the current pulse varies with the extent of funneling and diffusion present in the charge collection at any given junction.

A double exponential pulse shape is often used to fit the pulses with a characteristic rise time (about 1 ps) and a varying decay time. For example, Bajura [23] presents the comparison of current pulses obtained from 3D device simulation and

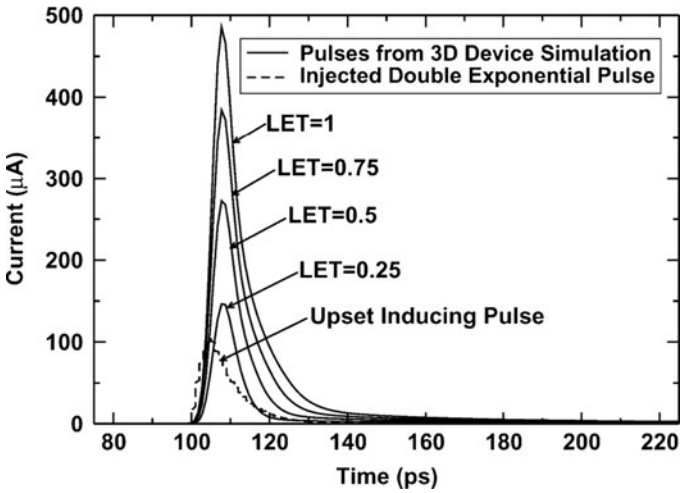

Fig. 2.4 Comparison of 3D simulation pulses with double exponential pulse (From Bajura [23])

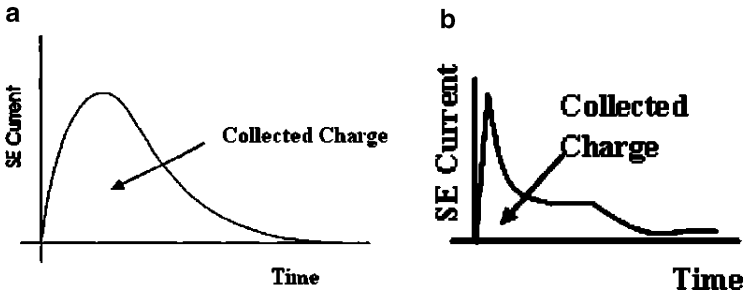

Fig. 2.5 Comparison of double exponential waveform with current waveforms obtained in 3D simulation. (After Dodd [24, 25])

the classical double exponential pulse injected at critical nodes in a 90 nm technology in the Off NMOS transistor (Fig. 2.4).

For older technologies, the charge collection was accurately modeled by a double exponential current waveform (Fig. 2.5a). However, for advanced technologies the current pulse shape becomes much more complex as shown in Fig. 2.5b, as discussed by Dodd [24, 25].

2.4 Sensitivity of Devices

The sensitivity of devices can be investigated by considering the effect of the ionization track on devices with increasing complexity. The simplest device is a reverse-bias PN junction. The current waveforms in PN junctions were discussed

previously. These junctions are often parasitic (drain-substrate, drain-well, well-substrate in bulk CMOS technology) that must be described accurately.

Due to the different locations of impact, track direction, track length, ionization density, and many waveform shapes are expected. So empirical models, taking into account these parameters, must be developed for a given technology, in order to allow the prediction of the behavior of the elementary logic functions such as combinational gates [26].

2.4.1 SET

DSETs (Digital SET) are momentary voltage or current disturbances affecting combinational gates. Although an SET does cause a transient in the gate output struck by the recoil ion, it may propagate through subsequent gates and eventually cause an SEU when it reaches a memory element. Dodd [25] recalls that at least four criteria must be met for a DSET to result in a circuit error.

- The particle strike must generate a transient capable of propagating through the circuit.
- There must be an open logic path through which the DSET can propagate to arrive at a latch or other memory element.
- The DSET must be of sufficient amplitude and duration to change the state of the latch or memory element.
- In synchronous logic, the DSET must arrive at the latch during the latching edge of the clock.

The probability that transient glitches will be captured as valid data in combinational logic increases linearly with frequency because the frequency of clock edges increases. As circuit speeds increase, it is also expected that the ability of a given transient to propagate increases (high speed means faster gates and/or less logic levels per pipeline stage); however, one might also conjecture that the duration of transients decreases. Due to both their greater ability to propagate in high-speed circuits and their higher probability of capture by subsequent storage elements, such as latches, DSETs have been predicted to become a very important issue in deep submicron digital ICs [27, 28].

Mixed-level simulations have been used to study the production and propagation of DSETs in scaled silicon CMOS digital logic circuits [25]. The modeling technique is illustrated in Fig. 2.6. In this figure, the production of SETs in the off-biased n-channel transistor in the struck CMOS inverter is modeled in the 3D device domain, and propagation through an ensuing ten-inverter delay chain is modeled in the circuit domain within the mixed-level simulator. Transients that can propagate without attenuation are obviously a concern, although it must be reminded that propagation of the DSET is only the first of a set of conditions that must be met for a DSET to become an SEU.

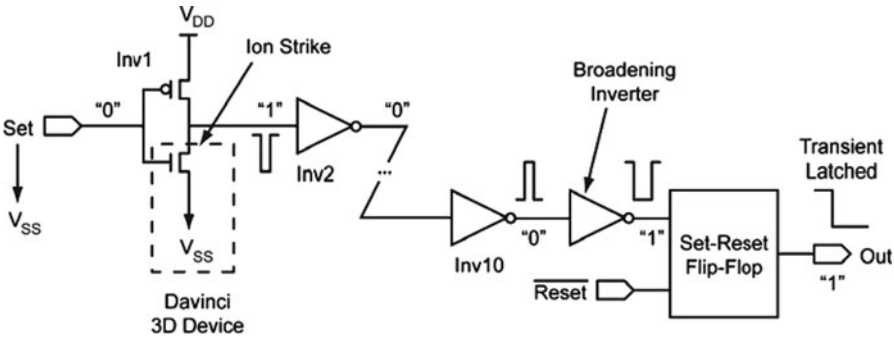

Fig. 2.6 Mixed mode simulation used to study SET propagation in an inverter chain (after Shuming [29])

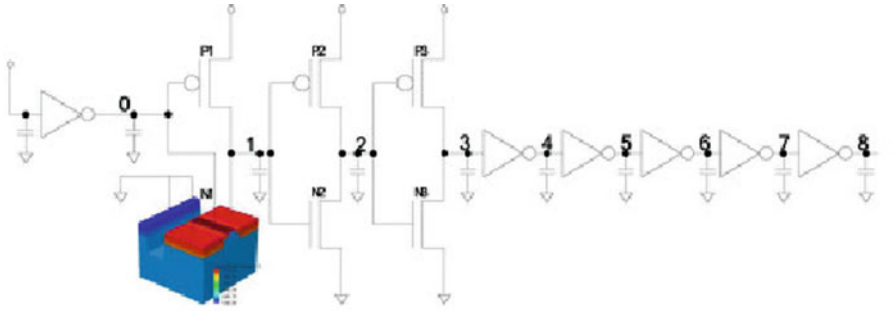

Fig. 2.7 An other example of mixed simulation used to study DSET propagation. Note that an inverter is placed before the inverter described with 3D simulation code (after Dodd [25])

An important advantage of 3D mixed-level simulations compared to circuit simulations is that they can directly predict the ion-induced transients in response to a given particle strike.

At the same time, the simulations calculate the propagation of the transient through the inverter delay chain.

Shuming [29] has investigated the temperature effects on SET in a chain of inverters in 180 nm bulk by using mixed simulation on the structure given below. Dodd [25] uses nearly the same approach. This approach can be used in all combinatorial logics with more complex gates (Fig. 2.7).

2.4.2 SEU

An SEU occurs when an ionizing particle strike modifies the electrical state of a storage cell, such that an error is produced when the cell is read. In an SRAM or

a flip-flop, the state of the memory is reversed. In a DRAM, the charge stored can be slightly modified and interpreted as a wrong value by the read circuitry. In logic circuits, SEUs can also be obtained when a SET propagates through the combinational logic and is captured by a latch or a flip-flop.

SEU is experimentally studied in memories or registers by writing a known content, irradiating the device at a given particle flux and recording the variation of the contents.

Different tests algorithms can be used from the simple write-irradiate-read called also static test to much more complex dynamic test sequences.

2.4.2.1 SRAM

In 6T SRAM cells with two coupled CMOS inverters and two NMOS access transistors, SEUs have been studied by means of full 3D simulations as well as mixed-mode simulations, in order to evaluate the critical charge needed to obtain an upset.

Bajura [23] has studied the minimal-sized SEU-inducing pulses, when applied to the drains of the "off" NMOS and "off" PMOS transistors. He has found a total integrated charge of 1.1 fC and 2.4 fC, respectively. He explains that the difference in minimum injected total charge required for a bit upset to occur is due to the design of the 6T cell. The cross-coupled inverters are highly asymmetric with the pull-down NMOS transistors having much stronger drive strength than the PMOS pull-ups. Under normal operating conditions, this asymmetric design improves the speed at which the SRAM can flip states.

The following figure illustrates the two cross-coupled inverters and the pulse current injected at the drain of the off NMOS in a circuit simulation (Fig. 2.8a, b).

The two inverters output are obtained for the two limiting ionization density just below the upset level and just above the upset level (Fig. 2.9).

On the one hand, critical charge of SRAM is decreasing in successive process nodes due to the shrink in dimensions and the decrease of the power supply voltage. But on the other hand, the area of elementary cells is also decreasing as indicated below (data presented by Bai et al. [30]), resulting in a compensation of the two effects. The decrease of the critical charge implies that an increasing number of interactions produce recoils that can induce SEU. It results that an increasing fraction of recoils becomes effective. For older technologies, only a small part of the reactions were efficient to give SEU, and so a strong increase of the sensitivity was obtained when the critical charge was decreasing for two successive technology nodes. For more recent technologies, the fraction of effective interactions reaches 90% so only a small effect of reduction of critical charge is expected in the future.

The diminution of the cell area will then be the dominant effect and a global reduction of the sensitivity per Mb is expected in the future. The sensitivity trends are more deeply discussed in Chap. 1 (Fig. 2.10).

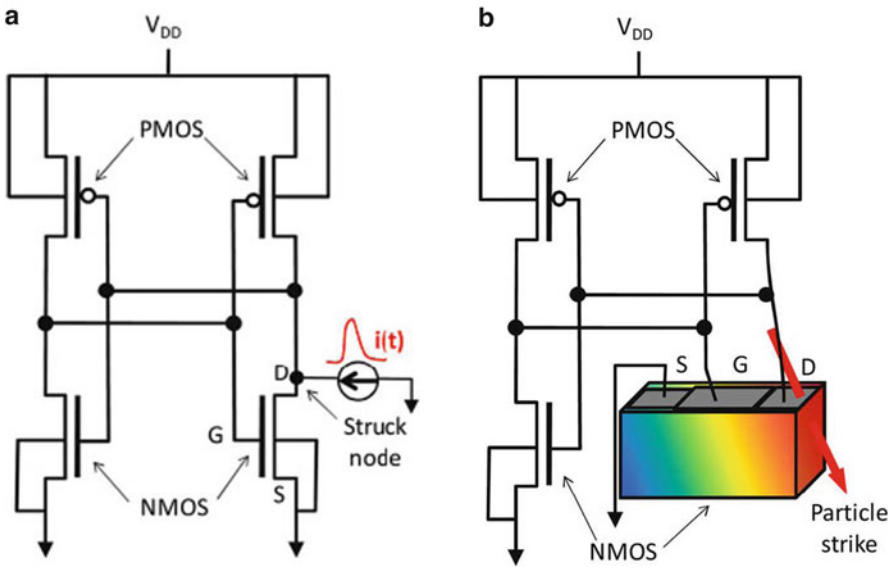

Fig. 2.8 (**a**) Schematic of two cross-coupled inverters in CMOS technology. A current pulse is injected at the drain of the off NMOS transistor. (**b**) Mixed Mode simulation is used to simulate SEU. The Off NMOS is studied by means of device simulation and the remaining transistors are studied with the coupled circuit simulator (after Munteanu [22])

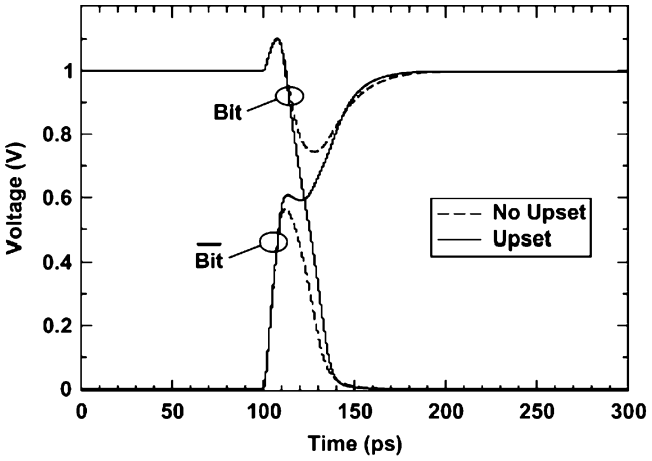

Fig. 2.9 Drain voltage waveforms for ionization density slightly lower (*no upset*) and slightly larger (*upset*) than the ionization upset threshold

2.4.2.2 Upset by Direct Proton Ionization

Low energy protons ($E < 1$MeV) have a LET that varies between 1.8 fC/μm at 1 MeV and 5.5 fC/μm at 50 keV. In SRAM with very low critical charge (<1 fC)

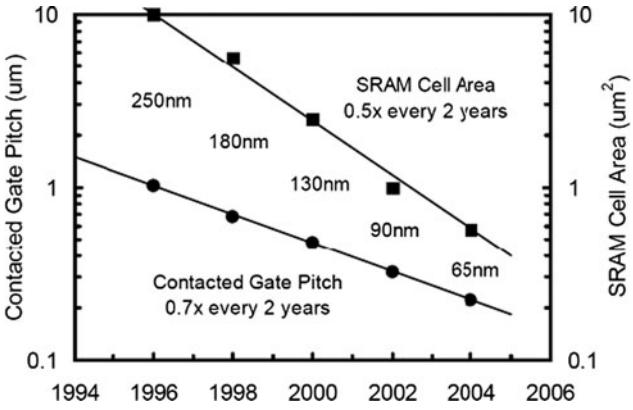

Fig. 2.10 From Bai [30]. SRAM cell areas and contact gate pitch decrease with each technology node. At 65 nm, cell area is about 0.6 μm^2

and for particular proton incident directions where the collection length is greater than 200 nm, upsets are expected. These upsets have recently been observed experimentally [45, 46] in 65 nm SOI SRAMs at high incidence angles.

2.4.2.3 DRAM and SDRAM

A DRAM cell consists of a capacitor and a transistor. The capacitor stores the bit of information, and the transistor isolates the capacitor during nonread or nonwrite times, which is approximately 99% of the time [32]. During this time, the cell experiences subthreshold leakage that causes the DRAM cell to lose its programmed state. Thus, the cell needs to be refreshed, i.e., rewritten, occasionally. During a READ operation, the word-line potential is raised to access the storage node. A sense amplifier compares the potential on the bit line to the potential of a reference bit line on the other side of the sense-amp, and the sense-amp latch sets depending on whether there charge stored in the capacitor exceeds a certain threshold. At the end of the operation, the bit is restored to the cell and the bit lines are charged up to a high level for the next cycle. The bit lines are then allowed to float, making them sensitive to charge collection about 99% of the time.

O'Gorman [33] reported soft errors at ground level in 288 k DRAM and clearly separated the contributions from alpha particles and neutrons.

The critical charge of the cell, defined as the minimum amount of charge that must be collected by the cell to cause a soft error, was in the range of about 70–100 fC.

Scheick [32] indicated that half of the cells have 0 charge on the capacitor when programmed to 1, while the other half have a charge stored when programmed to 1. Now, since a DRAM can only upset by discharge of the capacitor, a DRAM programmed with all ones or zeros will have about half of the cells vulnerable to SEU.

The DRAM vulnerability is related to the technology of the capacitor that stores the information (see Chap. 1).

As clearly indicated by Massengill [34], a degradation of the stored signal to a level outside the noise margin of the supporting circuitry is considered an upset, as it will lead to erroneous interpretation and a resultant error. In a DRAM cell, the current in the source of the NMOS transistor may discharge the capacitor.

In 1987, Hisamoto et al. [35] reported a direct source-drain penetration effect due to alpha-particle strikes in scaled (short channel MOS) DRAM structures. This alpha-particle induced source-drain penetration (ALPEN) effect causes current flow across the normally off access transistor, due to a source-drain shunt effect. While the normal SEE mechanism is to deplete charge from a DRAM cell storage capacitance, the ALPEN mechanism causes the opposite result: the shunting of charge onto the storage node. Thus, a $0 \rightarrow 1$ versus a $1 \rightarrow 0$ mechanism is introduced. In this early study, the ALPEN effect was found to be important for device gate lengths less than 0.3 μm.

2.4.3 MCU and MBU in SRAM and DRAM

SEU is a perturbation of one bit by a single particle. Single Error Correction Codes (ECC) such as Hamming codes that can detect two errors and correct one in a word can be used to mitigate these errors. But if two or more errors are present in a single word, a more elaborated and complex ECC is needed. Multiple errors can be created in devices when a particle crosses the sensitive zones of different cells (drains of blocked MOS transistors) or when the free carriers of the ion track can be collected by different junctions of transistors of several memory cells.

As the elementary cell area is continuously decreasing for successive technology nodes, the probability that recoils have a range long enough to reach different cells increases. So the probability of multiple cell upsets increases. This probability also increases due to an increasing charge sharing probability: neighbor circuit nodes in advanced technologies are closer to each other and can collect charges from a single particle track. The ratio of MCU to SEU and the probability to have a given number or errors in a MCU are important parameters because they allow to determine the efficiency of an ECC and to choose the most appropriate one for meeting the SER requirements of the target application. The geometrical repartition of bits in a word is also an important parameter for determining the fraction of the errors produced by an MCU that are located in the same word (MBU). In particular to avoid MBU, bits in same word are placed as far as possible one from each other by using appropriate scrambling in the memory design.

2.4.4 SEFI

SEFI is an anomalous behavior observed in complex devices. It can be the result of the upset of some registers or latches that are used in the configuration of the working modes of these complex devices.

Koga [36] was among the first to define SEFI from observations in SDRAM, EEPROMS, and microprocessors. Dodd [37] defines SEFI as a triggering of an IC test mode, a reset mode or some other mode that causes the IC to temporarily lose its functionality.

SEFIs were reported in flash nonvolatile memories, SDRAM, SRAM based FPGA, microprocessors, and microcontrollers.

2.4.4.1 SEFI in Flash Memories

Bagatin et al. [38] studied 1 Gb Nand Flash and could identify different SEFIs. They classify SEFI in different ways:

- SEFI that gives a full page or block read-errors and SEFI that slows down or disables the capability of the device to program and/or to erase.
- SEFI can be also classified depending on the way the functionality was restored after the event: a power cycle can be necessary or a reset command is sufficient, or a spontaneous recovery is observed.
- Supply current increase is also observed, and nominal value is restored by reset or by power cycle. In this latter case, SEFI is difficult to separate from SEL.

2.4.4.2 SEFI in FPGA

In SRAM based Field Programmable Arrays (FPGA), such as Virtex, George [39] expected to find SEFI due to upsets in particular circuits that involve Power-on-reset (POR), failures in the JTAG or Select-Map communications port or others.

2.4.4.3 SEFI in SDRAM

In SDRAM, the block diagram shows that mode registers, address registers, refresh counter, are used to control the device. A SEU in one of these registers may modify the refresh period, or induce other sorts of SEFI.

SEFI is a complex effect that needs a special treatment in a system. Fortunately, the cross-section is generally very low.

2.4.5 Single Event Latch-Up

SEL is related to the activity of parasitic structures in bulk CMOS technology. Some PNPN structures can switch from a high impedance state to a low impedance one. Latch-up can be induced also by electrical transients or by high dose rate X-ray

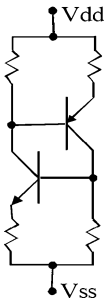

Fig. 2.11 Two bipolar transistors equivalent structure of a PNPN parasitic structure found in bulk CMOS technology

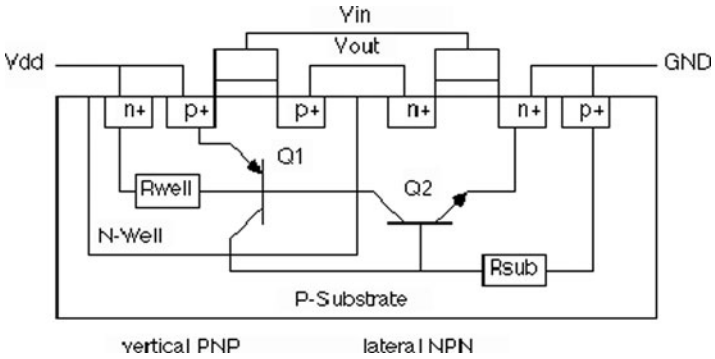

Fig. 2.12 PNPN parasitic structure in an N-Well bulk CMOS Inverter structure

pulse. The possibility of a PNPN structure to switch depends upon the following factors:

- Bias of the structure.
- Activity of the structure.
- Triggering energy delivered by the recoil.

The PNPN structure can be described by two cross-coupled bipolar transistors (one PNP and one NPN) as indicated in Fig. 2.11. Resistors are included in series with emitters and between base and emitters. In some equivalent schematics, resistors in series with collectors can be included.

The relation with the CMOS structure of an inverter in a CMOS bulk N Well Technology is given in Fig. 2.12 (after Puchner [40]).

The N-Well/P-Substrate junction is the base collector junction of both PNP and NPN junction. The emitter-base junctions are N+Source-PSubstrate and P+source-NWell junctions. The current gain of a bipolar transistor is related to the base width and the injection efficiency of the emitter-base junction. The base width varies with design rules and the position of the source relative to the Well-Substrate junction.

An ideal PNPN structure is active if the gain product of the NPN and PNP transistors is $\beta 1 \times \beta 2 > 1$, where $\beta 1$ and $\beta 2$ are the current gains Ic/Ib of the bipolar transistors.

Other important parameters that influence the sensitivity are the resistivity and depth of the well and the resistivity of the substrate. To reduce the base-emitter resistor a thin epitaxial layer on a high doped substrate can be used. Multiple substrate and well contacts also reduce the base-emitter resistors.

2.4.5.1 Latch-Up Triggering Mechanisms

The triggering mechanism can be understood by considering the equivalent scheme with cross-coupled NPN and PNP bipolar transistors.

When active the PNPN structure has two stable states: Off-state where both bipolar transistors are Off- and On-state where both bipolar transistors are On.

The minimum voltage and current needed to sustain the On-state are called respectively holding current and holding voltage.

The holding voltage must be compared to the power supply voltage: When the PNPN structure is On, both base-emitter junctions are On and the collector-base junctions are also On (saturated structure). So the minimum holding voltage between Vdd and Vss is about 0.6 V. In practice, voltage drops in series resistors increases this minimum value that may reach 0.8–1 V. In most advanced technology nodes, this holding voltage is close or greater than the power supply value. So the reduction of power supply voltage limits the occurrence of SEL (Fig. 2.13).

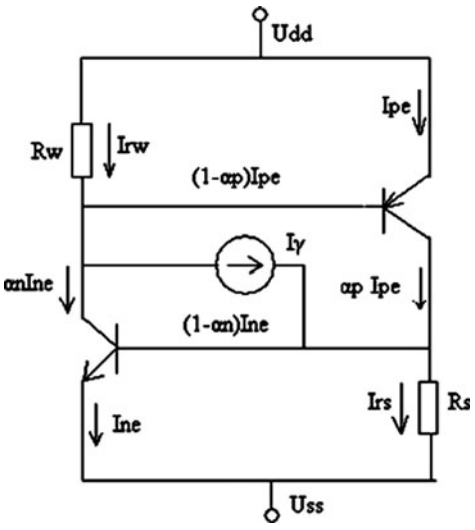

Fig. 2.13 PNPN structure trigger: The ion track crosses the N-Well/P-Substrate junction: The current is amplified in the positive feedback structure. After Useinov [41]

2.4.5.2 Design Rules Effects on SEL Sensitivity

The reduction of the base width increases the current gain and the cutoff frequency of the bipolar transistors. The junction capacitance decreases so the charge needed to bias the junction at +0.6 V is reduced. These parameters enhance the sensitivity because the trigger energy is reduced and the structure can switch with very short duration transients. But, as indicated above, at each new technology generation, the power supply decreases, the space-charge layer width and the free carrier lifetime decreases, and so the collected charge is reduced.

So a global compensation exists and SEL occurrence is difficult to predict without a detailed knowledge of the topology of the design.

SEL must be imperatively avoided by the designers. Several ways exists for eliminating it. The more drastic one is to use SOI technology that eliminates the PNPN structure. In bulk CMOS, as previously discussed, a thin epitaxial layer on a heavily doped substrate is efficient to reduce the shunt resistors in parallel with base-emitter junctions, and then a strong increase of a triggering current is needed.

SEL has been widely studied in the literature mainly for heavy ions [41, 42], but also for neutrons [43, 44]. For atmospheric neutrons-induced SEL, Dodd [43] has clearly shown that the sensitivity increases with temperature and power supply voltage. FIT values from 10 FIT to more than 300 FIT/Mb have been measured in SRAMs.

2.5 Conclusion

At ground level and in the atmosphere, SEEs are mainly due to neutrons and to alpha particles emitted by radioactive impurities. The recoils, created by neutron interaction with the nucleus of the different materials used to build the components, ionize the semiconductor and charges are collected at sensitive nodes. Soft errors (recoverable) and hard errors (non recoverable) can be induced in semiconductor devices. The basic mechanisms are rather well known, but a lot of work is still needed to accurately predict the sensitivity of the devices. For successive technology nodes, the relative importance of different effects varies. SEE prediction is a multidisciplinary task that involves nuclear and solid state physics, simulation tools, semiconductor technology, devices, and system architecture.

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