

Chapter 2

SiC Materials and Processing Technology

This chapter contains a broad review of SiC materials and processing technology necessary to create SiC electronics, micromechanical transducers, and packaging. Details on deposition and etching methods are covered. The material properties of various forms of SiC (single crystalline, polycrystalline, and amorphous) along with their use for creating the various components of harsh environment microsystems will also be discussed. Current status and future research are highlighted with regards to both materials and processing technologies.

2.1 Material considerations for various applications

The creation of harsh environment microsystems using SiC is advantageous because all of the system components can be made from SiC. Semiconductor grade SiC is commercially available for electronic device fabrication. MEMS structures can be fabricated using single-crystalline, poly-crystalline, or amorphous SiC. Likewise, packaging of MEMS and electronics can be accomplished using any of these forms of SiC. The following sections will briefly describe the materials consideration specific to each of these components of the microsystem.

2.1.1 Electronics (*crystallinity, doping, defects, polytype*)

As described in Chapter 1, over 200 SiC polytypes exist. Among all the polytypes, 3C-, 4H-, and 6H-SiC are the most commonly available today. Each SiC polytype exhibits different electrical, optical, and thermal properties due to differences in stacking sequence. Some of the key electrical parameters for 3C-, 4H-, and 6H-SiC are listed in Table 2.1 (a more detailed list of properties of SiC polytypes can be found in Table 1.2 in Chapter 1). The significant electrical disparity among

Table 2.1 Key electrical parameters of SiC [1]

Property	4H-SiC	6H-SiC	3C-SiC
Bandgap [eV]	3.2	3.0	2.3
Intrinsic Carrier Concentration (cm^{-3})	10^{-7}	10^{-5}	10
Electron Mobility at $N_D = 10^{16} \text{ (cm}^2/\text{V-s)}$	\parallel c-axis: 800 \perp c-axis: 800	\parallel c-axis: 60 \perp c-axis: 400	750
Hole Mobility at $N_D = 10^{16} \text{ (cm}^2/\text{V-s)}$	115	90	40
Donor (nitrogen) Dopant Ionization Energy (MeV)	45	85	40

these polytypes clearly shows that it is essential to use a single polytype (single-crystalline) for electronics device fabrication.

4H- and 6H-SiC are the only choice for wafer substrates since 3C-SiC wafers are not yet commercially available. Regardless of polytype, fabrication of devices directly on SiC wafers is hindered by lack of device quality wafers, inability to drive in surface doping (Chapter 1.1.2), and poor electrical quality as a result of direct ion implantation into the substrate [2]. Therefore, the SiC electronics fabrication is mainly centered on epitaxial layers grown on these substrates. Currently, high quality homoepitaxial layers of 4H- and 6H-SiC with different thicknesses and doping levels are routinely produced. 3C-SiC is also gaining attention as it can be grown heteroepitaxially on various substrate materials. Furthermore, there has been significant progress in producing device-grade 3C-SiC epilayers in recent years. However, it is necessary to further reduce crystallographic structural defects in 3C-SiC epilayers before this polytype becomes a viable alternative to 4H- and 6H-SiC [3].

Low defects, controlled doping, and dopant uniformity of both substrate and epilayers are crucial for device applications. In terms of the device type, low-resistivity substrates are vital for power devices as they reduce power losses due to parasitic substrate and contact resistances [1]. However, for devices and circuits operating at microwave frequencies; it is necessary to have semi-insulating substrates to achieve low dielectric losses and reduced device parasitics.

Most current SiC based electronics devices are fabricated using either 4H- or 6H-SiC due to the aforementioned short coming of 3C-SiC. Between 4H- and 6H-SiC, 4H-SiC has substantially higher carrier mobility, shallower dopant ionization energies, and low intrinsic carrier concentration (Table 2.1). Thus, it is the most favorable polytype for high-power, high-frequency, and high temperature device applications. In addition, 4H-SiC has an intrinsic advantage over 6H-SiC for vertical power device configurations because it does not exhibit electron mobility anisotropy while 6H-SiC does [1]. Therefore, many SiC device fabrication efforts have shifted towards 4H-SiC as it has become more readily available.

2.1.2 MEMS (*Stress, strain gradient*)

Silicon carbide MEMS are fabricated using both single-crystalline substrates and thin films. When MEMS structures are created using single-crystalline substrates, bulk micromachining (discussed in Chapter 4) is used. Fabrication of devices directly from the substrate material has the inherent advantage of having the same mechanical and electrical properties of original substrate and material optimization for MEMS can be avoided, particularly removing the need for stress and strain gradient optimization. However, from the structural device standpoint, bulk micromachining is limited in terms of device architectures that can be realistically fabricated. Thus, most SiC devices are fabricated using surface micromachining techniques.

In surface micromachining, the structural SiC layer is typically deposited on a different material layer, such as a sacrificial or isolation layer, and this interlayer involvement leads to deviations of both electrical and mechanical properties compared to the substrate. At the current maturity of the technology, it is not possible to achieve single-crystalline SiC with optimized electrical and mechanical properties for MEMS on widely-used sacrificial or isolation layers *i.e.* polysilicon, silicon dioxide, and silicon nitride. However, many MEMS devices do not require as stringent electrical characteristics as are needed for electronics. This allows the use of electronically inferior but mechanically sound alternatives. For instance, polycrystalline SiC (poly-SiC) can be produced with comparable elastic stiffness to single-crystalline SiC and can have sufficient electrical characteristics for MEMS applications. To date, most SiC MEMS devices are fabricated with poly-SiC. Amorphous SiC, though mostly electrically insulative, has also been used for MEMS components such as diaphragms as well as for packaging structures.

The key concerns with amorphous SiC and poly-SiC thin films are the residual stress and stress gradient of the deposited films. The residual stress in thin films can be attributed to many different sources. The films are deposited at temperatures significantly above ambient, and the difference in thermal expansion coefficients between the film and the underlying layers leads to stress generation upon cooling to room temperature. Crystal defects, impurity incorporation, and grain growth and orientation are also sources of film stress. When the mechanical microstructure is released the residual stresses in the structural layers relieve by deforming the structural layers. In extreme cases, the thin film may crack while attached to the substrate or delaminate from the underlying layers. Furthermore, a stress gradient exists when the residual strain in a film varies through its thickness. This is particularly troublesome for MEMS applications because it can cause significant curvature of free-standing microstructures even when the average residual stress of the film is near zero.

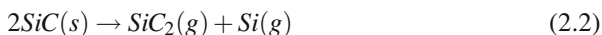
MEMS typically demands significantly thicker films than is needed for electronics fabrication. This further complicates the desire to produce low stress and low stress gradient films. Changes in stress levels through the film thickness occur because of changes in grain size over the course of the deposition. Therefore, micromechanical sensor fabrication requires processes that can precisely control mechanical

characteristics of deposited thin films. This will be described in more detail in Chapter 4.

2.2 Substrate

Production of semiconductor grade SiC ingots is one of the most challenging tasks faced by the SiC semiconductor and microsystems industry. Even though the first reported growth of SiC crystals by the Acheson technique dates back to 1892 [4], growth of single-crystalline SiC substrates with both size and quality equivalent to most common semiconductors — silicon, gallium arsenide, and indium phosphide — is yet to be realized. Difficulty growing single-crystalline SiC is attributed to the physical-chemical nature of SiC. The SiC phase diagram reveals a peritectic decomposition at 2830 °C and pressure around 10^5 Pa. Theoretical calculations indicate that stoichiometric melting can be attained when temperatures and pressures exceeding 3200 °C and 10^5 atm, respectively [56]. Therefore, growing single-crystalline SiC boules from stoichiometric melt or from solution (similar to common semiconductor growth) is impractical. Furthermore, using these very high temperature conditions makes producing single-crystalline materials rather demanding because of the narrow differences in enthalpy of formation of the different polytypes of SiC [6]. These reasons led SiC semiconductor developers to seek alternative methods that include solution phase growth from non-stoichiometric solutions and vapor phase growth. Solution phase routes exploit the solubility of SiC and carbon in silicon melt to grow SiC from non-stoichiometric solutions while vapor phase growth utilizes the sublimation products of SiC or CVD methods to produce SiC substrates.

The most common SiC substrate process is based on the vapor phase growth using sublimation products of SiC. SiC sublimes at temperatures above 1800 °C, forming various elemental and molecular species. The sublimation not only produce SiC(gas) but also forms various elemental and molecular species due to dissociation of SiC as shown in the chemical equations below [7]:



The first successful growth of high purity SiC crystal using sublimation growth was developed by Lely in 1955 [8]. Lely's initial process used a dense graphite crucible and a porous graphite thin-walled inner cylinder. The SiC powder is loaded between the inner and outer cylinder and heated to temperatures of 2550-2600 °C in an argon atmosphere. Spontaneous nucleation of SiC was observed at the inner surface of the thin-walled cylinder. The Lely method had limited impact on SiC crystal growth due to two main reasons. First, the control of platelet thickness, doping, and polytype of the crystal is poor due to the inability of controlling initial nucleation,

growth rate, and growth direction. Second, Lely method is capable of producing SiC crystals only up to 10 mm in diameter due to self-termination of the growth process as pores of the inner cylinder are blocked by growing crystals.

A major breakthrough came around 1980 with the introduction of SiC seed crystal sublimation growth. This method uses a high quality seed crystal surface to begin growth process in contrast to Lely's method which begin growth on a graphite membrane [9]. The seeded sublimation growth is often referred to as the physical vapor transport method (PVT) or Modified Lely Method. Later, this method was further refined for producing large diameter SiC boules [10, 11, 12]. Various improvements and modifications of PVT evolved from both commercial production environments and research laboratories until today it has become the current standard industrial process. High quality SiC wafers are routinely produced with the current PVT method (often referred to as the standard PVT method). Currently 100 mm 4H- and 6H-SiC wafers are commercially produced by standard PVT and 150 mm wafers are expected near future [14, 15].

The ever increasing demand for further improvement of quality and production throughput of SiC wafers requires either additional improvement of standard PVT or exploring other viable options. This has led to many successful attempts to fuse CVD based methods or further modify PVT techniques for producing semiconductor grade SiC wafers. One such method gaining attention for industrial wafer production applications is high temperature CVD (HT-CVD) [16].

Other recent efforts include continuous feed PVT (CF-PVT) [17], Halide CVD (H-CVD) [18], and Modified PVT (M-PVT) [19]. While these techniques claim to have some technological edge over their predecessors, they are still primarily at the research stage. Solution phase growth has yet to prove it is capable of producing large area substrates. Nonetheless, promising initial results and the advantages of this method will certainly draw more attention from the research and industrial community. Figure 2.1 summarizes the current status of known SiC substrate technology. The following section will briefly describe the processes involved in each of these techniques, and discuss their relative advantages over the well-established standard PVT method.

2.2.1 Vapor Phase Growth

2.2.1.1 Standard Physical Vapor Transport (PVT) or Seeded Sublimation Method

Standard PVT growth is carried out in a quasi-closed graphite crucible in an argon environment. The reactor configuration is schematically shown in Figure 2.2. The source material is held at the bottom of the crucible, and the seed is fixed onto the top lid of the crucible. The distance between source and seed is typically around 20 mm [20]. The crucible is inductively heated and operating temperatures of the system ranges from 1800 to 2600 °C. A linear temperature gradient is maintained

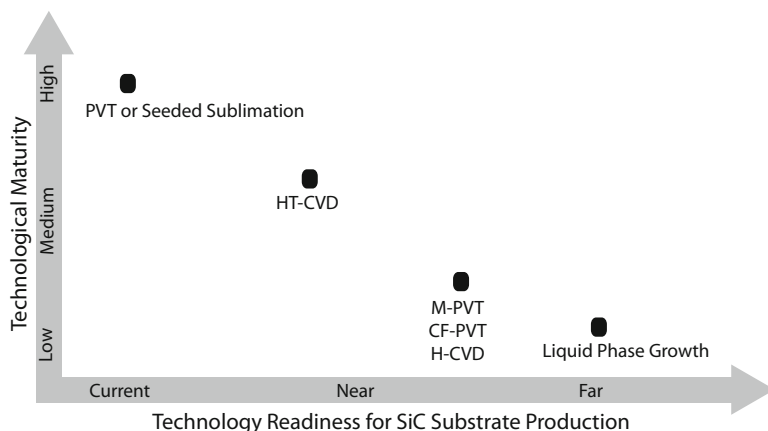


Fig. 2.1 The current state of possible SiC substrate technology available today.

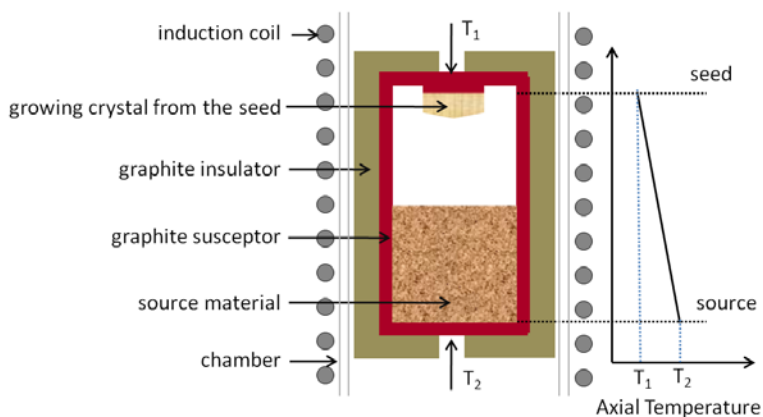


Fig. 2.2 The schematic representation of the standard PVT reactor with representative axial temperature profile.

between source and the seed causing vapor phase transport of Si and C containing species from the source to the seed. The typical temperature gradient ranges from 1.0 to 2.5 °C per mm. In most cases, the temperature at the bottom of the crystal is around 2300 °C while the seed temperature is around 2100 °C. The crystallization process is facilitated by the supersaturation of a vapor phase species at the seed surface [14, 15].

SiC boule growth via the sublimation process is complex and many growth parameters have to be controlled precisely for high quality crystal formation [14]. The suggested profile of two key parameters, temperature and pressure, during the growth process is shown in Figure 2.3. Initially, the source material is preheated up to 1800 °C. High argon pressure, typically around 600 Torr, is held during pre-

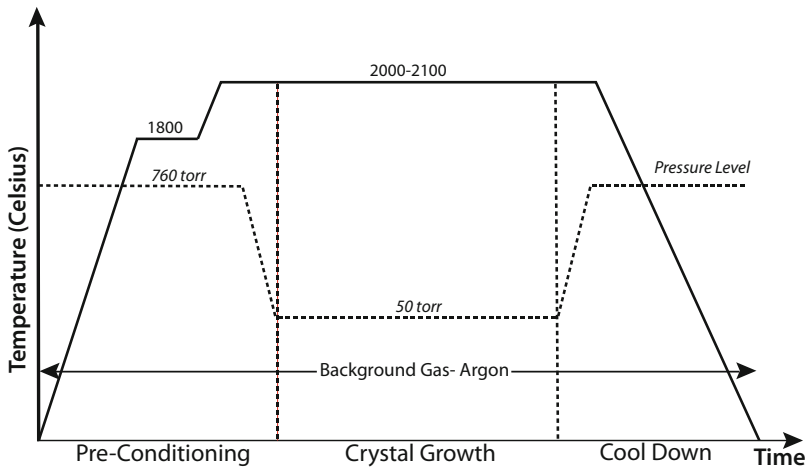


Fig. 2.3 [20] Temperature and pressure profile of the PVT growth process (©Taylor & Francis 1997), reprinted with permission.

heating and until the growth temperature stabilizes over 2200 °C to eliminate low temperature polytype growth, particularly 3C-SiC. Once at growth temperature, the argon pressure is reduced below 50 Torr to initiate the growth process [20]. Background argon pressure is again increased above 600 Torr to stop the growth process before decreasing the temperature. The typical growth rate of seeded sublimation lies between 0.2 to 2 mm per hour [14].

The nucleation, growth, and defect formation are intertwined with the temperature profile of the reactor and boule. Slight variations in the temperature profile can lead to defect formation via polytype formation and elastic deformation. Therefore, temperature control is a key aspect of this process. Defects in the seed crystal surface directly translate into defects in the bulk crystal. Hence, a high quality seed crystal is also critical for creating a high quality SiC substrate.

Other factors that are highly critical for SiC boule growth is the control of polytype and doping concentrations. Recently, several methods have been developed for controlling polytype and doping levels of SiC boules. Some of these technologies will be detailed in the later section of this chapter. They include the use of the surface polarity of the seed crystal and introduction of rare-earth elements to the source material [21, 22].

To date, the standard PVT method has become the dominant SiC growth technique used in the SiC industry. There is vast knowledge base in both academia and industry around standard PVT. This technique is capable of producing commercially-viable, large dimension SiC boules, up to 100 mm, with high crystal quality.

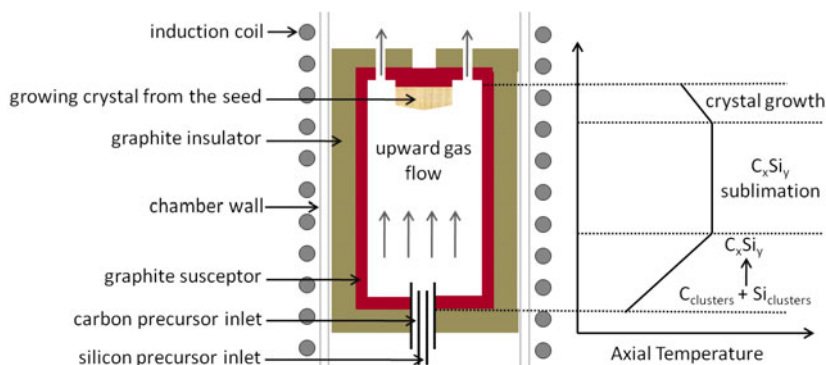


Fig. 2.4 [24] The schematic representation of the reactor geometry of HTCVD system with the temperature profile of the reactor along with corresponding chemical stages (©Trans Tech Publishing 2004), reprinted with permission.

2.2.1.2 High Temperature CVD Method (HTCVD)

The High Temperature CVD Method (HTCVD) for SiC bulk crystal growth is relatively young in comparison to PVT growth [23]. Nonetheless, tremendous progress has been reported in this method since its inception in 1996 [24]. HTCVD has very recently been used to produce commercial SiC wafers [15]. Figure 2.4 shows the schematic representation of the vertical reactor used in this process. The gas delivery components and retractable rotating crystal mount are the major differences between HTCVD and standard PVT reactors. Furthermore, the temperature profile of the reactor as shown in Figure 2.4 is also different from standard PVT.

The growth is carried out using conventional silicon and carbon containing precursors. Silane (SiH_4) is used as the silicon source while methane, ethane, or propane can be used as the carbon source. The growth precursors are introduced in coaxial tubes with the inner-most tube used for the silicon precursor. High flow rate and pressure conditions are maintained so that the dissociation of silane can lead to the formation of Si clusters by homogeneous gas phase nucleation. These clusters react with the hydrocarbon precursor as the temperature further increases downstream, forming Si_xC_y clusters. Upon entering to the high temperature heating zone, these Si_xC_y clusters sublime to form Si and C containing species before reaching the seed crystal. Crystal growth occurs via supersaturation, similar to the PVT technique. The typical growth rate associate with this process is 0.1 to 0.7 mm/h.

The technique offers some intrinsic advantages over the standard PVT method. The continuous feed of the precursor allows direct control of the Si to C ratio as well as the dopant concentration. The availability of high purity gas ensures the purity of the crystals. Semi-insulating crystal growth using HTCVD has been demonstrated [25]. The versatility of this method has been shown by growing p-type substrates with precise dopant control [26]. Despite initial successes, further refinement is

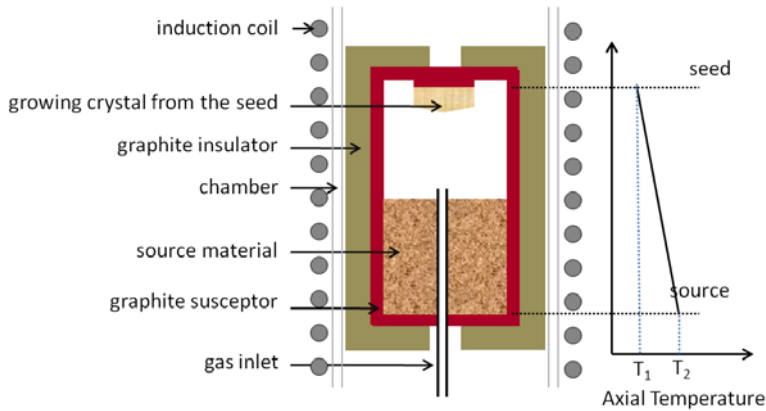


Fig. 2.5 [14] Typical reactor configuration of M-PVT method and the temperature profile of the reactor (©IOP 1997), reprinted with permission.

needed in order to obtain large diameter crystals, which would enable it to be a commercially-viable competitor to standard PVT.

2.2.1.3 Modified PVT Method

The modified PVT (M-PVT) method is derived from both the standard PVT and CVD methods. Figure 2.5 schematically illustrates the reactor architecture used in M-PVT along with the axial temperature profile of the reactor. The configuration is very similar to that of a conventional PVT reactor with the added capability of delivering small amounts of Si and C containing gaseous precursors, as well as dopant precursors to the system [19]. This configuration enables a growth process carried out in a very similar fashion to PVT but with more precise control of stoichiometry and dopant uniformity of the SiC crystals.

In a conventional PVT reactor, the gas phase composition of various Si and C containing gas species is determined by the temperature field that is set by the heating procedure and crucible design. However, the temperature field can change during the growth process due to process instabilities induced by evolution of the crystal as well as changes in gas phase composition arising from morphological changes in the source materials. In M-PVT, the ability to feed Si and C containing gases at the growth front allows minimizing the variations in gas phase composition, enabling better controlling growth of SiC crystals.

The possibility of continuous feeding of dopant gases also improves the resulting doping level uniformity in both axial and radial directions. In PVT, nitrogen is usually used for n-type doping. Nitrogen gas is incorporated into the wall of the growth crucible, exploiting the porosity of the graphite. In the case of p-type doping, aluminum is directly mixed into the SiC source material. The much higher vapor pressure of aluminum in comparison to Si and C containing gas species makes mass

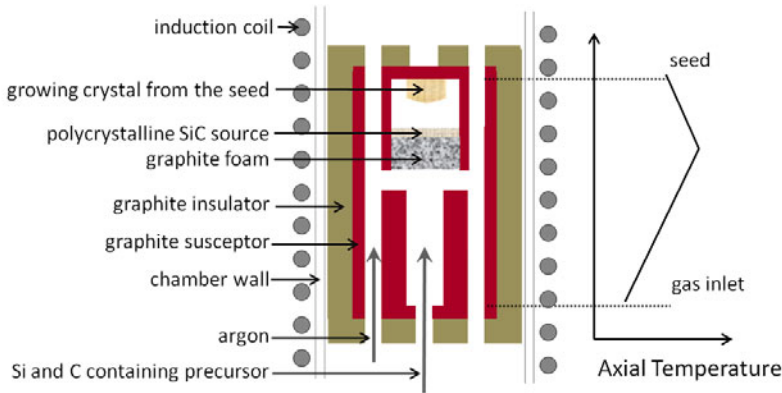


Fig. 2.6 [14] Schematic drawing of the reactor configuration of CF-CVD and the axial temperature profile (©IOP 1997), reprinted with permission.

transport control rather difficult. M-PVT enables continuous feed of aluminum vapor or aluminum containing precursor with fine control. This method may lead to the fabrication of low resistance p-type SiC wafers that will open paths to fabricate power SiC device on p-type wafers. Ion implantation experiments demonstrated that phosphorus exhibit a ten-fold increase in solubility limit compared to nitrogen [27]. Thus, it can be argued that higher n-type doping can be achieved using M-PVT by continuous feed of phosphine gas, a widely used n-type doping precursor in the semiconductor industry.

2.2.1.4 Continuous Feed PVT (CF-PVT)

The continuous feed PVT is essentially a hybrid of both PVT and HT-CVD. This method exploits the fundamental advantages of both PVT and HT-CVD techniques for producing high quality SiC crystals [17, 15]. Figure 2.6 shows the typical configuration of the CF-PVT reactor. A Si and C containing single precursor tetramethylsilane diluted in argon is typically used as the source material. At the low temperature zone, tetramethylsilane forms high quality poly-crystalline SiC through a process similar to HT-CVD. This poly-crystalline SiC source material is transferred to the high temperature sublimation zone through a highly porous graphite foam layer. The SiC growth occurs through supersaturation similar to that of classical PVT. The growth rate obtained by this method is around $100 \mu\text{m/h}$ at 1900°C .

One of the inherent advantages to the CF-PVT is its ability to grow longer SiC ingots because of the continuous supply of the source material. In classical PVT, the supersaturation close to the seed surface is controlled by the pressure and temperature distributions within the crucible. This method adds another parameter to process control: precursor concentration. It has been shown that the feeding gas flow rate that controls the source material formation can be used for precise control

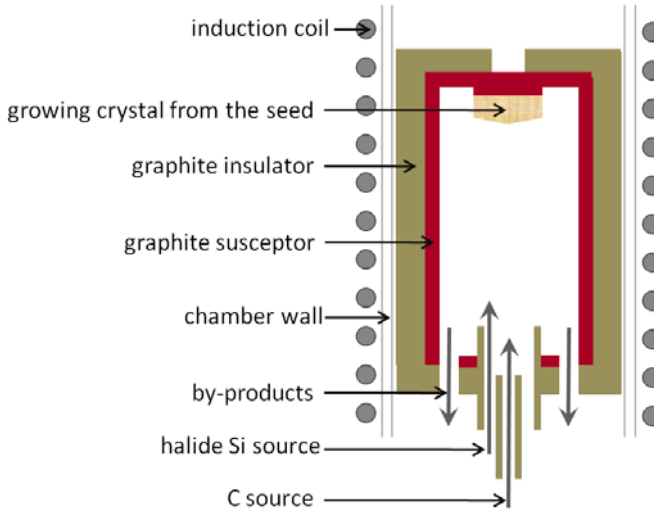


Fig. 2.7 [14] Schematic representation of the HCVD growth reactor (©IOP 1997), reprinted with permission.

of the supersaturation close to the seed that, in turn, enables a means of polytype control [28]. Although CF-PVT is at an early stage of development, it has successfully produced both high purity 4H-SiC and 3C-SiC [28].

2.2.1.5 Halide CVD (HCVD)

Halide Chemical Vapor Deposition (HCVD) is a recently introduced and very promising technique for the creation of high purity SiC crystals [18, 30]. The process is done in an inductively heated chamber very similar to a HT-CVD reactor; however, the growth mechanisms are fairly different. HCVD growth occurs through surface reaction, and the growth rate is determined by desorption kinetics. The process characteristics are the same as the conventional CVD. The earlier described HT-CVD growth takes place by a sublimation process, and growth rate is determined by supersaturation. Figure 2.7 schematically represents the reactor. A chlorinated Si precursor (SiCl_4), a C precursor (C_3H_8 or CH_4), and hydrogen feed upward from the bottom of the reactor via separate concentric graphite injectors. Chlorinated precursors are used to avoid homogeneous nucleation in the gas phase. Reactor temperature is maintained around 2000°C , and no temperature gradient exists between seed and source in contrast to all other previously described method. The typical growth rate of this method is $250\text{--}300\ \mu\text{m/h}$.

HCVD possesses all the intrinsic advantages that classical CVD offers. The stoichiometry of SiC crystals can be easily controlled by using the flow rates of the precursors and keep constant throughout the growth process. The crystal grown with HCVD has very low impurity levels and high electrical resistivity mainly due to the

use of high purity precursor gases. These features of HCVD are very attractive for producing semi-insulating SiC wafers for high power devices.

2.2.2 Solution Phase Growth

The thermodynamic properties of SiC do not permit the solution phase bulk growth of SiC from a stoichiometric melt (section 2.2). However, many studies have taken advantage of the solubility of both SiC and C in Si melt as an alternative route to grow SiC from a high temperature solution. The key to this method is that SiC can be grown from the liquid phase using non-stoichiometric solutions containing Si and C [31]. Early efforts on solution phase SiC crystal growth date back to 1961 [32]; however, there has not been much progress reported on this method until very recently. The main reason is the remarkable success of PVT methods, which have diverted attention away from the solution growth approach. The recent focus on liquid phase bulk growth of SiC is mainly driven by its ability to grow crystals with low dislocation densities and grow crystals at relatively low temperatures (1500–1700 °C at the seed). Solution growth process occurs under the conditions close to thermal equilibrium resulting in high quality crystals with better polytype controllability [33, 34]. The low growth temperature is also attractive for 3C-SiC growth as this polytype forms at relatively low temperatures, and sublimation growth, which requires relatively high growth temperatures, is not suitable for 3C-SiC growth.

The low solubility of C in Si melt, which is directly related to the growth rate, is one of the limiting factors to this method. This problem can be mitigated by adding transition metals into the Si melt, which increases the solubility of carbon for higher growth rate. Besides the solubility aspect, there are other important issues that must be considered when selecting the solvent (Si + metal) system. Those include no metal incorporation into the solid, excellent wetting of the crystal by the solvent, low vapor pressure, low melting point, and reduced degradation of the crucible due to reaction mixture. Furthermore, the crystal should be the only stable solid phase [31]. A few solvent systems have been successfully employed, and reasonable progress has been made in terms of increasing growth rate and the crystal diameter.

Several growth techniques have been considered for solution growth of SiC. The commonly discussed techniques include traveling zone method, slow cooling technique, and top seed solution growth method (TSSG) [31, 35, 36]. To date, TSSG is the most successful method of growing SiC crystals from solutions. Figure 2.8 shows a typical reactor configuration for TSSG growth. The seed crystal is mounted on a graphite rod inserted into the growth crucible. The seed and crucible can rotate with respect to each other. In typical process mode, only the seed is rotated at 10–20 rpm. In the accelerated crucible rotation technique, which is used for increasing growth rate, both the crucible and the seed are rotated in opposite directions. The maximum crucible and seed rotation rates are typically 20 and 10 rpm, respectively. The seed is held as the low temperature point and a temperature gradient of 2.0 °C/mm is maintained between the seed and the bottom of the crucible.

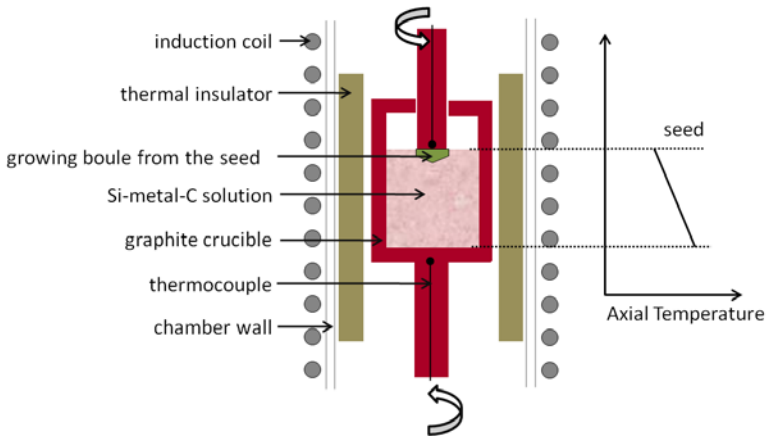


Fig. 2.8 [37] Schematic representation of the TSSG growth reactor (©Elsevier 2008), reprinted with permission.

Initial research done by Hoffmann *et al.* [31] using TSSG has demonstrated growth of 1.4 inch 6H-SiC crystals with a high degree of crystallinity. The reported growth rate ranges between 0.05-0.2 mm/h. Recent research reported from Japan shows the growth of 6H-SiC single crystals from Si-Ti-C ternary solution using TSSG. Two inch diameter SiC crystal with thickness of 5mm (Figure 2.9) was grown and the crystal exhibited a homogeneous green color without cracks and inclusions of polytypes [36]. The capability of the solution growth process for growth of 3C-SiC crystals, the forgotten polytype, has also been demonstrated recently by using a slightly modified version of the TSSG reactor [37]. This method has produced crystals with reduced stacking fault densities in comparison to 3C-SiC crystals produced by chemical vapor deposition methods.

These studies have clearly positioned the liquid phase growth as a viable route for bulk SiC crystal growth. Nonetheless, there exist many unanswered questions before it becomes a competitor to the standard PVT method. Some of the fundamental questions include the control of dopant concentration and uniformity as well as the incorporation of solvent into the crystal. Finding a suitable crucible material, though graphite shows promise, is a challenge as molten Si is highly corrosive to all current crucible materials. Increased complexity of the growth equipment is also a considerable factor.

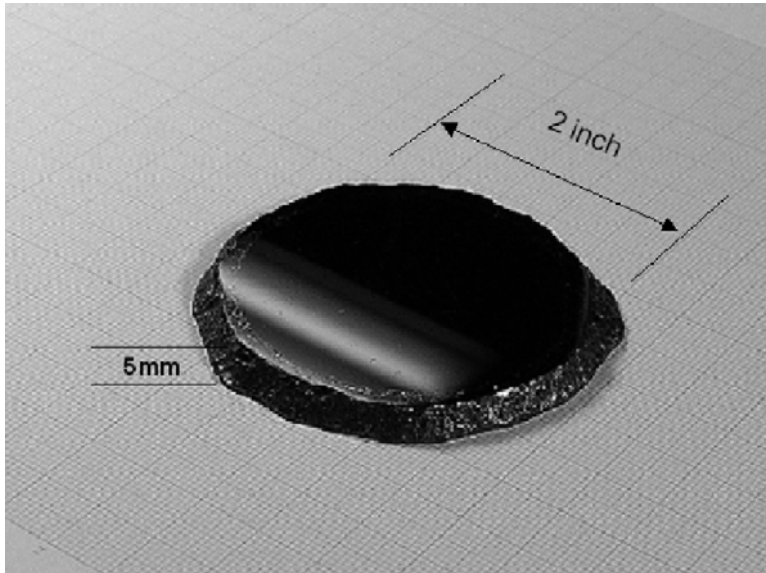


Fig. 2.9 [37] 6H-SiC bulk crystal grown by TSSG technique using Si-Ti-C solution (©Elsevier 2008), reprinted with permission.

2.2.3 Growth Related Issues

2.2.3.1 Polytype Control

A characteristic property of SiC is its ability to exist as over 200 polytypes. The most common polytypes are 3C, 4H, 6H and 15R. As described in Chapter 1, SiC is formed by covalently bonded silicon and carbon atoms in a tetrahedral fashion with each C atom surrounded by four Si atoms and each Si atom is surrounded by four neighboring carbon atoms. These Si-C units are arranged in a hexagonal bilayer with Si and C alternately occupying sub-layers. The stacking sequence of these bilayers along the C-axis determines the polytype. Depending on the terminating atom type, the 0001 face of the SiC has either a C or Si terminating layer.

One of the major obstacles faced by the SiC substrate technology is the different polytype inclusion in crystals. Polytype inclusion during the growth limits the larger diameter single-crystalline SiC substrates. Polytype inclusion also creates nucleation sites for other defects leading to severe quality deterioration [38, 39, 40, 41, 42]. The main reason behind the different polytype inclusion during growth is very low stacking fault energy. This demands exceptional control over thermodynamic and kinetics of the growth process, thus, precise control of thermal conditions and growth pressures are needed [43, 44]. The growth cell must be carefully designed and special attention must be given to the mounting of the seed crystal [14]. In addition to thermal and pressure conditions, the other factors that

influence the polytype inclusion include seed surface polarity [21, 11], supersaturation [44, 6, 28, 45], vapor phase stoichiometry [45, 44, 6], impurity levels [46, 47], seed off-cut angle [48, 49], and facet of the crystal [42].

Surface polarity of the seed crystal has a dominant influence of the polytype of the growth crystal in PVT growth. As stated previously, SiC lattice consists of a bilayer in which Si and C making alternating layers. This makes silicon carbide polar in nature, thus, it has two chemically different [0001] crystal surfaces, i.e. the [0001] Si-face and the [0001] C-face, which have different surface energies. It has been shown that the [0001] Si-face has a higher surface energy than the [0001] C-face [11]. The 4H polytype, which has a higher formation enthalpy, always grows on the C-face with the lower surface energy regardless of the polytype of the seed crystal used. Similarly, the 6H polytype, which has a lower formation enthalpy, preferentially grows on the Si-face with the higher surface energy. Many studies have revealed that the polytype of the grown crystal depends on surface polarity rather than the polytype of the seed, thereby indicating the strong influence of the surface energy or surface polarity on the resulting polytype inclusions [50, 11].

Analytical modeling shows a strong correlation between growth temperature and nucleation of different SiC polytypes [51]. For instance, 3C-SiC grows at low temperature while hexagonal polytypes need high growth temperature due to differences in the energy of formation. 4H-SiC requires growth temperatures lower than that for 6H-SiC growth [43, 44] but 4H and 15R polytypes occur at similar temperature conditions [52]. It is rather difficult to control polytype transition by merely controlling temperature conditions however, as the stacking fault energy is very small. There exists a complex interplay between formation energy and growth condition on polytype inclusion in both the initial stage as well as during the growth. Two parameters that have significant impact on polytype transition are supersaturation and the Si:C ratio in the vapor phase. These parameters are directly controlled by the crucible temperature, temperature gradient, and pressure of the reactor. High supersaturation and low Si:C vapor ratio are crucial to form 4H polytype when grown on the C-face of 6H-SiC. A high axial temperature gradient is needed to meet both these conditions as it allows the use of a high source temperature, thereby producing carbon rich vapor, and low seed temperature, which facilitates supersaturation [6, 45]. When the 4H polytype is grown on the C-face of a 4H-SiC seed, high reproducibility is achieved if growth starts at low supersaturation levels (growth rates of 100 $\mu\text{m/h}$). However, once the proper growth front has developed, supersaturation level can be increased in order to obtain high growth rate [44]. This is typically achieved by reducing the inert gas pressure while keeping the high temperature gradient to achieve the desired Si:C ratio.

Impurities in source materials also found to affect SiC polytype stabilization. Rare-earth elements such as Sc and Ce tend to stabilize the 4H polytype [47, 22]. The exact role of these elements is still unknown; however, some speculative assumptions have been made. One assumption suggests that these metals may enrich the vapor with C via carbides [14] and others think impurities work as a surfactant which changes the surface energy of the nuclei [50]. Nitrogen, which incorporates into the lattice, also has a significant impact on the polytype stability of 4H-SiC.

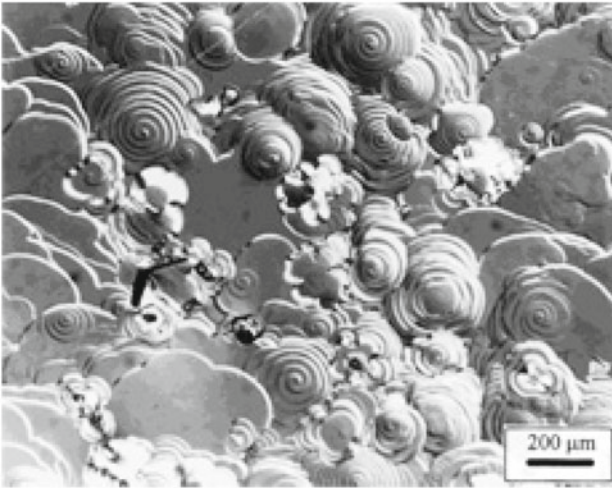


Fig. 2.10 [14] SEM image of growth surface with several growth centers assumed to be formed through spiral growth mechanism around screw dislocations (©Wiley 1997), reprinted with permission.

This effect is attributed to the influence on the Si:C concentration ratio and to the relative enrichment of the growing surface with carbon [47, 50, 46].

2.2.3.2 Substrate Defects Control

Substrate defects are detrimental to the SiC device technology because these defects typically propagate to the subsequent epilayers. The reduction of the substrate defects is perhaps the most critical challenge faced by SiC wafer technology. As most studies centered on reducing defects in wafers grown using standard PVT method, most of the discussion here related to the standard PVT growth of 4H- and 6H-SiC with growth direction parallel to the c-axis, unless otherwise stated.

A distinct feature to PVT growth is the existence of growth spirals (Figure 2.10). Many growth factors such as instabilities in growth parameters and the quality of the seed crystal can lead to secondary and three-dimensional nucleation causing the spiral growth [14]. These spirals have a strong relation to the formation of crystal defects. For instance, these spirals can move across one another as the growth progress resulting in low-angle grain boundaries due to mis-orientation of one spiral with respect to the other. Other major defects due to spiral growth include dislocations, crystal mosaicity (domain structure), and micropipes (open core screw-dislocations).

Among all defects, micropipes are seen as the major threat that can potentially limit the viability of SiC as a commercial semiconducting material. Micropipes, the hollow core of a large screw dislocation, penetrate the entire crystal along the growth direction (when growth is parallel to *c*-axis) and are replicated to the device epitaxial layer [53]. Therefore, they become detrimental to the device performance. The causes and the formation of micropipes have been widely discussed and there exist many contradicting views and opinions on the mechanisms involved in micropipe formation. Most opinions revolve around Frank's Theory [54] that predicts micropipes are formed on a screw dislocation that possesses a large Burgers vector. Recent studies using synchrotron white-beam x-ray topography (SWBXT) further confirm that micropipes are large Burgers vector screw dislocations and the magnitude of the Burgers vector of a micropipe can range from 2 to 7 times the unit *c* lattice parameter [55]. Size of the micropipe has a direct relationship to the magnitude of the Burgers vector.

Several possible growth-related sources of micropipe formation have been identified [56, 57]. They can be categorized into three groups: thermodynamics, kinetics, and technological related. The thermodynamic sources can be thermal field uniformity, vapor phase composition, vacancy supersaturation, dislocation formation, and solid-state transformation. The kinetic sources include nucleation processes, growth phase morphology, inhomogeneous supersaturation, and capture of gas bubbles [14]. The technological aspects include process instabilities, seed surface preparation, and contamination of the growth system. Better understanding of these sources along with experimental investigations and accurate modeling of the growth process have resulted in a vast improvement of growth technology and successful control over micropipe formation. Particularly in recent years, there has been a steady progress in reducing of micropipe densities. Currently, four inch n-type 4H-SiC wafer with zero micropipes are commercially available [13].

Micropipe defects are seen in crystals grown by the seeded sublimation growth (standard PVT) with the growth direction parallel to *c*-axis. Even though the micropipe defects are inherent to seeded sublimation growth, crystals grown using its ancestry methods, namely Acheson and Lely, rarely exhibits any micropipes. The phenomenon is credited to the growth direction as Acheson and Lely crystal growth occurs in the directions perpendicular to the *c*-axis, that is [1100] and [1120] (*a*-axis). The micropipe suppression for these off-axis growth methods is attributed to strain relaxation. Strain relaxation largely depends on growth axis and differs significantly between the crystal grown parallel to the *c*-axis and perpendicular to the *c*-axis [58]. These finding led to new research directions and many research have been focused on growing SiC perpendicular to *c*-axis. Results confirm that micropipes can be the eliminated when crystals are grown in the [1100] and [1120] direction using seeded sublimation growth [59, 60]. Although this approach has shown merit in reducing micropipes, at its current stage, the commercial feasibility of this method is rather remote because this method tend to yield a large number of basal plane stacking faults in the grown SiC crystal [58, 61]. Recently, a method called inverted "repeated *a*-face" growth was introduced as a modification of the perpendicular to *c*-axis growth process [62]. This method is far superior in terms

of its ability to reduce the micropipe density along with the density of dislocations. However, the complexity of this method has prevented its wide spread commercial implementation.

2.2.3.3 Electrical Property Control

Resistivity is one of the most important factors for any semiconductor material. The challenge is to control the residual and intentional doping levels for desired device applications. High power devices, one of the major application areas of SiC, require low resistance substrates in order to reduce power losses caused by parasitics and contact resistances. In contrast, semi-insulating substrates are essential to achieve low dielectric losses and reduced device parasitics for devices and circuits operating at microwave frequencies.

Nitrogen is commonly used as the n-type doping impurity and aluminum is the main p-type dopant for SiC. They create relatively shallow donor and acceptor levels in the SiC bandgap. Recently, phosphorus has been proposed as a replacement for nitrogen as the n-type donor, because the solubility of phosphorus in SiC is higher than that of nitrogen [27]. However, the standard PVT method used for commercial production of SiC substrates uses nitrogen. Nitrogen doping is carried out by incorporating nitrogen gas into the wall of the growth crucible by exploiting the porosity of the graphite. Aluminum, on the other hand, is directly mixed into the SiC source material though aluminum depletion during the process is a key drawback to this approach. This source depletion during the growth has negatively impacted the production of p-type substrates by standard PVT.

The characteristics of dopant incorporation to 6H and 4H polytypes are generally similar. In the case of seed polarity, the doping incorporation varies substantially between the [0001] C-face and [0001] Si-face. Nitrogen incorporation in crystal grown on the [0001] C-face of 6H- or 4H-SiC exhibits higher carrier concentration than crystal grown on the [0001] Si-face under identical growth conditions by a factor of 3 to 5 times [21]. Figure 2.11 shows the dependency of dopant incorporation on nitrogen flow for the n-type doped 6H-SiC grown on the [0001] C-face and [0001] Si-face [21]. A reverse effect has been seen with regards to aluminum incorporation as it prefers the [0001] Si-face. In the case of undoped SiC crystals, the crystals grown on the [0001] C-face show n-type conductivity while the crystals grown on the [0001] Si-face exhibit p-type conductivity. The preferential doping incorporation is attributed to surface kinetic effect as N incorporate to C sites and Al incorporate to Si sites on the crystal.

The surface polarity effect along with precise control of growth parameters has been used for effective control of the impurity levels. Currently, highly doped (10^{20} cm^{-3}) n-type 4H- and 6H-SiC and semi-insulating (10^{14} cm^{-3}) 4H-SiC substrates are commercially available. The lowest reported resistivity values for 4H and 6H-SiC are 0.0028 and 0.0016 $\Omega\text{-cm}$, respectively [14], while the highest resistivity value reported is for 4H-SiC: greater than $10^5 \Omega\text{-cm}$ [13]. Owing to its intrinsic crystal properties, 4H-SiC has higher carrier mobility with smaller anisotropy com-

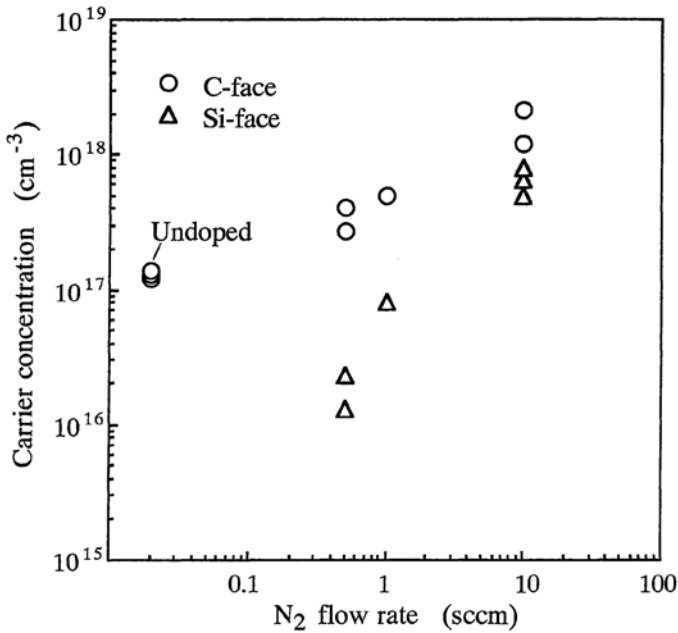


Fig. 2.11 [21] The dependence of the dopant incorporation on nitrogen flow for the n-type doped 6H-SiC grown on [0001] C-face and [0001] Si-face (©Japan Society of Applied Physics 1995), reprinted with permission.

pared to 6H-SiC. These key properties are highly beneficial for high power and high frequency device applications, and due to this particular benefit, the current market trend is leaning towards 4H-SiC substrates.

2.2.4 Current Status

Larger diameter SiC substrates with low defect densities, high crystalline quality, and controlled impurity levels are critical for realizing the full potential of SiC as a mainstay material for electronics, photonics, and microsystems. Continuous relentless research and development efforts from both academia and industry have guided SiC substrate technology to new heights in terms of quality and the size. Figure 2.12 shows the progress of increasing the substrate diameter during the last two decades [63]. Currently 100 mm diameter 4H- and 6H-SiC substrates are commercially available, and it is expected that 150 mm diameter substrates will soon become available.

In addition to increasing the wafer diameter, reduction in defect densities, especially micropipes, took precedence over the last ten years because both performance

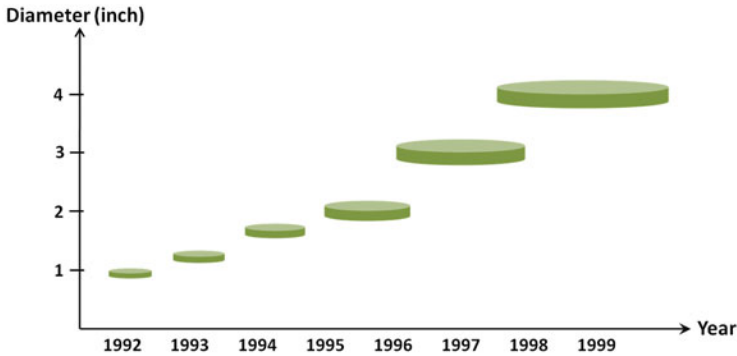


Fig. 2.12 [63] Increase in wafer diameter for 4H-SiC vs. year (©Elsevier 1999), reprinted with permission.

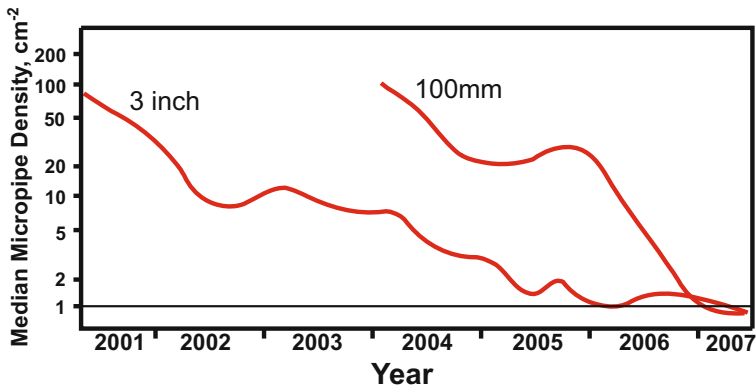


Fig. 2.13 [64] The reduction of median micropipe density on n-type 4H-SiC vs. time for 100 mm and 3 inch wafers (©Trans Tech Publications 2009), reprinted with permission.

and yield largely depend on these defects. Figure 2.13 shows the recent progress in micropipe reduction of PVT grown SiC substrates [64]. It should be noted that this data is related to SiC growth along the c-axis as this is the current method of commercial production of SiC substrates.

It is clear that SiC substrate technology has made a tremendous progress during the last two decades. These advances indisputably provide a solid foundation for the realization of the full SiC microsystems. Further reduction of substrate defects, increase of wafer diameter, and decrease of production cost will lead to the full potential of SiC as the materials for harsh environment microsystems.

2.3 Epitaxial Thin Films

The realization of SiC based harsh environment microsystems is in part determined by the ability to produce SiC electronic devices. For all SiC electronics, epitaxial film growth is a necessity as diffusion doping of substrate is not feasible, and direct ion implantation into the substrate, as is typical for Si, produces inferior electrical quality in SiC [2]. Therefore, the progress and performance of SiC electronics devices to a large extent depends upon the quality, reproducibility, and high volume production capability of epitaxial SiC layers. This includes reducing of defect densities, eliminating polytype inclusions, and controlled doping of n-type and p-type with doping profiles ranging from extremely low (10^{14} atom/cm³) to very high (10^{20} atom/cm³). Epitaxial growth of SiC on a variety of substrates has been reported that include homoepitaxial growth on SiC substrate and heteroepitaxial growth on silicon substrate [65, 107, 67]. The discussion here simply focuses on homoepitaxial growth on SiC substrates because it is a prerequisite that devices have to be on SiC substrates for harsh environment compatibility. Furthermore, nearly all SiC high performance devices are currently fabricated using homoepitaxial films as they provide superior electrical characteristics.

Homoepitaxial growth of SiC films can be achieved by various means, each with its own advantages and disadvantages. Selection of a growth technique is in part determined by the application requirements and the technological maturity of the technique. The reported homoepitaxial techniques for SiC can be categorized into vapor phase epitaxy (VPE), liquid phase epitaxy (LPE), and vapor-liquid-solid (VLS) epitaxy. The latter is a recently introduced, novel epitaxial approach which shares the common fundamentals of VLS nanowire and nanotube growth [68, 69]. The following section will briefly discuss SiC epitaxial growth techniques in terms of their maturity and impact as well as advantages and disadvantages.

2.3.1 Vapor Phase Epitaxy (VPE)

Three main techniques are applied in Vapor Phase Epitaxy (VPE), namely chemical vapor deposition (CVD), sublimation epitaxy, and high temperature CVD. Among these, CVD is the most matured and researched technique for epitaxial growth of SiC. It is the core technique adapted by the industry for commercial production of epitaxial SiC (epitaxial thin film on SiC substrate) wafers. Epitaxial SiC wafers are generally referred to as SiC epi wafers.

2.3.1.1 Chemical Vapor Deposition (CVD)

In CVD growth of SiC, carbon- and silicon-containing gaseous compounds are transported to a heated single-crystalline SiC substrate where the homoepitaxial growth occurs through a surface-induced chemical reaction. Depending on the poly-

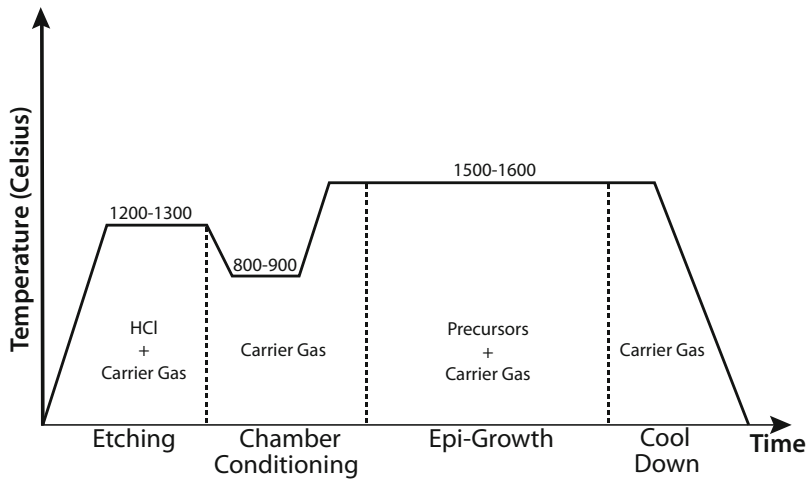


Fig. 2.14 [20] Typical temperature profile vs gas flow conditions for CVD homoepitaxial growth of SiC (©Taylor and Francis 1997), reprinted with permission.

type and the reactor configuration (hot wall or cold wall), the growth temperature can be considerably different, but typically, is above 1200° C. Based on the deposition pressure, CVD can be categorized into atmospheric pressure CVD (APCVD) and low pressure CVD (LPCVD). APCVD was a dominant technique for SiC epi growth throughout the 1980s and early 1990s, mainly due the availability of the APCVD reactors. With advancement in LPCVD, researchers shifted focus to LPCVD as it offers better control of the growth process in terms of gas phase nucleation and impurity levels. Most current industrial processes are now based on LPCVD, yet APCVD is still being used in some research laboratories throughout the world.

There are many different gases used as Si and C precursors. For Si sources, SiH_4 , SiH_2Cl_2 , SiCl_4 , and Si_2H_6 are the most popular choices. C_3H_8 is the most common C source. CH_4 , C_2H_2 , and CCl_4 have also been explored as C precursors. In almost every case, hydrogen is used as a carrier or growth-facilitating gas. Process conditions for a particular gas combination may need to be tuned due to differences in dissociation and nucleation kinetics of the precursors. A typical process for homoepitaxial growth of SiC using SiH_4 and C_3H_8 are shown Figure 2.14 [20].

The process starts with etching the substrate with HCl gas around 1200-1300°C. This helps to atomically clean the surface, which in turn reduces the defects in the epilayer. After etching is stopped, the temperature is reduced and the H_2 flow rate is increased. High hydrogen flow ensures the flushing of residual HCl from the reaction tube. Then reactor temperature is increased again to the appropriate epi growth temperature while keeping the hydrogen flow constant. Once the temperature uniformity is achieved, the precursor gases are introduced into the reaction tube. At the end of crystal growth, the precursor gases are shutoff, the reactor temperature is main-

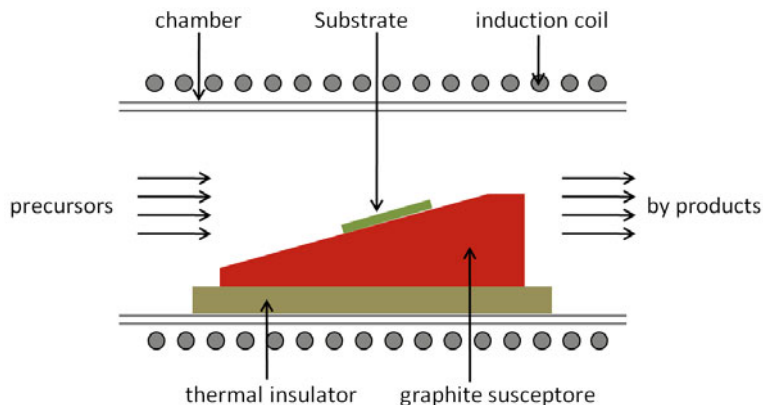


Fig. 2.15 The reactor geometry of the cold-wall SiC epitaxial CVD reactor used in early stage of SiC technology.

tained at the same level for few minutes while hydrogen is flushing out the residual precursor gases before the temperature is decreased. This prevents the inclusion of low temperature polytypes. CVD growth reactors for SiC epi can be categorized into two major groups, cold wall and hot wall. Prior to the mid 1990s, cold-wall reactors were primarily used for SiC epitaxy. Cold-wall reactors were common in III-IV semiconductor processing and adapting that technology for initial SiC development was relatively easy. However, the trend has changed toward hot-wall reactor because of the intrinsic advantages of hot-wall reactor based processes. Currently, hot-wall reactors are the dominant configuration in commercial SiC epi wafer production.

Many reactor configurations have been exploited in both cold-wall and hot-wall CVD. Each of these reactors has its own advantages and limitation in terms of control growth and throughput. Some are highly suited for industrial level production while some offer more flexibility for research and development. Most common reactor types will be discussed below. This will be followed with process related issues and advances in CVD epitaxial growth of SiC.

Early research into SiC epi growth was performed using converted gallium-arsenide reactors similar to one shown in Figure 2.15. The cold-wall configuration is achieved by using a double-walled quartz tube with water circulated between the walls. The wafer is placed on an inductively heated graphite susceptor. To ensure the cold-wall conditions, the susceptor is placed on thermal insulation. The susceptor is slightly tilted with respect to the gas flow to minimize the gas depletion effect for uniform growth. The capabilities of reactor configuration were limited in terms substrate size, temperature uniformity, and growth rate, yet it can be valuable tool for understanding aspects of epitaxial growth.

Later, many cold-wall reactors with slightly different configurations were introduced. Figure 2.16 shows two of the notable reactor configurations used in SiC epitaxy. Figure 2.16(a) a represent the multi-wafer barrel reactor developed by Kong and co-workers [70]. The multiple wafer capability and reduction in particle accu-

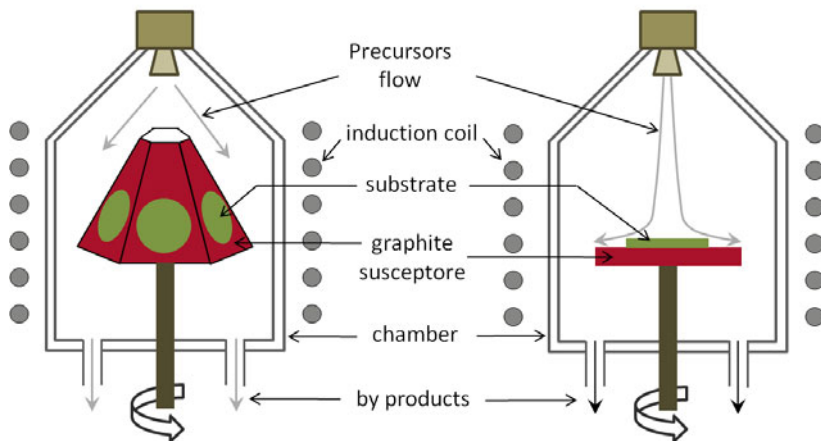


Fig. 2.16 Schematic drawings of cold-wall multi-wafer barrel reactor and rapid rotating reactor.

mulation on the substrate surface is a key advantage to this geometry. This is one of the early era reactor design which still being used in both epitaxial and polycrystalline SiC growth. The rapid rotating vertical reactor (Figure 2.16(b)) was developed in the late 1990s and has shown promises. This reactor would be very good choice for research scale applications; however, further scaling of this reactor to facilitate large area wafers for industrial scale production is challenging. The depletion of source gas and dopant precursor along with temperature nonuniformity causes variations in thickness and dopant profiles [71, 72].

Despite heavily used in early stage SiC development some inherent disadvantages of the cold-wall reactor configuration limits its viability as an industrial tool for SiC epi. Most of the shortcomings are related to the thermal uniformity of the reactor because the area above the substrate is not actively heated. The hot wall reactors enjoy better thermal uniformity in both lateral and vertical directions. In comparison, the temperature gradient in the vertical direction over the substrate surface can be as large as 220K/mm in a cold-wall reactor and that is nearly ten times higher than what is achievable in a hot wall reactor [73].

One of the key disadvantages that relates to the temperature profile of the cold-wall reactor is poor precursor dissociation efficiency, which directly translates into the growth rate. The maximum growth rate of cold-wall reactors is around 5 $\mu\text{m/h}$ [74] while the growth rate of a hot-wall reactor can be as high as 100 $\mu\text{m/h}$ [75]. However, most hot-wall reactors operate with growth rates below 25 $\mu\text{m/h}$ to control the quality of the epitaxial layer [76]. In addition to the growth rate related issues, the vertical temperature gradient over the substrate leads to excessive Si supersaturation in the gas phase, causing nonuniformity in the epilayer [77]. In the hot-wall configuration, gas phase Si aggregation is minimized due to high temperature surroundings [78]. Furthermore, hot-wall reactors provide long-term stability of the growth environment, and continuous growth over 30 hours is possible with-

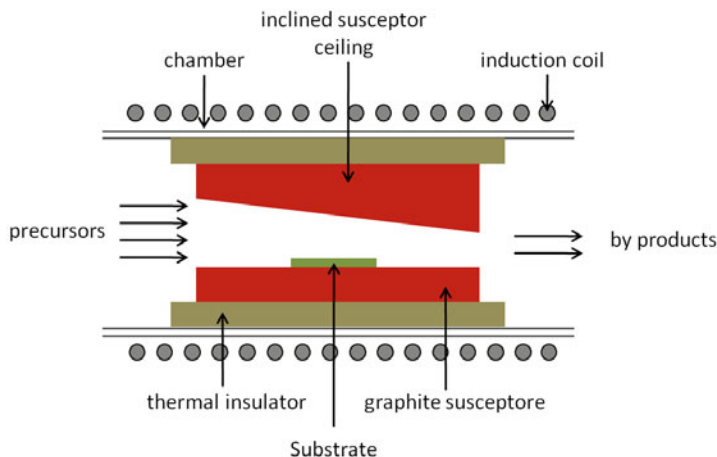


Fig. 2.17 Conceptual diagram of the horizontal hot-wall CVD reactor for epitaxial SiC.

out significant degradation of the SiC growth front [79]. These decisive advantages attracted many users to adapt to hot-wall reactor technology. Some of the widely used hot-wall reactors are discussed below.

The hot-wall reactor concept was first introduced by Kordina *et al.* in 1994 [80]. This was a horizontal geometry reactor module. Later, the reactor was further improved for highly uniform epitaxial layer growth [81]. Figure 2.17 conceptually represents the horizontal hot-wall CVD reactor. The graphite susceptor used here is a rectangular-shaped hole which runs along the entire length of the reactor with inclined ceiling. This geometry of the susceptor increases the gas velocity and reduces the depletion effect in order to grow a uniform epitaxial layer. The susceptor is encircled by thermal insulator which is placed inside an air cooled quartz tube. The thermal insulator reduces the heat loss due to radiation and consequently, hot-wall reactors consume less power (20–40 kW) than cold-wall reactors. The thermal insulator also helps maintain thermal uniformity. To date, this reactor geometry is one of the most widely used hot-wall reactor configurations.

Another hot-wall configuration called a chimney reactor has received considerable interest due to its ability to achieve high growth rates [76]. This is a vertical reactor similar to one shown schematically in Figure 2.18. It likewise has a hollow susceptor with an internal rectangular cross-section. The symmetrical nature of the susceptor provides symmetric temperature and gas flow distributions allowing the substrates to be mounted on opposing sides of the inner walls. Typically, the gas flow is upward through the reactor. The flow is facilitated by free convection due to the high temperature process. The growth rate of this reactor can be as high as 50 $\mu\text{m}/\text{hour}$. Since the high growth rate introduces more defects in the deposited film, the reactor is generally operated below 30 $\mu\text{m}/\text{h}$ to produce high quality epilayers.

The introduction of the multi wafer hot-wall planetary reactor concept can be considered a significant step towards high throughput production of SiC epitaxial

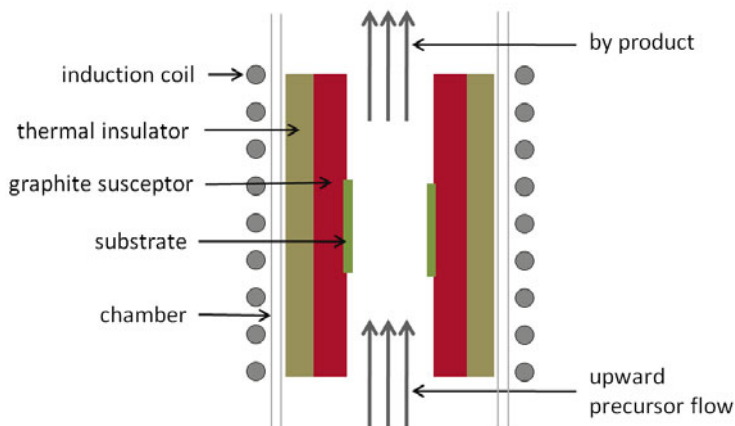


Fig. 2.18 [76] Schematic diagram of the chimney CVD reactor for epitaxial SiC (©Elsevier 2002), reprinted with permission.

wafers. The planetary reactor concept was originally developed by Frijlink *et al.* in the late 1980s for the growth of III-V compound semiconductors [82]. This design went through a few iterations [71, 83] before becoming current high throughput industrial scale SiC epi hot-wall reactor. The schematic illustration of the reactor concept is displayed in Figure 2.19. The precursors enter from the top at the center of the reactor and flow outward radially. The gas transport properties of this configuration result in a decrease in growth rate as the susceptor radius increases. The growth rate decreases because of precursor depletion as well as an increase in the boundary layer thickness due a rapid drop in gas velocity as the area increases. In this reactor configuration, this effect is successfully eliminated by the rotation of the individual wafers about their individual axes. Experimental evidence confirms achieving extremely good thickness uniformity (1.5%) and dopant uniformity (6%) over 100 mm substrates [84]. Extremely high wafer to wafer uniformity is also reported. The growth rate is typically around 10 $\mu\text{m/h}$.

A very promising hot-wall reactor concept was introduced recently for high growth rate and uniformity [85]. The highest growth rate reported in this method is 250 $\mu\text{m/h}$. Optimal epilayer conditions are achieved at lower growth rates, typically around 80 $\mu\text{m/h}$. Thickness uniformity of 1.1% and dopant uniformity of 6.7% over 100 mm substrate have been reported for this method. The reactor is essentially an improved version of the cold-wall rapid-rotation reactor. The reactor concept is schematically shown in Figure 2.20. The uniform growth is achieved by controlling the gas flow and the temperature distribution in the reactor. First, precursor gases are introduced from an off-centered inlet and the susceptor moves up and down during the growth, resulting in changes in gas flow distribution. The vertical position RF coil can also change independent of the susceptor position to control the vertical thermal distribution. Despite a promising start, the complex nature of the reactor hardware and operation has hindered the wide spread usage of this method.

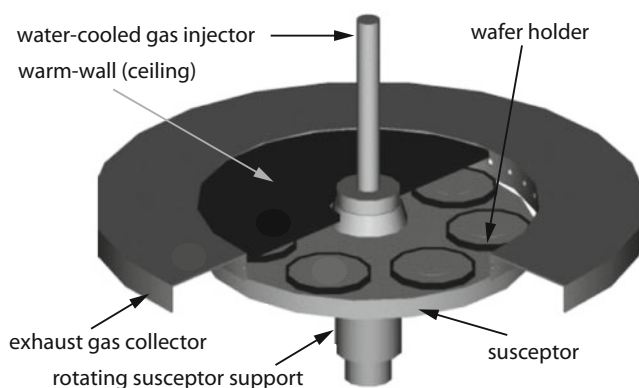


Fig. 2.19 [84] Schematic representation of the multi-wafer epitaxial SiC hot-wall reactor that uses the planetary rotation principle (©Trans. Tech. Publishing 2009), reprinted with permission.

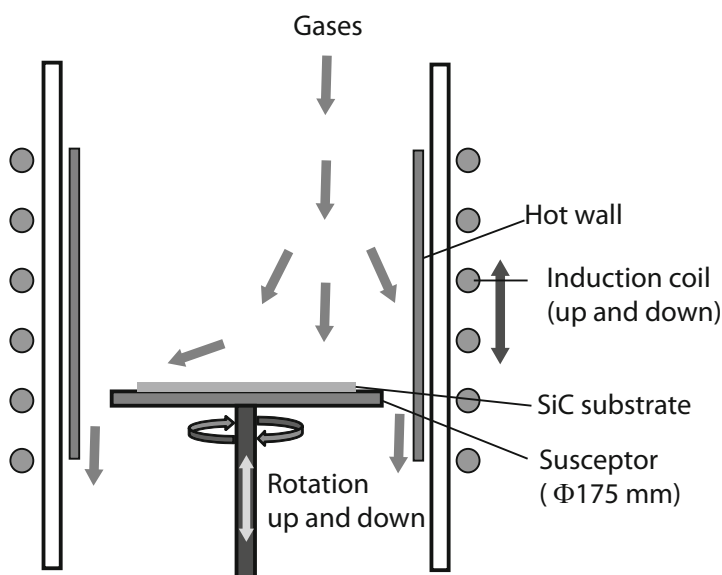


Fig. 2.20 [85] Schematic representation of epitaxial SiC reactor that uses up and down motion of the susceptor and off-centered gas delivery for optimal uniformity (©JSAP 2008), reprinted with permission.

In addition to quality and throughput improvements by novel CVD reactor designs and process optimization, the growth aspect of CVD has also been heavily studied. Two major breakthroughs in growth of SiC CVD epilayers occurred in late 1980s and early 1990s, namely step-controlled epitaxy and site competition epitaxy. These advances have had a tremendous impact on the SiC electronics industry.

Step-controlled Epitaxy: In general, growth of homoepitaxial 6H-SiC layers performed on well-oriented [0001] faces requires temperatures of 1700-1800 °C. Unfortunately, this very high temperature growth environment causes: unwanted impurity contamination from the growth system itself, redistribution of dopants through diffusion, and thermal-induced damage to the epilayer. These problems can be mitigate by lowering the growth temperature but low temperature growth conditions results in inclusion of 3C-SiC, the low temperature polytype. This polytype mixing due to 3C-SiC inclusion is a serious issue in CVD epitaxial growth of 4H- and 6H-SiC polytypes. The 3C-SiC inclusion in hexagonal epilayers is known as triangular defects as they can be distinctly identify by the triangular shape of 3C-SiC crystals. In the late 1980s, several research groups successfully grew high-quality homoepitaxial 6H-SiC with a smooth morphology without 3C-SiC incorporation at 1400-1500 °C using vicinal, or off-axis (off-oriented), substrates [86, 87, 88]. Surface steps existing on the off-oriented substrates serve as a template for replication of the underlying polytype. This technique of growing epilayers on off-axis substrates is known as step-controlled epitaxy. This technique was a significant breakthrough in homoepitaxial growth of SiC as it enabled production of device-quality epilayers with replication of substrate polytype at reduced growth temperature (>300 °C). This is beneficial in reducing contamination from the reactor wall and minimizing unwanted dopant diffusion.

Figure 2.21 schematically illustrates the epitaxial growth process on (a) a well-oriented and (b) an off-oriented 6H-SiC substrate [89]. The well oriented [0001] face consists of vast terraces and has very low step density. The growth process proceeds through two-dimensional nucleation on the terraces due to high supersaturation on the surface. The growth process is controlled by surface reactions such as adsorption and desorption. Therefore, the primary factor that determines the polytype is the growth temperature. According to ABC notation, the stacking order of 6H-SiC is ABCACB while 3C-SiC can be either ABCABC or ACBACB. When 3C-SiC grow on well-oriented face, two adjacent nucleation sites may also leads to double positioned twins as shown in Figure 2.21(a).

The off-oriented substrates possess high step density with narrow terrace width. The smaller terrace width allows the adatoms to reach the step through surface diffusion and the incorporation of the adatoms to the lattice at the step. The growth process is governed by bonds from the step resulting replication of the substrate polytype.

The initial studies on step-controlled epitaxial were performed on 6H-SiC polytype; however, later studies shows its viability to homoepitaxial growth of other polytypes including 4H-SiC [22]. The remarkable success in step control growth led to a burst in research to understand the growth mechanism and the factors affecting step-controlled growth. The growth process of step-controlled growth is found to be mass transport limited, not surface reaction limited. Therefore, supersaturation conditions should be controlled to promote mass transport limited growth and to prevent two-dimensional nucleation. Growth rate, growth temperature, and terrace width all influence the growth mechanism [89].

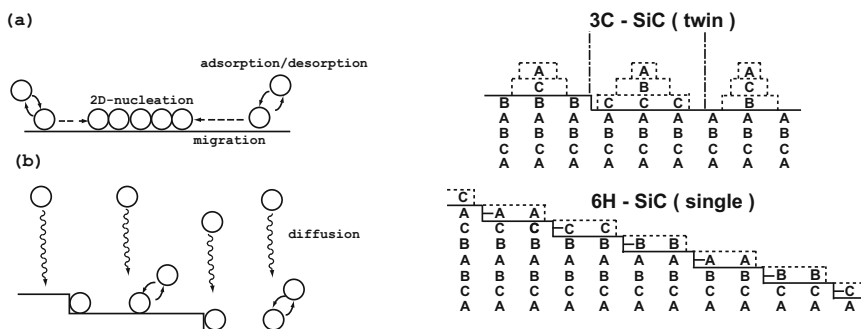


Fig. 2.21 [89] Schematic representation of the growth mechanism on (a) well-oriented and (b) off-oriented of 6H-SiC [0001] faces ((©)AIP 1994), reprinted with permission.

As the off-angle of the substrate increases, the terrace width decreases. Figure 2.22 gives the experimental data of the growth rates for various off-angles of the [0001] face of 6H-SiC substrate at 1500 °C [90]. It clearly shows 3C-SiC growth on both the Si-face and C-face of well oriented substrates at 1500 °C while homoepitaxial growth is observed on off-oriented substrates under the same experimental conditions. It is also clear that off-angle orientation as small as 1 degree can induce the step flow growth conditions. The data further reveals that surface polarity does not affect growth on off-oriented substrates. As stated in Section 2.2.3.1, 4H polytype, preferentially grow on C-face whereas 6H polytype preferentially grows on the Si-face. The nonexistence of the polarity effect on step controlled growth is attributed to the relatively low activation energy for the step controlled growth (3 kcal/mol) in comparison to that of well-oriented substrate (C-face 20 kcal/mol, Si-face 22 kcal/mol).

Site Competition Epitaxy: The precise control of dopant incorporation is essential to fully realize the intrinsic advantages of SiC for high power, high temperature, and high frequency electronics. This was a difficult task, especially in obtaining lightly-doped material because of unintentional doping that was difficult to prevent at the high deposition temperatures. The introduction of site competition epitaxy by Larkin *et al.* in early 1990s [91] provided a solution. In this method, the controlled doping is based on adjusting the C:Si ratio within the growth reactor. Earlier research pointed out that dopant atoms occupy specific sites of the SiC lattice, specifically nitrogen occupies the carbon site while aluminum occupies the silicon site [92, 93]. High C:Si ratio results in an increase in carbon concentration in the growth environment forcing a competition between nitrogen and carbon for the C-sites on active growing surface of SiC lattice. A similar situation occurs when the C:Si ratio decreases, which results in the relative increase in silicon concentration in the growth environment forcing a competition between Al and Si for Si sites on the active growing surface of the SiC lattice. Therefore, controlling C:Si ratio of the feeding gasses can be used for controlling dopant atom incorporation. This is the basis for “site-competition epitaxy.”

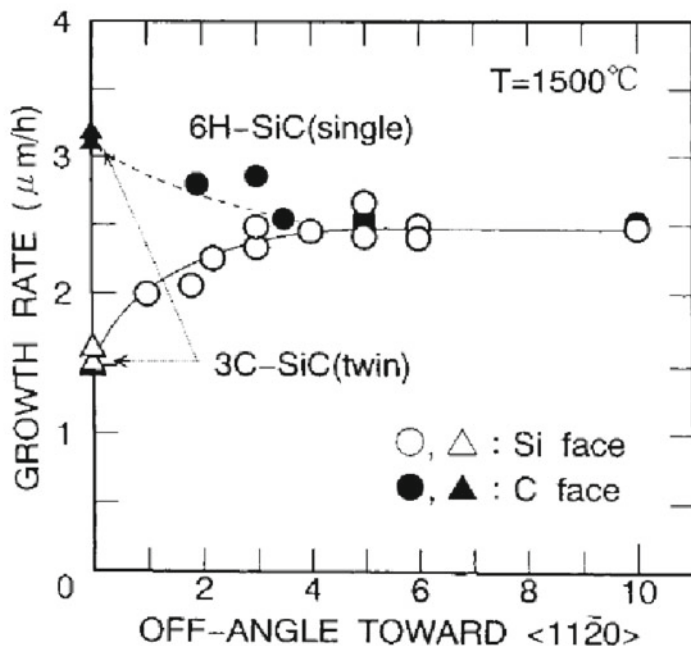


Fig. 2.22 [90] The effect of the off-angle of the substrate on the growth rate and polytype of an epitaxial SiC layer grown on 6H-SiC at 1500°C with flow rates of SiH_4 and C_3H_8 are 0.30 and 0.20 sccm, respectively. Triangles represent 3C-SiC and circles represent 6H-SiC (©AIP 1993), reprinted with permission.

Site competition epitaxy is used not only for N and Al incorporation, but also has been worked for common impurities such as boron and phosphorus [94]. This technique has been heavily implemented to control impurity levels for both intentional and unintentional dopant incorporation during the epitaxial CVD growth of 6H-, 3C-, 15R-, and 4H-SiC. For instance, when the C:Si ratio was increased from 2.3 to 10 for undoped epitaxial growth on the Si face of 6H-SiC, the layers changed from n-type to p-type due to suppression of N incorporation. This technique enables production of both p-type and n-type epilayers with carrier concentration down to 10^{14} cm^{-3} . These types of semi-insulating substrates with low carrier concentrations are desirable for high power SiC devices. Highly doped (up to 10^{20} cm^{-3}) epilayers have also been achieved by site competition epitaxy, benefitting device technologies that require low parasitic resistances.

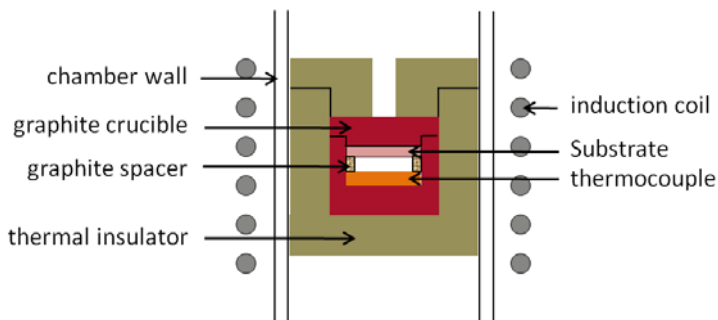


Fig. 2.23 [95] Schematic diagram of the reactor used in close space technique for epitaxial SiC growth (©Elsevier 1999), reprinted with permission.

2.3.1.2 Sublimation Epitaxy (SE)

Sublimation epitaxy (SE), sometimes referred as close space technique, involves a very similar process to the standard PVT method (modified Lely method) described previously. The SiC substrate is placed very close to the source material; the typical distance between source and substrate is around 1 mm, compared to 20 mm for standard PVT. The reactor is schematically depicted in Figure 2.23 [95]. The process is carried out at slightly lower temperatures (1800–2200 °C) and higher pressure (up to 1 atm) than standard PVT. The biggest advantage of SE over previously described CVD techniques is the capability of growing epitaxial films at very high rates — as much as 1000 $\mu\text{m/h}$ has been demonstrated [95]. One drawback to this method is that changing dopant levels or dopant type during the growth is not possible.

2.3.1.3 High-Temperature Chemical Vapor Deposition (HTCVD)

This method was initially introduced by Kordina *et al.* It shows greater promises in terms of growth rate, purity, and dopant control [23, 81]. High-Temperature Chemical Vapor Deposition (HTCVD) is suitable for both SiC epitaxy and bulk growth. A brief description on the HTCVD apparatus and the process can be found in section 2.2.1. As stated earlier, the growth process in HTCVD occurs through sublimation of gas phase nucleated Si_xC_y clusters; it greatly differs from the conventional CVD processes. The process temperature is extremely high (1800–2300 °C) and helium is used as the carrier gas to prevent etching of the susceptor by hydrogen. Growth rates as high as 800 $\mu\text{m/h}$ have been reported, and it is comparable to that of boule growth by the standard PVT method. Along with HTCVD crystal growth, this method for producing epilayer has been adapted in industrial environment [16].

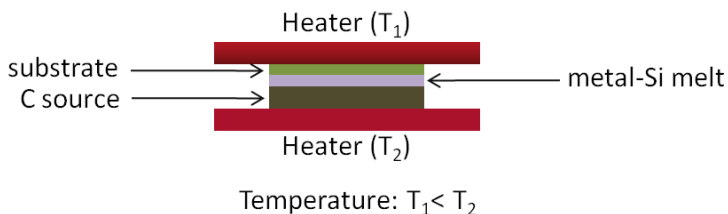


Fig. 2.24 Conceptual drawing of the sandwich configuration used for liquid phase epitaxial growth of SiC.

2.3.2 Liquid-Phase Epitaxy (LPE)

LPE was one of the widely used techniques for SiC epitaxial layer growth for device applications during the 1990s [96]. Although CVD is currently the preferred method for SiC epitaxial layer growth, recently there has been a renewed interest in LPE due to its ability to reduce the micropipe defect density. As mentioned in section 2.2.2, the growth process occurs at low temperature in equilibrium conditions and micropipe generation is not energetically favorable under these conditions. The epitaxial growth process is mainly carried out using the traveling solvent method [97, 98], in contrast to liquid phase bulk growth that primarily utilizes the top seed solution growth method. Figure 2.24 schematically represents the reactor geometry. A temperature gradient is maintained between the source and substrate to facilitate the growth process. The growth rate of LPE can be as high as $300 \mu\text{m/h}$. Both n- and p-type doping can be achieved by selecting proper source materials. A key limitation to this method is the inability to switch doping level and conductivity type during the growth [79].

2.3.3 Vapor-Liquid-Solid Epitaxy (VLS)

VLS is comparatively a new technique for growth of epitaxial SiC [99]. The growth mechanism is based on the well known VLS process of SiC nanowire or whisker growth [69]. The reactor configuration for VLS SiC epitaxial growth is depicted in Figure 2.25. A silicon melt is formed in a crucible by a combination of metal and silicon powders. There are few steps involved in the growth process, which starts with transporting of the carbon precursor (C_3H_8) to the surface of the liquid where precursor dissociation and dissolution of carbon in the silicon melt take place. Then, carbon transport from the vapor-liquid interface to the liquid-solid interface occurs where crystallization of SiC happens. The wetting properties of the substrate surface by Si melt and the height liquid droplet on the substrate is crucial for uniform growth rate. The crucible was designed in such a way that uniform droplet height is maintained to mitigate growth rate variations as shown in Figure 2.25.

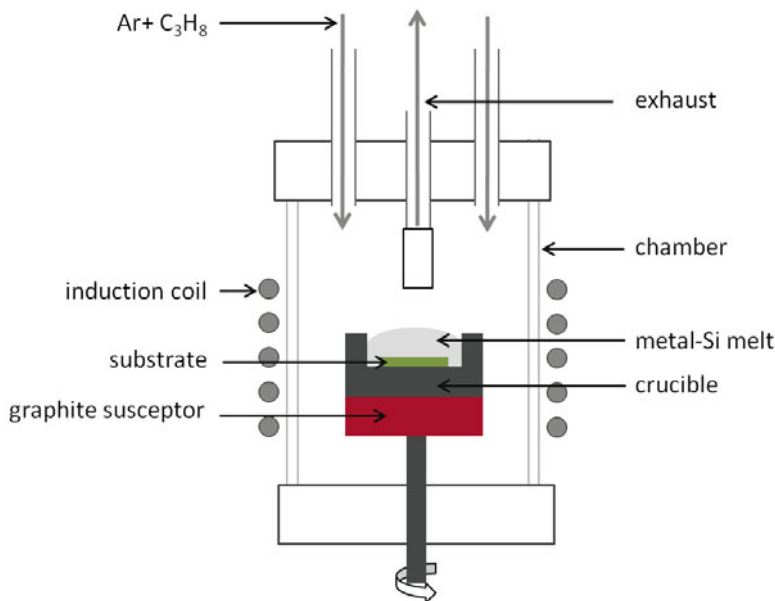


Fig. 2.25 [99] Schematic illustration of VLS growth reactor for epitaxial SiC growth (©RSC 2004), reprinted with permission.

The maximum growth rate obtained with this method is around $35 \mu\text{m/h}$. The VLS concept is still at the research stage. The commercial implementation of this method is yet to be seen.

2.3.4 Current Status of SiC Epitaxial Wafers

Table 2.2 summarizes the key features of the SiC epitaxial growth techniques discussed above. Some of the techniques are already being used in the commercial production environments while others are still at the research stage. Most industrial production of SiC epitaxial films produces 4H- and 6H-SiC polytypes. Both n- and p-type doping are available with a wide range of carrier concentrations (9×10^{14} to $1 \times 10^{19}/\text{cm}^3$) and doping uniformity better than 10% over a 4 inch substrate. Thicknesses up to 50 microns are routinely produced with thickness uniformity better than 2% [13, 100, 101]. Despite commercial availability and wide spread usage of epitaxial SiC layers, there still remain many challenges to eliminate defects in epilayers. For example, micropipe formation due to substrate imperfections is yet to be solved. Even though 3C-SiC inclusion is suppressed to an acceptable limit by step controlled growth, further improvement in this area is desirable.

Table 2.2 Key features of the current SiC epitaxial growth techniques

Technique	Growth Temp. (°C)	Growth rate ($\mu\text{m/h}$)	Comments	Ref.
CVD	1400-1500	25	Adopted in commercial environments, Growth rate can be as high as $100\mu\text{m/h}$	[76]
SE	1800-2000	1000	Changing doping level and switching conductivity type during growth not possible	[95]
HTCVD	1800-2300	800	Adopted in commercial environments	[16]
LPE	1700-1800	300	Changing doping level and switching conductivity type during growth not possible	[97]
VLS	1500-1600	35	At initial research stage	[99]

2.4 Polycrystalline SiC and Amorphous SiC Films

SiC MEMS technology is today dominated by poly-crystalline 3C-SiC (Poly-SiC). Poly-SiC growth does not require an epitaxial alignment and consequently the high temperature pre-carbonization can be avoided. This allows the growth of poly-SiC on variety of substrate materials. Common substrate materials include single-crystalline silicon and single-crystalline SiC as well as silicon dioxide, silicon nitride, and polysilicon thin films [102, 103]. The ability to grow on substrates other than SiC offers great flexibility in device fabrication using poly-SiC. The ability to deposit at lower temperatures minimizes the temperature mismatch between SiC structural layers and the underlying sacrificial or isolation layers. From a fabrication flexibility perspective, it enhances the ability of achieving complex MEMS structures through surface-micromachining as poly-SiC can deposit on a wide range of sacrificial and isolation materials [106]. The low temperature deposition also permits the use of the poly-SiC layer as a protective coating for MEMS devices fabricated using other materials such as polysilicon [104, 105].

Initially, APCVD reactors used for epitaxial SiC growth were adapted for poly-SiC deposition [107, 108]. Later, as the process matured, various reactor configurations as well as wide range of deposition techniques were introduced for poly-SiC. LPCVD is currently the leading deposition technology for poly-SiC. However, other techniques are also used to produce poly-SiC including PECVD, magnetron sputtering, ion-beam sputtering, and ion implantation. Each of these techniques has its own advantages and disadvantages with regards to control of electrical and mechanical properties and deposition characteristics. Later in this chapter, each of these techniques will be detailed briefly.

Amorphous SiC (a-SiC) retains most of the chemical and mechanical properties of poly-SiC and has been used for many MEMS structures. In particular, the ability to deposit at very low temperatures is attractive from an integration point of view. All the techniques used for poly-SiC deposition can also be used to deposit a-SiC, and depending on the technique, the deposition temperature can be as low as 25 °C. This even allows use of polymeric layers or heat sensitive materials as sacrificial or isolation layers. Furthermore, it can also be used as a coating material to enhance the chemical resistance of MEMS made using other materials. Currently, PECVD is

the dominant technique for producing a-SiC; however, newly emerging techniques such as ion-beam assisted deposition show promise with regards to deposition characteristics such as line-of-sight deposition and no hydrogen in the deposited film.

The remainder of this section will detail various deposition techniques mentioned above and outline advantages and disadvantages of each.

2.4.1 APCVD

APCVD was the primary technique used for deposition of poly-SiC during the early phase of SiC MEMS technology. APCVD was the natural choice at that time because it was widely used in epitaxial growth of SiC films for electronics. So extending that knowledge to poly-SiC deposition was relatively easy. Most APCVD poly growth is carried out using reactors that were originally used for 3C-SiC heteroepitaxial growth on Si [107, 108, 109]. Both vertical and horizontal reactors are used. The growth can be accomplished either by dual precursors such as silane and propane as the Si- and C-containing precursor gases [108] or by using a single precursor such as hexamethyldisilane (HMDS) [109, 110]. In both cases H_2 is used as the carrier gas, and stoichiometric poly-SiC films on Si wafers are achieved at temperatures above 1050 °C.

At the initial phase of SiC MEMS, APCVD played a critical role in demonstrating the suitability of poly-SiC thin film technology for harsh environment MEMS applications. It was successfully used to produce MEMS-grade poly-SiC films. Nonetheless, commercial implementation of APCVD for SiC MEMS is hindered by some inherent disadvantages with regards to scaling up the process volume and lowering growth temperature. APCVD SiC reactors use inductively heated graphite susceptors similar to those shown in section 2.3.1.1. This restricts the substrate size and reactor load, limiting throughput. The deposition temperature is over 1050 °C, which is not suitable for depositing poly-SiC on wide range of materials. Furthermore, the high deposition temperature is also a concern for monolithic integration with ICs. In order to address these issues, LPCVD and PECVD methods were proposed.

2.4.2 LPCVD

LPCVD is a well established technique in silicon semiconductor and MEMS processing. This technique offers precise control of gas transport properties compared to APCVD, permitting deposition of thin films with excellent uniformity and extremely good step coverage. These characteristics are highly critical factors for MEMS fabrication. Moreover, excellent purity, large-size wafer capability, and multi-wafer capacity of LPCVD reactors are attractive for high throughput production of high quality films.

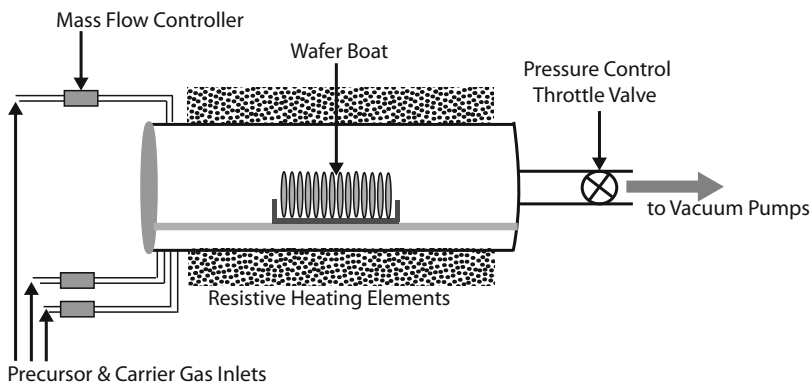


Fig. 2.26 Schematic diagram of a high throughput large diameter hot-wall LPCVD reactor.

Over many years, a large number of feasibility studies, done in small scale reactors, have proven the usefulness of LPCVD as a method for poly-SiC thin film growth [112, 113, 114, 115, 116, 117]. Those studies have shown that LPCVD offers the flexibility to grow poly-SiC films that have a wide range of electrical, mechanical, and chemical characteristics. Encouraged by these initial results, recent efforts have been focused on developing process for poly-SiC deposition in large area multi-wafer reactors. Zorman *et al.* were the first to report depositing poly-SiC films on 100 mm diameter silicon substrates in a reactor capable of handling 100 wafers at a time [118]. From then on, a tremendous amount of research has been performed to optimize deposition parameters and increase throughput. Today, LPCVD processes are available for substrates as large as 150 mm in diameter. The optimization of LPCVD processes to improve film properties for specialized applications continues to be an active area of research.

Figure 2.26 is a schematic illustration of a hot-wall LPCVD reactor used in poly-SiC growth. The reactor is resistively heated as opposed to inductive heating in APCVD. Nitrogen and hydrogen are commonly used as carrier gases. The reactors are very similar to the reactors used in poly-Si processes, except that the temperature of poly-SiC reactors can go as high as 1200 °C. The deposition temperature varies with process conditions and precursor type.

A wide array of single and dual precursors has been exploited for poly-SiC. Single precursor includes disilabutane (DSB), trimethylsilane, and hexamethyldisilazane (HMDS). As for the dual precursor, silane and dichlorosilane are commonly used as the silicon precursor while methane, butane, and acetylene are used as carbon precursor. As the process optimization is based on precursor type, the following discussion is mostly limited to precursors that have reasonably well developed processes for poly-SiC based MEMS production.

For single precursor poly-SiC growth, 1,3 disilabutane (DSB) is the most explored to date. It is capable of producing high quality poly-SiC around 800 °C and can be used to deposit a-SiC at temperatures as low as 650 °C [116, 117]. One of the notable distinctions for DSB is the high growth rate, which can be as high

as 55nm/min at 800 °C [116]. There is an extensive set of data available with regards to process conditions as well as the electrical and mechanical properties of the poly-SiC films deposited using DSB [119, 120, 121, 122]. For instance, in-situ nitrogen doped films show resistivity as low as 0.02 Ω -cm [120] and carrier concentrations up to $6.8 \times 10^{17} \text{ cm}^{-3}$ [123]. One of the key deposition characteristics of DSB-based LPCVD is the highly conformal nature. The low temperature deposition along with highly conformal deposition characteristics is highly desirable for wear and chemical resistive coatings for released MEMS structures. Some examples include wear resistive coating on microscale engine components fabricated using silicon [124] and a chemically resistive coating of a silicon double ended tuning fork resonator [125] and capacitive strain gauge [126]. As for a structural material for MEMS, poly-SiC deposited using DSB has been used for many functional MEMS structures such as Lamé mode filters [127].

Single source precursors such as methylsilane [103], trimethylsilane, and HMDS [109] have similar potential as a source material for LPCVD poly-SiC. Methylsilane has been recently used in a large diameter multi-wafer format LPCVD reactor [128]. Key advantages of using methylsilane as a single precursor over DSB are that it is readily available and is substantially less expensive. In terms of deposition temperature, methylsilane can also produce poly-SiC at 800 °C. Initial results show great promise with regards to electrical and mechanical property control. Nitrogen doped films made using methylsilane exhibit resistivities comparable to DSB deposited films [129]. Based on current status, methylsilane is a sound single precursor that needs attention from poly-SiC developers.

The combination of dichlorosilane (SiH_2Cl_2) and acetylene (C_2H_2) dominates dual precursor based LPCVD poly-SiC deposition because of its early start and well characterized processes for MEMS grade films. The deposition temperature for MEMS grade poly-SiC using this gas chemistry is 900 °C. Starting with a feasibility study by Wang *et. al*, this gas combination was quickly adapted to poly-SiC deposition on large area (100-150 mm) wafers in multi-wafer LPCVD reactors [118]. From then on, LPCVD deposition with SiH_2Cl_2 and C_2H_2 has played a crucial role in SiC MEMS development. Extensive research has been performed on this precursor combination for many years, so there exists a vast knowledge base on process conditions and corresponding material properties. Outstanding stress control over a wide range from high tensile to medium compressive, including crossing zero stress, has been achieved. In terms of n type doping, the nitrogen atomic concentration up to of $2.6 \times 10^{20}/\text{cm}^3$ and resistivity down to 0.02 Ω -cm have been reported [130]. In terms of technological maturity, the process using this dual precursor system is ready for wide spread use. Most of the MEMS devices discussed in Chapter 4 have been fabricated using thin films deposited with this technique. High-temperature, shock-resistance strain gauge [131], harsh environment accelerometer [132], and pressure sensor for in-cylinder pressure measurements [133] are but a few.

Despite new PECVD and other physical vapor deposition methods emerging for creating poly-SiC films, to date LPCVD has become the gold standard technique for poly-SiC MEMS mainly because of the relentless push towards achieving high quality films with reproducible electrical and mechanical properties. In the next sec-

tion, process parameters that are used for controlling highly critical factors such as doping, residual stress, and strain gradient of LPCVD poly-SiC films will be discussed.

2.4.2.1 Doping of LPCVD Poly-SiC Films

For many MEMS applications, poly-SiC with tunable levels of conductivity are either highly desired or required. As mentioned in Chapter 1, diffusion doping is not an option for SiC, and the controlled inclusion of impurity atoms is accomplished through the addition of a dopant precursor to the reactor during the growth. With regards to MEMS applications, the conductivity takes precedence over the impurity type (n or p). Therefore, in most cases, n-type doping with nitrogen is preferred for poly-SiC due to processing ease. Furthermore, nitrogen has the shallowest ionization energy in SiC comparison to other dopant atoms such as phosphorus, aluminum, and boron [1].

Doping of epitaxial as well as bulk growth of SiC are routinely done using gaseous nitrogen and ammonia [134, 135]. However, dopant incorporation in MEMS-grade poly-SiC is relatively difficult due to low temperature deposition requirements along with the required material characteristics of the poly-SiC. First, the doping precursor must decompose at low temperatures. The existence of grain boundaries in poly-SiC also complicates dopant incorporation and carrier transport at low temperature. The trapping of dopant atoms in grain boundaries and reduction of adatom mobility directly affects the growth process, resulting in changes in the film properties [119, 136, 137].

There were many concurrent studies on doping low-temperature-deposited poly-SiC using ammonia. The first successful attempt was reported by Wijesundara *et al.* for doping of poly-SiC grown by DSB at 850 °C [119]. Resistivity down to 0.02 Ω -cm was achieved. Later, doping of poly-SiC at growth temperature as low as 800 °C was demonstrated confirming the practicality of NH_3 as a doping precursor for low temperature deposition of poly-SiC [124]. Figure 2.27 shows the resistivity changes due to increase in ammonia in the feed gas. Currently, NH_3 is being used as the dopant precursor for poly-SiC deposited from both single and dual precursor deposition systems [130, 129].

The key challenge in doping poly-SiC is to optimize electrical properties while keeping the desired mechanical properties for MEMS applications. It is shown that doping can lead to changes in the growth characteristics such as growth rate, degree of crystallinity, grain size, and residual stress as well as influences the Young's Modulus of poly-SiC. Changes in the degree of crystalline quality due to doping variations was initially observed by Wijesundara *et al.* [119]. This was further confirmed by Zhang *et al.* showing a decrease in the lattice constant as doping concentration increases [123]. Furthermore, recent studies show that changes in grain size due to doping influences the quality factor of flexural-mode poly-crystalline silicon carbide (SiC) lateral resonators [136]. These results shows that mechanical properties and the doping level of poly-SiC are intertwined, and it is important to optimize both

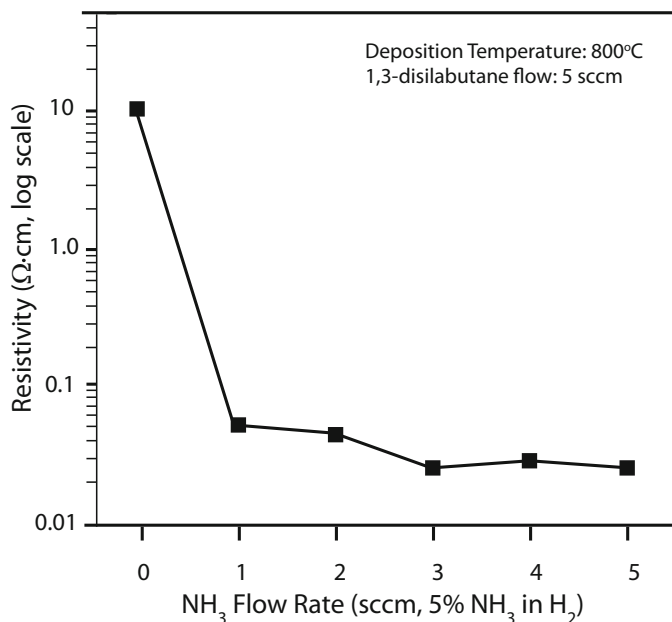


Fig. 2.27 [124] The resistivity variation of poly-SiC films deposited at 800 °C as a function of the NH₃ (dopant precursor) flow rate (©Elsevier 2003), reprinted with permission.

electrical and mechanical properties together for the realization of poly-SiC MEMS devices. These studies also suggest that doping can be used as a tool for tailoring device characteristics.

2.4.2.2 Residual Stress and Stress Gradient Control on LPCVD poly-SiC

As mentioned at the beginning of the chapter, the residual stress and stress gradient are two highly critical factors that have to be addressed at the materials level in order to realize MEMS devices. Processes have to be developed to reduce both the average stress and stress gradient such that they are sufficiently small to be useful in creating free-standing microstructures that do not break, buckle, or curve out of plane. The control of these two parameters in poly-SiC thin films is very challenging due to several reasons. First, deposition is done on top of different materials with varying thermal properties. The thermal mismatch and elevated deposition temperatures cause thermal induced stress at room temperature. Lowering the deposition temperature and selecting substrates and interlayer materials with similar thermal expansion can be helpful. However, for LPCVD deposition, the temperature is primarily dictated by the precursor used. The material selection is governed by the poly-SiC surface micromachining technology. Currently, polysilicon, silicon dioxide, and silicon nitride are the primary set of materials used in poly-SiC micromachining. Therefore,

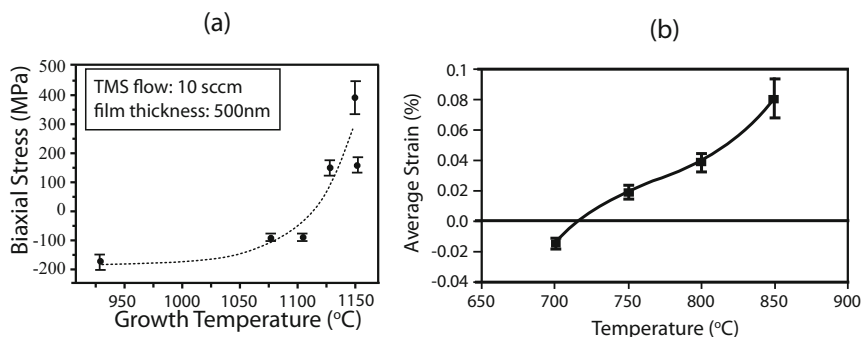


Fig. 2.28 [113, 121] Influence of deposition temperature on the average stress of LPCVD poly-SiC thin films deposited using (left) Tetramethylsilane (TMS) (©AIP 2000) and (right) 1-3 disilabutane (DSB) showing zero-crossing (©SPIE 2003), reprinted with permission.

the material choice is rather limited. The other factor which highly influences the stress and stress gradient of deposited film is the microstructure of the film. Typically, poly-SiC growth occurs with a columnar or grain structure. The size of grains or columns has a strong correlation to residual stress. Furthermore, the grain or column size vary as the growth progresses, resulting in variation in stress through the film thickness, causing strain gradient.

The deposition temperature has been one parameter explored for controlling both residual stress and stress gradient as it has a direct relation to the microstructural properties of the films including grain, column, and crystallinity. Figure 2.28 displays the temperature dependence of poly-SiC films deposited by (a) tetramethylsilane and (b) DSB [113, 121]. Temperature can be used to change thin film stress from highly compressive to medium compressive to tensile, including crossing the zero stress point. However, temperature alone cannot be used to optimize MEMS films as it also changes other parameters such as resistivity and crystallinity.

One notable development in controlling the film stress is reported for dual precursor poly-SiC deposition is to control deposition pressure [138]. Pressure influences the gas transport property of the reactor thereby causing microstructural changes, specifically grain or column size. In this case, low stress poly-SiC films were obtained while keeping the stoichiometry, crystallinity, and resistivity at optimal conditions. Figure 2.29 shows the residual stress versus pressure for films deposited at 900 °C using SiH_2Cl_2 and C_2H_2 .

Other aspects of changing deposition parameters have also been investigated. Roper *et al.* reports that changes in the C:Si ratio has an effect on the stress levels of poly-SiC deposited using DSB [139]. Adding small amounts of SiH_2Cl_2 to a reactor during deposition changes the elemental composition and grain size of the resulting film, thereby changing the stress level.

The cause for a variation in stress through the thickness of a material is mainly attributed to changes in the stress level of the films as a function of microstructure variation along the thickness. Structural changes have been observed for both

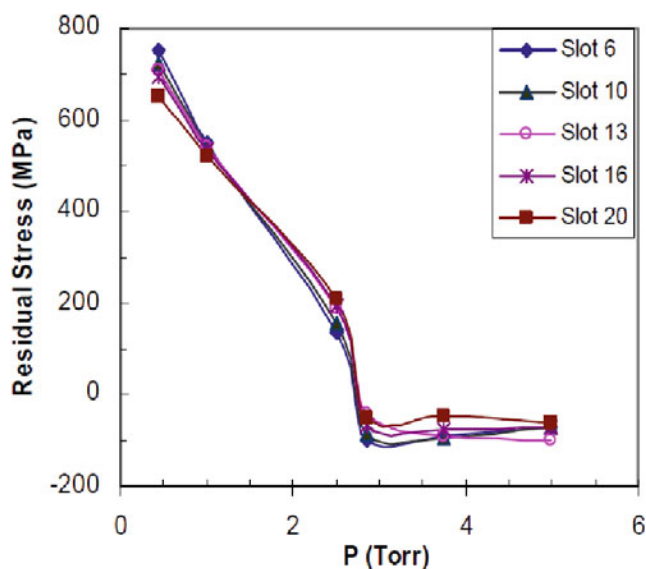


Fig. 2.29 [138] Residual stress as a function of deposition pressure for poly-SiC films deposited at 900 °C using SiH_2Cl_2 and C_2H_2 (5% in H_2) (©Trans Tech Publications 2004), reprinted with permission.

columnar and grain growth of poly-SiC as the thickness increases. Figure 2.30 is a TEM image of poly-SiC interface grown on a SiO_2 substrate [110]. It clearly indicates the column size varies as the thickness increases. For grain growth, a similar behavior was observed by Fu *et al.* for poly-SiC grown on a SiC substrate [140]. One successful approach to suppress this structural variation is by disrupting the growth process. Deposition can be done in few successive runs in order to stop the continuation of underline grains or columns. Another way of addressing this issue is layer by layer deposition with each different layer having different doping levels to further modulate the stress. More detail on this process can be found elsewhere [141].

Even though there is room for further optimization and development, LPCVD poly-SiC has matured to a level that makes it useful for many MEMS applications. At this stage, the majority of poly-SiC MEMS are still limited to academic research institutions (Figure 2.31). The transition of academic poly-SiC processes for MEMS to commercial production of SiC microsystems is gated by unavailability of supporting SiC electronics.

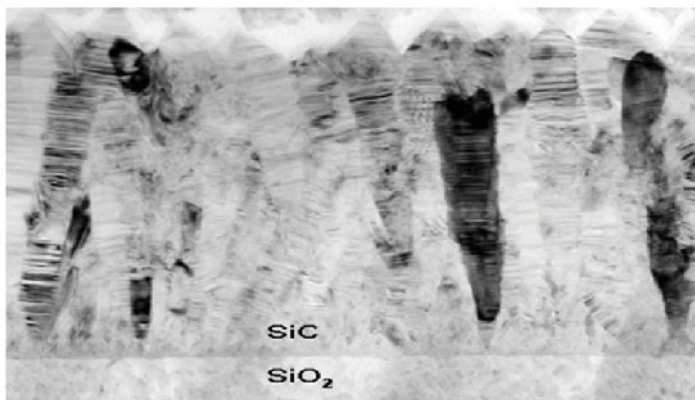


Fig. 2.30 [110] TEM image of poly-SiC grown on SiO₂ showing the variation of the size with film thickness (©Elsevier 2009), reprinted with permission.

2.4.3 PECVD

As a structural material for harsh environment MEMS, PECVD deposited amorphous SiC (a-SiC) exhibits the desired chemical and mechanical properties [143]. PECVD deposition of a-SiC has drawn significant interest because of its very low deposition temperatures (<600 °C). This enables integration of a-SiC into a wide range of substrates, making PECVD an important technique for SiC microsystem fabrication.

The main areas that may heavily benefit from the use of PECVD a-SiC include device encapsulation, protective coatings, and forming dielectric layers. As with the deposition techniques described earlier, the film properties largely depend on the deposition conditions. Depending on the specific application and maximum thermal budget allowed, deposition parameters can be used to tailor film properties.

In general, SiC PECVD is performed in conventional PECVD reactors with heated substrate holders [144]. Methane and silane are commonly used precursors [144, 145, 146]. It is also possible to use a single precursor such as DSB or methylsilane. The film properties strongly depend on the process parameters including deposition temperature, pressure, plasma power, and gas phase composition. In general, PECVD films exhibit compressive stress but process conditions can be optimized to tailor the stress levels to desired values. Typically, low plasma power and high temperature conditions yield low stress films. Sometimes post-deposition annealing at temperatures between 450 and 600 °C may still be required to reduce stress levels [143].

PECVD deposition of a-SiC can be used as a scaffolding layer as well as the final sealing layer for MEMS devices (see Chapter 5). Early studies demonstrated PECVD a-SiC for encapsulation of membranes. Figure 2.32 shows a SEM image

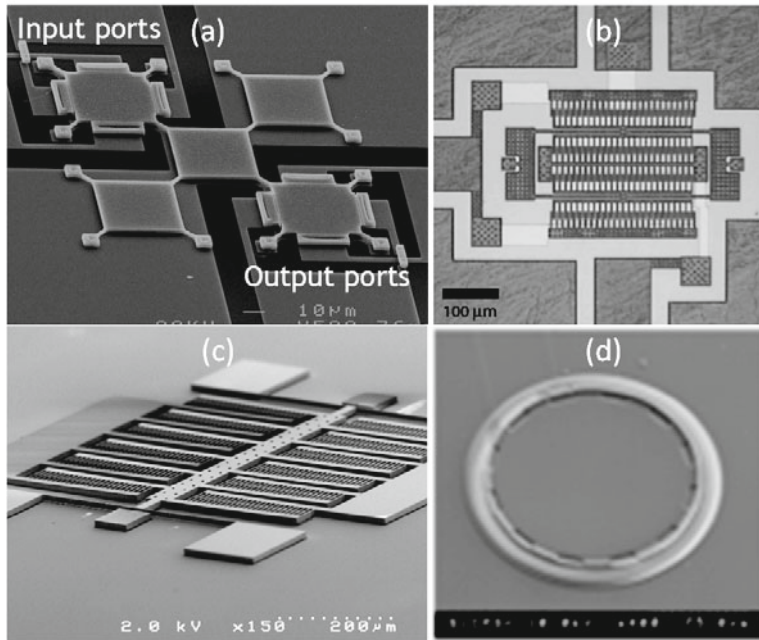


Fig. 2.31 Some of the notable poly-SiC MEMS devices fabricated at various research institutes: (a) a checkerboard filter fabricated using a array of Lamé mode resonators with center frequency of 175 MHz [127], (b) double-ended tuning fork resonant strain gauge that works at 500 °C and survive at 64,000 g shock load [131], capacitive accelerometer for range of 5,000 g [132], and pressure sensor that operates at 575 °C [133]. (©IEEE 2005, SPIE 2009, Trans Tech Publications 2009, Elsevier 2008), reprinted with permission.

of the top-view of a cleaved circular membrane created by PECVD a-SiC encapsulation [147]. These examples demonstrated the potential of PECVD deposited a-SiC. However, as deposited, a-SiC is not conductive enough to become a standalone MEMS material.

2.4.4 Ion Beam Assisted Deposition

Ion beam assisted deposition (IBAD) utilizes physical wafer deposition combined with concurrent ion bombardment to create thin films. The physical wafer deposition technique can be either sputtering or evaporation. Figure 2.33 shows a schematic diagram of an IBAD system equipped with a sputtering ion source (deposition source) and an assist source (ion bombardment source). The role of the assist source can vary depending on the application needs. In some instances, it can be used to densify the deposited film or to create a modified interface between substrate and deposited film. In both cases, ions from a noble gas such as argon are used. This mode of

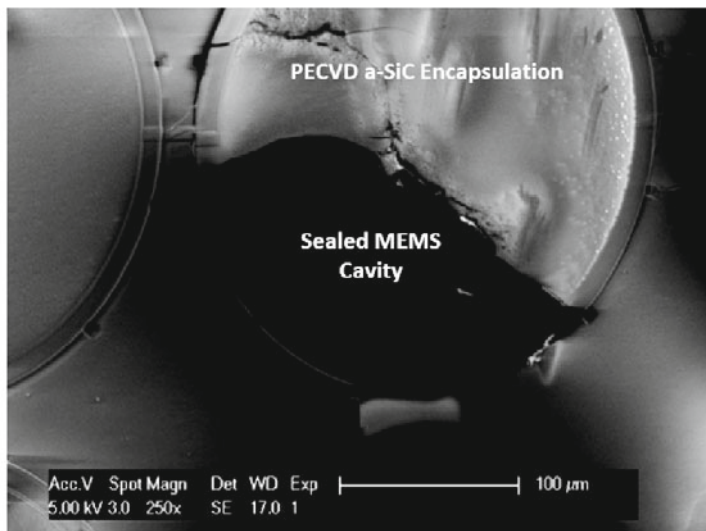


Fig. 4. Top-view of a cleaved circular PECVD a-SiC encapsulation

Fig. 2.32 [147] Top view of cleaved encapsulation membrane fabricated using PECVD a-SiC (©IEEE 2009), reprinted with permission.

operation is suited for depositing single element layers, such as metals. However, if the assist source provide reactive ions to the growing surface, it creates compound materials. In this case, typically, a metal is evaporated or sputtered while the growth surface is continuously bombarded with reactive ions, such as oxygen or nitrogen ions to create metal oxides and nitrides. Currently, IBAD thin films are widely used as magnetic thin films, protective coatings, and hard coatings [148].

To form compound films such as SiC using ion beam sputtering, typically dual ion beam systems are used with separate targets for each type of element [149]. Multiple targets are used because ion beam sputtering is not well suited for sputtering compound material targets such as SiC due to preferential sputtering of one element over the other [150]. That leads to the formation of nonstoichiometric films. However, it has been shown that if a SiC target is sputtered with ion energy around 1200 eV, the sputtering yields 1:1 ratio of silicon to carbon [151]. Encouraged by this observation, an IBAD system was developed for low temperature deposition of a-SiC [152]. This system (Figure 2.33) consists of two ion guns, a target holder, and a substrate holder. The ion energy range of the sputter gun is between 500 and 1500 eV and argon is used as the sputtering gas. The assist ion gun ranges from 50-500 eV. The role of the assist gun in SiC MEMS thin film deposition is for stoichiometric fine tuning of the films as well as strain gradient control of the deposited film [153]. The typical deposition rate of this type of system varies from 5 to 15 nm/min and is a function of the ion fluence of the sputtering source.

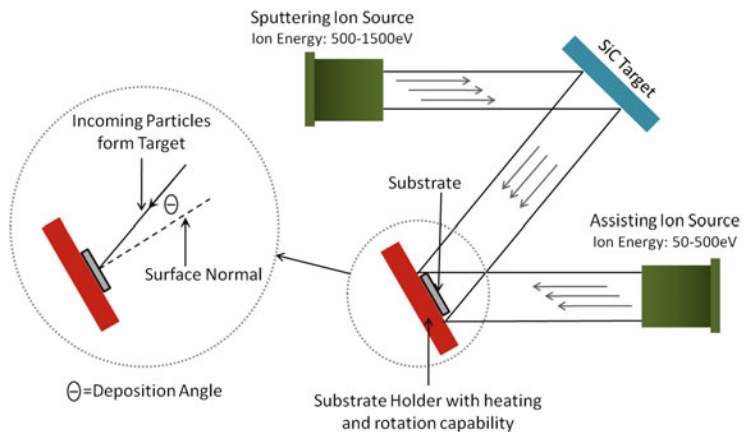


Fig. 2.33 Schematic representation of ion assisted SiC deposition system with definition of the deposition angle.

Films can be created at room temperature or at high temperature with a heated substrate holder. The film stress is compressive in nature and the stress levels decrease as the temperature increases. The deposition pressure also has an effect on stress levels. Typically, higher deposition pressure reduces compressive stress. Deposition angle, θ , also has a huge impact on the stress levels. As θ increases, the compressive stress decreases due to changes in packing density. Assisting ions also increase the compressive stress due to film densification. Therefore, it is desired to do deposition without assisting ions, unless demanded for stoichiometric fine tuning or strain gradient control.

A unique characteristic to ion beam sputter deposition is the high directionality of sputtered particles coming out of the target. This is due to the use of collimated ion beam for sputtering. Therefore, the IBAD technique allows line-of-sight deposition, which is highly advantageous for etch hole sealing during encapsulation in comparison to other physical and chemical vapor deposition techniques.

Typical zero level encapsulation schemes deposit a sealing layer on a porous scaffold film after releasing the underlying MEMS device (see Chapter 5) [154]. Currently, CVD is the main technique employed for sealing the scaffolding layer [154]. In some instances, PECVD and material reflow methods have also been investigated [132, 155]. Despite being a widely used technique, CVD tends to mass load the released MEMS devices due to the conformal nature of the deposition [156]. IBAD enables etch hole sealing without unwanted mass loading of released MEMS structures because of its inherent line-of-sight deposition capability. The preliminary results of IBAD for etch hole sealing highlight its potential. Figure 2.34 represents the deposition characteristics of IBAD based etch hole sealing. Results clearly indicate no visible side-wall or down-hole deposition of SiC.

IBAD for a-SiC is still at an early stage of development. As shown in Figure 2.34, it has a tremendous potential for wafer level encapsulation [152]. Since the deposi-

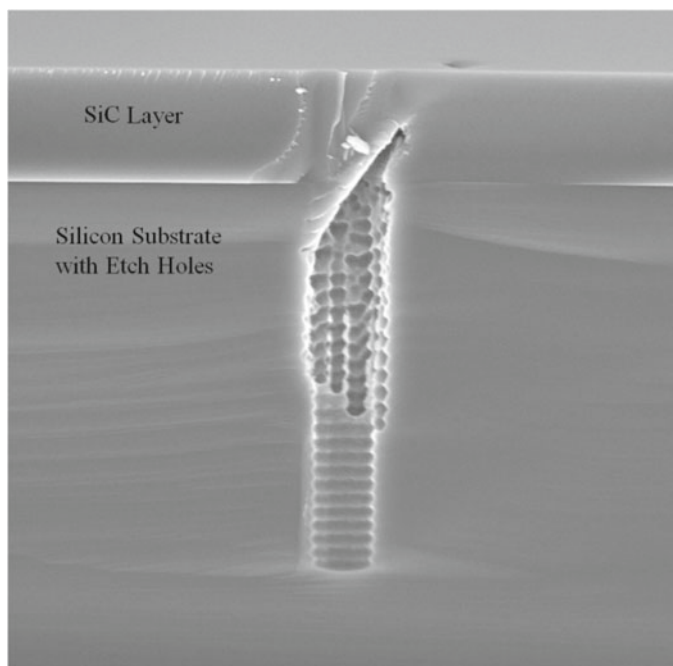


Fig. 2.34 [152] Cross-sectional SEM image of a sealed etch hole with deposition angle of 50 degrees showing no visible deposition on sidewalls and the bottom of the substrate (©IEEE 2007), reprinted with permission.

tion is typically carried out at pressures on the order of 10^{-6} Torr, this method would be highly attractive for vacuum encapsulation as the low cavity pressure drastically reduces air damping of vibrating MEMS devices. Furthermore, line-of-sight deposition can be used for creating unique MEMS devices such as 3D microstructures by using shadow mask techniques. Despite the lower deposition temperature of an IBAD a-SiC film, it does not contain hydrogen as opposed to PECVD. Hydrogen-free films are highly attractive for high temperature applications due to its high thermal stability.

2.4.5 Other Deposition Methods

Poly-SiC and a-SiC can be deposited using wide variety of techniques. Magnetron sputtering is an attractive technique for SiC since it is a low temperature deposition method very similar to PECVD. However, studies have yet to be focused on utilizing this technique for MEMS grade poly- or amorphous-SiC. Some limited studies on the deposition of a-SiC demonstrates that it is possible to achieve stoichiometric SiC by magnetron sputtering [157]. Exploring this technique as an alternative to PECVD

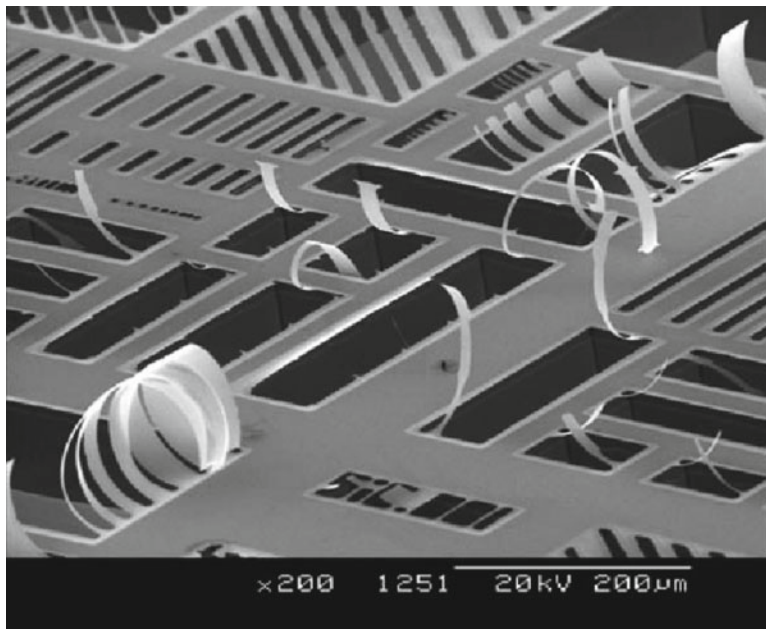


Fig. 2.35 [158] SEM topograph of a released MEMS test structure fabricated using C ion implantation of polysilicon (©IOP 2000), reprinted with permission.

would be beneficial because it enables producing hydrogen free a-SiC films at lower temperature. Further studies need to be focused on controlling of mechanical and electrical properties of the SiC films.

Serre *et al.* reported direct synthesis of SiC microstructures by implanting carbon ions through a shadow mask into a SiC substrate [158]. This is a very attractive process as it allows creation of MEMS devices without etching SiC films. When SOI wafers are used, the top Si layer is converted to SiC by ion implantation, and the underlying oxide layer can be used as sacrificial layer. Figure 2.35 displays a SEM image of a fabricated microstructure using this method. As evident by the SEM images, stress and stress gradient control of the films is an issue. The implantation leads to dislocating atoms in close proximity and densification of the film leading to increased film stress. Further research in this area is needed to mitigate stress factors and understand thickness limitations of this method.

At the current stage of SiC MEMS technology, CVD SiC deposition techniques are mature enough to support fabrication of complex microstructures that are similar to silicon MEMS. However, the advancement of SiC MEMS demands new deposition techniques that will enhance the prospect of achieving an all SiC microsystem. More specifically, it is highly critical to examine low temperature deposition processes because it allows fabrication of MEMS devices on top of electronics without violating the overall thermal budget of the electronic circuitry.

2.5 Patterning of SiC

The creation of microstructural features by selectively removing SiC films or bulk materials is essential for each device layer of the microsystem. However, high chemical inertness, owing to high bond strength between the silicon and carbon, makes sculpting of SiC quite difficult. This imposes an extra burden on selecting a patterning method, masking materials, and sacrificial layers in order to create microdevices.

Etching, molding, milling, and ablation can be used for micropatterning of SiC materials. As for etching, both dry and wet chemical etch processes have been exploited. Molding of microstructural elements is seen as a way to overcome the patterning difficulties that arise from the high chemical inertness of SiC. Ion milling techniques, such as FIB (focused ion beam), provide opportunities for creating high precision submicron features; however, the serial nature of the process limits the throughput and complexity of structures. Laser ablation of SiC is faster in comparison to FIB but its ability of making microstructures with fine geometric control has yet to be demonstrated. The following section will review the most commonly used methods for selective patterning of SiC thin films and bulk materials.

2.5.1 Dry Etching of SiC

Dry etching of SiC is mainly achieved through plasma-based reactive ion etching (RIE). This method is the primary method used to selectively etch SiC for device fabrication today. RIE dry etching provides precise control of linewidth, sidewall, and surface profile. The removal of SiC in RIE occurs through a combination of physical and chemical processes. Physical sputtering occurs through bombardment of the surface with energetic particles ejected from the plasma. Chemical etching occurs through reaction of active chemical species present in the plasma with surface species. Controlling of these two competing processes are essential for creating an etch profile with the desired side-wall angle and surface finish. Therefore, the selection of reactor type, the process conditions, and gas chemistries are extremely critical.

Various etch chemistries have been developed for plasma-based SiC etching. Most processes have been centered on fluorine based chemistries. Fluorinated compounds such as CHF_3 , CBrF_3 , CF_4 , SF_6 , and NF_3 mixed with O_2 have been successfully implemented [159, 160, 161]. However, SF_6 and O_2 is the most researched gas combination for Si etching, widely deployed in both research and industrial environments [159]. Hence, it is an obvious choice to explore for SiC etching. Some of the probable chemical reactions associated with SiC etching in a plasma containing fluorine and oxygen is given in equation (2.4), (2.5) and (2.6) [159].



The presence of oxygen in a fluorinated plasma facilitates the SiC etch process in several ways. From Eq. (2.6), it is apparent that it is directly involved in the removal of C from SiC. Furthermore, the atomic oxygen in the plasma reacts with unsaturated fluoride species to generate reactive F atoms. Therefore, the oxygen presence in the plasma provides more reactive species for removing C and Si while simultaneously consuming the polymer-forming fluorocarbon species [159, 162].

Plasma etching of SiC with SF₆ and O₂ typically uses metal masks to achieve a high selectivity; however, metal masks are known to create micromasking problem. Micromasking occurs when metal atoms of the mask material are sputtered by the plasma and redeposited in the etch field and act as local mask for the etch process. This results in grass-like structures on the etch surface. In addition, using a metal mask material typically requires a dedicated metal-contaminated tool or extensive cleaning between process changes as metal particles tend to be contaminants for many other processes including CMOS. To eliminate metals and to use widely accepted CMOS compatible masking materials such as SiO₂, and Si₃N₄, chlorine- and bromine-based chemistries have been investigated [163, 164]. Despite achieving reasonable selectivity for SiO₂, and Si₃N₄, chlorine- and bromine-based etching has significantly slower etch rates.

The selection of proper reactor type and operating conditions are also critical for realizing higher etch rate, etch selectivity, vertical sidewalls, and smooth surfaces. For example, conventional reactive ion etching (RIE) systems that use two parallel plates and a RF plasma generator have low plasma densities and high energy species. Therefore, etching of SiC in these type of reactors are dominated by physical sputtering, causing rough etch surfaces and low selectivity towards commonly used masking materials [159]. To overcome these shortcomings, most SiC etching is done using high-density, low-pressure plasma etchers, such as electron cyclotron resonance (ECR), transformer couple plasma (TCP), helicon plasma, and inductively coupled plasma (ICP) reactors [159, 164, 165, 166]. Among these, ICP is the most widely used technique. It offers many advantages over other methods including scalability and low operating cost. The capability of producing high plasma density at lower pressures is highly attractive because it reduces ion scattering, resulting in a significant reduction in lateral etch rate for high anisotropy [159, 166].

From the microsystem perspective, the required etch depth varies with the device type. For example, the etch depth is typically submicron for most SiC electronics applications, whereas it is often one to tens of microns for MEMS, and hundreds of microns for through-wafer holes for some high frequency SiC electronics [165]. To address these varying needs, different masking materials and process conditions have been developed. Photoresist, metal, SiO₂, Si_xN_y are the typical masking materials for selective etching of SiC. To date, the highest etch selectivity of 100:1 is reported for a Ni mask used with a SF₆ and O₂ gas chemistry in an ICP plasma etcher [167]. The reported etch rate is 1.5-1.6 $\mu\text{m}/\text{min}$. This would be an ideal pro-

cess for many SiC MEMS processes with regards to both etch rate and selectivity. The etch rate can be further increased up to $2.6 \mu\text{m}/\text{min}$ for bulk etching of SiC; however, the etch selectivity decreased to 45:1. The highest etch selectivity for a non-metal masking material, such as SiO_2 and Si_xN_y , is reported by Gao *et al.* using a HBr based gas chemistry in a TCP system [164]. The reported value for etch rate ratio for SiC: SiO_2 and SiC: Si_xN_y is up to 20:1 and 22:1, respectively. While the etch selectivity is reasonable, one of the drawbacks to this etch chemistry is the extremely low etch rate: $<150 \text{ nm}/\text{min}$. Although etch rate can be slightly increase with plasma conditions, the etch selectivity of non-metal mask become poor, leading to fast mask erosion. This results in undesired side-wall angles and rougher etch surfaces [164].

2.5.2 Wet Etching of SiC

Despite the fact that SiC is very difficult to be etched by wet chemical etching, many wet chemical etch processes have been investigated. Some attractive features of wet etching include selective etching of amorphous SiC over single crystalline SiC and dopant selective etching. In addition, wet etching does not require very expensive apparatus.

Wet etching processes for SiC fall into two general categories, namely chemical etching and electrochemical etching. Regardless of the category, the wet etching of SiC involves oxidation of the SiC surface and subsequent dissolution of the resulting oxides. Since the etch process occurs through surface oxidation, many parameters including surface defects, microstructure, dopant type, and seed polarity all can affect the etch characteristics. This section provides a brief overview of wet etching techniques used in SiC. An excellent review of SiC wet etching was conducted by Zhuang *et al.* [170].

Various etch chemistries ranging from highly basic to highly acidic have been investigated for chemical etching of SiC. Molten potassium hydroxide (KOH) etches SiC and the high etch rate is highly desirable for bulk-micromachining of substrates. However, the usefulness of this technique is limited by the lack of control over etching in the lateral direction. Furthermore, the high reactivity of molten KOH towards many other materials presents process compatibility issues. As a low temperature wet etch chemistry, a hydrofluoric (HF) and nitric acid (HNO_3) mixture has been shown to etch a-SiC and poly-SiC [171, 172]. The etch process can be done at room temperature, which is highly desirable. The inherent disadvantage to this method includes poor control over lateral dimensions. Similar to molten KOH, the etch solution is highly reactive to almost every standard masking, sacrificial, and isolation layer material (Si, SiO_2 , Si_xN_y , Al, Ti, Ni, Ta, Cr, Mo, W, and Cu) used in traditional microfabrication. Single-crystalline SiC and diamond are highly resistant to $\text{HF}+\text{HNO}_3$, so they can be used as etch masks. The etch resistance to single-crystalline SiC over amorphous SiC can be employed to pattern single-crystalline SiC by amorphization of selective regions. The amorphiza-

tion of single-crystalline SiC is typically done by ion implantation. Alok *et al.* has demonstrated a highly anisotropic etch by producing a trench with a depth of 0.3-0.8 μm on a 6H-SiC by ion implantation and $\text{HF}+\text{HNO}_3$ etching [171].

The electrochemical etch process of SiC occurs via oxidation reactions that forms volatile and dissolvable compounds. Diluted HF is commonly used as the electrolyte in which water serves as the oxidant and HF reacts with SiO_2 formed by the oxidation. The SiC surface act as the anode and generally Pt is used as the cathode. The widely accepted anodic reactions are shown in Eq. 2.7 and 2.8 [170]:



where h^+ represents holes.

According to the above reactions, the oxidation reaction is facilitated by hole generation. Ultraviolet (UV) illumination during the electrochemical etch process increases hole generation resulting in an increase in etch rate. This is known as photoelectrochemical etching (PEC) [170]. The feasibility of employing of PEC etching for SiC has been demonstrated by fabricating a pressure sensor using bulk micromachining of 6H-SiC [173]. Similar to other wet etching techniques, poor directionality control is a disadvantage. Furthermore, uneven etching is observed due to shadowing of UV light by evolving microstructures as the etch progresses. The prerequisite of having electrical contact to the regions being etched limits the usefulness of electrochemical etching and PEC for surface micromachining technology because some part of the microstructure can lose electrical contact as the etching process progresses.

2.5.3 Molding

The micromolding process for SiC was developed to obtain thicker 3D microstructures of SiC. This method was very attractive during the initial development phase of SiC MEMS because no viable DRIE process was available for SiC. The micromolding process resembles macro scale SiC molding using an investment cast technique. It starts with micromold fabrication, generally using silicon DRIE. The mold is subsequently filled by depositing SiC, typically using CVD, followed by chemical-mechanical polishing to remove excess material. Finally, the mold is removed by dissolving the mold materials to release the microstructure. The process steps are schematically depicted in Figure 2.36.

The first reported SiC microstructure created using the micromolding process was for the fabrication of SiC fuel atomizers for gas turbine engines [174]. In this case, a Si mold was fabricated using a Si DRIE process and SiC was deposited using APCVD. Excess SiC was removed by mechanical lapping before releasing the structure by dissolving the Si mold with heated KOH. Figure 2.37 shows the Si mold



Fig. 2.36 [174] (a) micromold, (b) SiC deposited micromold, (c) micromold with SiC after removing excess SiC, and (d) released SiC microstructure (©Elsevier 1999), reprinted with permission.

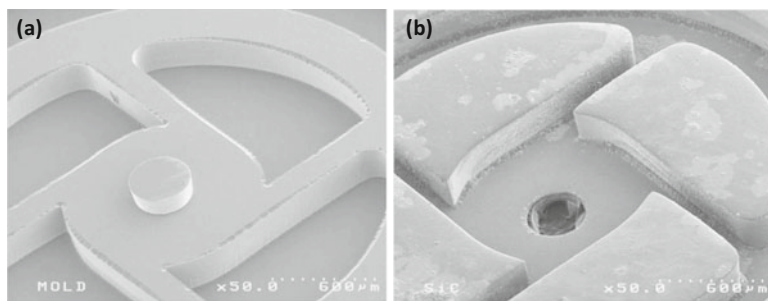


Fig. 2.37 [174] SEM image of (a) Si mold before deposition of SiC and (b) remolded SiC fuel atomizer using the Si mold (©Elsevier 1999), reprinted with permission.

and SiC fuel atomizer fabricated using the micromolding process. The performance of the micromolded SiC atomizer was compared with a Ni atomizer at similar conditions. Both atomizers performed equally well with the SiC device exhibiting a higher erosion resistance than the Ni atomizer. Some other examples of using micromolding for SiC microstructures include micromotors and micro-turbine engine parts [175, 176].

Today SiC DRIE is reasonably developed and can be successfully used to create a wide array of high aspect ratio SiC microstructures, yet there are areas of SiC microtechnology that still can benefit from the micromolding process. For instance, the maximum thickness of a bulk-micromachined SiC microstructure is predetermined by the wafer thickness. But in the molding process, thickness is determined by the mold. Furthermore, the ability to use well-established Si microfabrication techniques and no SiC etching requirement ease the fabrication constraints.

2.5.4 Other Patterning Methods for SiC

Direct writing methods such as focused ion beam (FIB) and laser micromachining have found applications in SiC microtechnology. Bhawe *et al.*, for example, reports the use of FIB for creating microstructures with 195 nm electrostatic gaps for electromechanical transduction in a poly-SiC Lamé-mode resonator [127]. In terms of achievable feature size and maskless patterning ability, FIB is very desirable as a prototyping tool to validate design concepts at a low cost. The major drawback to

this method is the serial nature of the process, which limits its usefulness for commercial SiC microsystem fabrication.

Laser micromachining is already widely used for cutting and drilling holes in many materials including SiC. Faster removal rate of laser micromachining is very attractive in comparison to FIB. One application is creating SiC vias of 10 to 20 μm in diameter using a femtosecond laser to bore through a 400 micron thick SiC substrate [177]. However, the holes seem to be significantly tapered and visible melting and resolidification can be observed. In theory, the use of nano- and pico-second pulse lasers will mitigate these problems, however, to date it has not yet been demonstrated for SiC patterning. Therefore, laser patterning is seen as still too immature of a process for SiC patterning to displace reactive ion etching for all but very specialized applications.

2.6 Planarization and Surface Preparation

Planarization and surface preparation of SiC are required at various stages of SiC microsystem fabrication. With regards to SiC electronics, defect-free, atomically-clean surfaces are a prerequisite for obtaining high-quality SiC epilayers because the surface defects in the substrate are replicated into the epilayer. Typically, a variety of sequential planarization and surface preparation steps are involved in SiC electronics fabrication. Although the criticality of defects and surface cleanliness for MEMS is below IC standards, planarization and surface preparation steps are helpful for MEMS fabrication as well. Planarization is needed for high fidelity pattern transfer when multi-step fabrication is used. Planarization is also a necessity for the previously discussed SiC molding process. From the perspective of integrated microsystem fabrication, planarization and surface preparation will play a critical role, regardless of whether the integration scheme involves MEMS first IC second, MEMS above IC, or MEMS next to IC (see chapter 6).

Steps for atomically-cleaned planar substrate surface preparation involve lapping and mechanical polishing followed by chemical mechanical polishing and etching. Each of these steps is briefly detailed below.

2.6.1 *Lapping and Mechanical Polishing*

Lapping and mechanical polishing is the first step performed on as-cut wafers from the SiC boule. This step is aimed at producing wafers with minimum bow, warp, and thickness variation. Diamond or boron carbide is used as polishing material because their hardness exceeds the hardness of SiC. The mechanism of material removal from SiC by finer grit, harder abrasives occurs through mechanical microfracture because of the higher hardness of the abrasive and inherent hardness of the work material (the material that is being polished) [178]. Polishing with harder abrasive is very

effective for producing wafers with minimum bow, warp, and thickness variation. It should be that polishing with hard abrasives inherently leaves scratches and residual subsurface damage that is detrimental to the subsequent SiC epitaxial process. By using abrasive slurries with decreasing grit size together with optimized rotation speed, pressure, temperature, and slurry feed, it is possible to improve the surface finish. Nonetheless, it is impossible to achieve scratch- and subsurface-defect-free results solely by using abrasive polishing [179].

2.6.2 Chemomechanical Polishing

Chemomechanical Polishing (CMP) is a two step process that starts with chemical surface modification and finishes with mechanical removal of the modified surface. Surface modification generally leads to formation of a softer passivation layer, which is subsequently removed by a softer abrasive material. As mechanical abrasion proceeds, the unreacted surface is exposed to the chemistry of the slurry and allows the chemical modification and abrasion process to repeat. As softer abrasive slurry only attacks the chemically modified surface, further scratching of hard work material, in this case SiC, is prevented.

A few different CMP processes have been reported for SiC. Generally, CMP occurs through formation of a SiO_2 passivation layer. The first CMP process, reported by Kikuchi *et al.*, uses Cr_2O_3 particles. The particles are responsible for both oxidizing the surface and mechanical abrasion [180]. A widely used SiC CMP process is based on a slurry of colloidal silica in high alkaline solution ($\text{pH} > 10$) at elevated temperatures ($\sim 55^\circ\text{C}$) [181, 179, 101]. Availability of polishing materials and similarity to silicon processes made this combination very attractive. A polishing rate of $0.1\text{--}0.2\ \mu\text{m h}^{-1}$ [181] and minimum roughness of $0.5\ \text{nm}$ [179] were reported for this process.

Electro-chemical-mechanical means have also been exploited for improving polishing characteristics of SiC with silica slurry. A small current ($1\text{--}20\text{mA}/\text{cm}^2$) passes through the substrate while H_2O_2 and KNO_3 are used as the electrolytes for anodic oxidation of the SiC surface. The reported best surface roughness using this method is $0.27\ \text{nm}$. Although passing current through the wafer adds another parameter for processing, this method is worth consideration when superior planarity is desired.

Although further improvements in SiC CMP are desired, the current stage of SiC CMP is mature enough for surface preparation of SiC electronics and MEMS. Many industrial SiC crystal and epilayer manufacturers routinely produce defect-free SiC surfaces using CMP for epilayer growth. The current CMP processes provide needed surface finish for high quality epitaxial growth [183, 184].

2.6.3 Surface Preparation

In-situ etching with gaseous precursors is the last step of the surface preparation (see Figure 2.14) for SiC epitaxial film growth. This etching step is highly critical for epitaxial layer growth as it further reduces defects in epilayer by reducing unwanted defect-induced nucleation sites [78]. A recent report by Horita *et al.* shows clear step-and-terrace structures after the etch process that were marginally visible after the CMP process [187]. However, it is important to note that etching neither reduces the surface roughness nor scratches since etching is mostly uniform throughout the surface [188]. Therefore, the initial surface quality coming from the CMP step is critically important. Many etch chemistries have been investigated and H_2 , HCl , or H_2+HCl are the most widely used etching sources, mainly due to superior etch characteristics as well as hydrogen is a common carrier gas for epilayer deposition [20, 187].

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