

# Preface

After more than 40 years of semiconductor technology advancement we have accepted the technical framework that has enabled us to bring the minimum feature size down to 45 nm, an incredible 1,000-fold reduction from the integrated circuits of the early 1970s. Going further, we may face limits in device downscaling due to the physical silicon crystalline structure. Therefore, besides the coordinated miniaturization (More Moore), according to Gordon Moore's prediction from 1965, the International Semiconductor Roadmap for Semiconductors (ITRS) now also considers applications of silicon technology that depend less on pushing down the minimum feature size (More than Moore).

However, the basic concept of silicon wafer manufacturing applies to both More Moore and More than Moore applications and essentially is not put into question. But, to a novice to silicon technology, several questions may come up that would not likely be raised by the expert: Why do we accept considerable material loss by cutting rectangular chips from a circular-shaped silicon wafer? Or, why do we work with very thick silicon wafer substrates if we only need the upper 1% layer to integrate the circuit components? In view of the possibility that economics may become a show stopper for semiconductor manufacturing even before the physical or technological limits are in sight, these are indeed good questions. And, such questions may stimulate ideas on new applications of silicon technology.

As silicon is not only the best suited semiconductor for complex circuit and system integration but also a material of excellent mechanical properties, ultra-thin chip technology and applications are to emerge as a new paradigm of silicon technology. Extremely thin and thus flexible silicon chips are expected to greatly enhance the emerging thin-film and organic semiconductor technologies by combining the well-known high performance of silicon chip technology with the large area and system-in-foil (SiF) applications. Moreover, very thin chips with through-silicon-via (TSV) interconnects will provide a means of overcoming the interconnect bottleneck of planar chip integration by allowing a migration to three-dimensional integrated circuits (3D IC). A small chip thickness also leads to a reduced thermal resistance and thus helps the management of the power density issue in modern high-performance silicon chips. Finally, there are

likely numerous new applications in microsystems that will emerge with the availability of ultra-thin chips.

However, ultra-thin chip technology features not only a new paradigm due to the thus emerging applications, but also because the fabrication of thin silicon chips will require certain adjustments and innovations in silicon process technology and circuit integration: Ultra-thin silicon chips need to have very high edge and surface qualities in order to retain the excellent inherent mechanical properties of silicon. Processing of thin wafers requires suitable handling techniques. Singulation of chips from thin wafers likely must be arranged by methods different from the conventional dicing process. The effect of stressors in increasing carrier mobility in the channel region of CMOS transistors will likely be different for extremely thin compared to thick silicon substrates. Also, ultra-thin chips will have physical properties that are different from those found on thick bulk substrates. Transistors on thin chips under variable bending stress will suffer from the piezoresistive effect shifting their operating point, which is thus an additional aspect to be considered in circuit design. The optical spectrum absorbed in a thin silicon film will be narrower compared to that absorbed on thick silicon. Also, the optical response of photo detectors on thin silicon might be affected by the properties of the back surface of the thin chip. The thermal boundary conditions of an integrated circuit on a thin silicon chip will to a large extent depend on the assembly of that chip into a rigid package or onto a foil substrate. Finally, for economic reasons, the techniques used to fabricate an ultra-thin chip will have to be optimized in terms of minimizing the density of defects to a tolerable level.

This book presents the general scope and the current status of the emerging ultra-thin chip technologies and applications. It was very fortunate that 75 leading international experts from academia, the semiconductor industry and equipment manufacturers could be brought together to contribute their expertise and vision to this new topic, and to do so in 34 chapters. Part I of the book provides an introduction, explaining the reasons why silicon technology has been based on thick wafers and chips for 40 years (Chap. 1) and why recently thin silicon chips became an issue considered by the ITRS (Chap. 2). Part II describes subtractive and additive thin chip fabrication based on bulk wafer thinning (Chaps. 3 through 5), wafer thinning that exploits etch stop techniques (Chaps. 6 and 7), and a new additive concept based on sintered porous silicon and epitaxial layer growth (Chap. 8). Part III relates to add-on process steps and modules that are applied to thin wafers in order to prepare them for specific applications, such as 3D IC and SiF (Chaps. 9 through 12). The assembly and embedding of ultra-thin chips is addressed in Part IV with SiF-specific chip embedding in foil (Chaps. 13 and 14) and general purpose chip-to-wafer alignment and micro-bump assembly (Chaps. 15 and 16). Part V is devoted to characterization and modelling of mechanical (Chaps. 17 and 18), electromechanical (Chaps. 19 and 20), thermal (Chap. 23) and optical (Chap. 24) properties. Also in this part, compact modelling of CMOS (Chap. 21) and bipolar (Chap. 22) are discussed, with a focus on flexible chips. Finally, in Part VI of the book, the possible improvements of known silicon applications and the emerging applications with thin chip technology are mentioned. Those include

power applications (Chap. 25), back-illuminated imagers (Chap. 26), thin solar cells (Chap. 27), biomedical applications (Chap. 28), sensor applications (Chap. 29), RF-ID tags (Chap. 30), security chips (Chap. 31), drive chips for flexible displays (Chap. 32), microwave and millimeter wave (Chap. 33) and specific 3D IC (Chap. 34) applications.

I hope that this book will serve as a useful resource to researchers and engineers in industry as well as to scientists in academia in their effort to turn the new paradigm of ultra-thin chip technology and application into major new applications of silicon technology and to overcome bottlenecks in conventional silicon technology development.

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