

Preface

This is a book on test and testability of digital circuits in which test is spoken in the language of design. In this book, the concepts of testing and testability are treated together with digital design practices and methodologies. We show how testing digital circuits designing testable circuits can take advantage of some of the well-established RT-level design and verification methodologies and tools. The book uses Verilog models and testbenches for implementing and explaining fault simulation and test generation algorithms. In the testability part, it describes various scan and BIST methods in Verilog and uses Verilog testbenches as virtual testers to examine and evaluate these testability methods. In designing testable circuits, we use Verilog testbenches to evaluate, and thus improve testability of a design.

The first part of the book develops Verilog test environments that can perform gate-level fault simulation and test generation. This part uses Verilog PLI along with Verilog's powerful testbench development facilities for modeling hardware and programing test environments. The second part of the book uses Verilog as a hardware design tool for describing DFT and BIST hardware. In this part, Verilog is used as a hardware description language describing synthesizable testable hardware. Throughout the book, Verilog simulation helps developing and evaluating test methods and testability hardware constructs.

This book professes a new approach to teaching test. Use of Verilog and Verilog PLI for test applications is what distinguishes this book from other test and testability books. As HDLs were used in late 1970s for teaching computer architectures, today, HDLs can be used to illustrate test methodologies and testability architectures that are otherwise illustrated informally by flow charts, graphs, and block diagrams. Verilog eliminates ambiguities in test algorithms and BIST and DFT hardware architectures, and it clearly describes the architecture of the testability hardware and its test sessions. Describing on-chip test hardware in Verilog helps evaluating the related algorithms in terms of hardware overhead and timing and thus feasibility of using them on SoC chips. Further support for this approach comes in use of testbenches. Using PLI in developing testbenches and virtual testers gives us a powerful programing tool interfaced with hardware described in Verilog. This mixed hardware/software environment facilitates the description of complex test programs and test strategies.



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Using HDL Models and Architectures

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