

Contents

1	Basic of Test and Role of HDLs	1
1.1	Design and Test	1
1.1.1	RTL Design Process	1
1.1.2	Postmanufacturing Test	4
1.2	Test Concerns	8
1.2.1	Test Methods	9
1.2.2	Testability Methods	11
1.2.3	Testing Methods	13
1.2.4	Cost of Test.....	13
1.3	HDLs in Digital System Test.....	15
1.3.1	Hardware Modeling.....	15
1.3.2	Developing Test Methods.....	15
1.3.3	Virtual Testers.....	16
1.3.4	Testability Hardware Evaluation	16
1.3.5	Protocol Aware ATE.....	16
1.4	ATE Architecture and Instrumentation.....	17
1.4.1	Digital Stimulus and Measure Instruments	17
1.4.2	DC Instrumentation	17
1.4.3	AC Instrumentation	17
1.4.4	RF Instrumentation.....	18
1.4.5	Ate	18
1.5	Summary	19
	References.....	20
2	Verilog HDL for Design and Test.....	21
2.1	Motivations of Using HDLs for Developing Test Methods	21
2.2	Using Verilog in Design	22
2.2.1	Using Verilog for Simulation	22
2.2.2	Using Verilog for Synthesis.....	23
2.3	Using Verilog in Test.....	24
2.3.1	Good Circuit Analysis.....	24
2.3.2	Fault List Compilation and Testability Analysis	24
2.3.3	Fault Simulation	25
2.3.4	Test Generation.....	26
2.3.5	Testability Hardware Design	26

2.4	Basic Structures of Verilog.....	27
2.4.1	Modules, Ports, Wires, and Variables.....	28
2.4.2	Levels of Abstraction	29
2.4.3	Logic Value System.....	29
2.5	Combinational Circuits	30
2.5.1	Transistor-Level Description	30
2.5.2	Gate-Level Description	31
2.5.3	Equation-Level Description.....	32
2.5.4	Procedural Level Description	32
2.5.5	Instantiating Other Modules.....	34
2.6	Sequential Circuits	36
2.6.1	Registers and Shift Registers.....	36
2.6.2	State Machine Coding	36
2.7	A Complete Example (Adding Machine).....	42
2.7.1	Control/Data Partitioning	42
2.7.2	Adding Machine Specification	42
2.7.3	CPU Implementation.....	43
2.8	Testbench Techniques.....	48
2.8.1	Testbench Techniques.....	48
2.8.2	A Simple Combinational Testbench.....	49
2.8.3	A Simple Sequential Testbench.....	50
2.8.4	Limiting Data Sets.....	51
2.8.5	Synchronized Data and Response Handling	51
2.8.6	Random Time Intervals	52
2.8.7	Text IO.....	53
2.8.8	Simulation Code Coverage.....	54
2.9	PLI Basics	56
2.9.1	Access Routines	57
2.9.2	Steps for HDL/PLI Implementation	57
2.9.3	Fault Injection in the HDL/PLI Environment	59
2.10	Summary	62
	References.....	62
3	Fault and Defect Modeling.....	63
3.1	Fault Modeling	63
3.1.1	Fault Abstraction	64
3.1.2	Functional Faults	67
3.1.3	Structural Faults	68
3.2	Structural Gate Level Faults	71
3.2.1	Recognizing Faults	71
3.2.2	Stuck-Open Faults	72
3.2.3	Stuck-at-0 Faults.....	72
3.2.4	Stuck-at-1 Faults.....	73
3.2.5	Bridging Faults	73
3.2.6	State-Dependent Faults.....	75
3.2.7	Multiple Faults	75
3.2.8	Single Stuck-at Structural Faults	77
3.2.9	Detecting Single Stuck-at Faults	83

3.3	Issues Related to Gate Level Faults.....	84
3.3.1	Detecting Bridging Faults	84
3.3.2	Undetectable Faults	85
3.3.3	Redundant Faults	85
3.4	Fault Collapsing	86
3.4.1	Indistinguishable Faults.....	86
3.4.2	Equivalent Single Stuck-at Faults.....	86
3.4.3	Gate-Oriented Fault Collapsing.....	87
3.4.4	Line-Oriented Fault Collapsing.....	89
3.4.5	Problem with Reconvergent Fanouts.....	91
3.4.6	Dominance Fault Collapsing	92
3.5	Fault Collapsing in Verilog.....	95
3.5.1	Verilog Testbench for Fault Collapsing.....	95
3.5.2	PLI Implementation of Fault Collapsing.....	97
3.6	Summary	100
	References.....	101
4	Fault Simulation Applications and Methods	103
4.1	Fault Simulation	103
4.1.1	Gate-Level Fault Simulation	103
4.1.2	Fault Simulation Requirements	104
4.1.3	An HDL Environment	105
4.1.4	Sequential Circuit Fault Simulation	111
4.1.5	Fault Dropping	111
4.1.6	Related Terminologies.....	111
4.2	Fault Simulation Applications.....	112
4.2.1	Fault Coverage.....	113
4.2.2	Fault Simulation in Test Generation.....	114
4.2.3	Fault Dictionary Creation	117
4.3	Fault Simulation Technologies	122
4.3.1	Serial Fault Simulation	124
4.3.2	Parallel Fault Simulation	127
4.3.3	Concurrent Fault Simulation	131
4.3.4	Deductive Fault Simulation	133
4.3.5	Comparison of Deductive Fault Simulation	137
4.3.6	Critical Path Tracing Fault Simulation	137
4.3.7	Differential Fault Simulation.....	140
4.4	Summary	141
	References.....	141
5	Test Pattern Generation Methods and Algorithms.....	143
5.1	Test Generation Basics	143
5.1.1	Boolean Difference.....	143
5.1.2	Test Generation Process	145
5.1.3	Fault and Tests.....	146
5.1.4	Terminologies and Definitions	147
5.2	Controllability and Observability.....	147
5.2.1	Controllability	148
5.2.2	Observability	148

5.2.3	Probability-Based Controllability and Observability	148
5.2.4	SCOAP Controllability and Observability	155
5.2.5	Distances Based.....	160
5.3	Random Test Generation	160
5.3.1	Limiting Number of Random Tests.....	160
5.3.2	Combinational Circuit RTG	163
5.3.3	Sequential Circuit RTG	171
5.4	Summary	174
	References.....	174
6	Deterministic Test Generation Algorithms.....	175
6.1	Deterministic Test Generation Methods.....	175
6.1.1	Two-Phase Test Generation.....	176
6.1.2	Fault-Oriented TG Basics.....	177
6.1.3	The D-Algorithm.....	182
6.1.4	PODEM (Path-Oriented Test Generation).....	191
6.1.5	Other Deterministic Fault-Oriented TG Methods	196
6.1.6	Fault-Independent Test Generation	197
6.2	Sequential Circuit Test Generation.....	198
6.3	Test Data Compaction	200
6.3.1	Forms of Test Compaction	201
6.3.2	Test Compatibility	201
6.3.3	Static Compaction	204
6.3.4	Dynamic Compaction.....	209
6.4	Summary	211
	References.....	211
7	Design for Test by Means of Scan	213
7.1	Making Circuits Testable.....	213
7.1.1	Tradeoffs.....	213
7.1.2	Testing Sequential Circuits.....	214
7.1.3	Testability of Combinational Circuits	215
7.2	Testability Insertion.....	215
7.2.1	Improving Observability	216
7.2.2	Improving Controllability.....	217
7.2.3	Sharing Observability Pins	218
7.2.4	Sharing Control Pins	219
7.2.5	Reducing Select Inputs.....	221
7.2.6	Simultaneous Control and Observation.....	222
7.3	Full Scan DFT Technique.....	225
7.3.1	Full Scan Insertion	226
7.3.2	Flip-Flop Structures.....	227
7.3.3	Full Scan Design and Test	234
7.4	Scan Architectures.....	244
7.4.1	Full Scan Design	245
7.4.2	Shadow Register DFT	245
7.4.3	Partial Scan Methods.....	248
7.4.4	Multiple Scan Design	251
7.4.5	Other Scan Designs	253

7.5	RT Level Scan Design	253
7.5.1	RTL Design Full Scan	253
7.5.2	RTL Design Multiple Scan	254
7.5.3	Scan Designs for RTL	258
7.6	Summary	258
	References	259
8	Standard IEEE Test Access Methods	261
8.1	Boundary Scan Basics	261
8.2	Boundary Scan Architecture	262
8.2.1	Test Access Port	262
8.2.2	Boundary Scan Registers	263
8.2.3	TAP Controller	267
8.2.4	The Decoder Unit	271
8.2.5	Select and Other Units	271
8.3	Boundary Scan Test Instructions	271
8.3.1	Mandatory Instructions	272
8.4	Board Level Scan Chain Structure	277
8.4.1	One Serial Scan Chain	278
8.4.2	Multiple-Scan Chain with One Control Test Port	278
8.4.3	Multiple-Scan Chains with One TDI, TDO but Multiple TMS	279
8.4.4	Multiple-Scan Chain, Multiple Access Port	279
8.5	RT Level Boundary Scan	281
8.5.1	Inserting Boundary Scan Test Hardware for CUT	281
8.5.2	Two Module Test Case	283
8.5.3	Virtual Boundary Scan Tester	285
8.6	Boundary Scan Description Language	290
8.7	Summary	292
	References	294
9	Logic Built-in Self-test	295
9.1	BIST Basics	295
9.1.1	Memory-based BIST	295
9.1.2	BIST Effectiveness	297
9.1.3	BIST Types	297
9.1.4	Designing a BIST	298
9.2	Test Pattern Generation	300
9.2.1	Engaging TPGs	300
9.2.2	Exhaustive Counters	300
9.2.3	Ring Counters	301
9.2.4	Twisted Ring Counter	302
9.2.5	Linear Feedback Shift Register	303
9.3	Output Response Analysis	312
9.3.1	Engaging ORAs	312
9.3.2	One's Counter	312
9.3.3	Transition Counter	314
9.3.4	Parity Checking	316
9.3.5	Serial LFSRs (SISR)	316
9.3.6	Parallel Signature Analysis	317

9.4	BIST Architectures	319
9.4.1	BIST-related Terminologies	319
9.4.2	A Centralized and Separate Board-level BIST Architecture (CSBL)	320
9.4.3	Built-in Evaluation and Self-test (BEST).....	321
9.4.4	Random Test Socket (RTS)	322
9.4.5	LSSD On-chip Self Test	324
9.4.6	Self-testing Using MISR and SRSG	325
9.4.7	Concurrent BIST	326
9.4.8	BILBO	328
9.4.9	Enhancing Coverage.....	329
9.5	RT Level BIST Design.....	329
9.5.1	CUT Design, Simulation, and Synthesis.....	330
9.5.2	RTS BIST Insertion	330
9.5.3	Configuring the RTS BIST	326
9.5.4	Incorporating Configurations in BIST.....	338
9.5.5	Design of STUMPS.....	340
9.5.6	RTS and STUMPS Results.....	343
9.6	Summary.....	343
	References.....	343
10	Test Compression	345
10.1	Test Data Compression	348
10.2	Compression Methods	347
10.2.1	Code-based Schemes.....	347
10.2.2	Scan-based Schemes.....	357
10.3	Decompression Methods	362
10.3.1	Decompression Unit Architecture	363
10.3.2	Cyclical Scan Chain	365
10.3.3	Code-based Decompression	366
10.3.4	Scan-based Decompression.....	372
10.4	Summary.....	372
	References.....	372
11	Memory Testing by Means of Memory BIST	375
11.1	Memory Testing	375
11.2	Memory Structure	376
11.3	Memory Fault Model	377
11.3.1	Stuck-At Faults.....	377
11.3.2	Transition Faults	378
11.3.3	Coupling Faults	378
11.3.4	Bridging and State CFs	378
11.4	Functional Test Procedures.....	378
11.4.1	March Test Algorithms.....	378
11.4.2	March C- Algorithm.....	379
11.4.3	MATS+ Algorithm	380
11.4.4	Other March Tests	380

11.5	MBIST Methods	381
11.5.1	Simple March MBIST	381
11.5.2	March C- MBIST	385
11.5.3	Disturb MBIST	387
11.6	Summary	391
	References	391
Appendix A	Using HDLs for Protocol Aware ATE	393
Appendix B	Gate Components for PLI Test Applications	397
Appendix C	Programming Language Interface Test Utilities	399
Appendix D	IEEE Std. 1149.1 Boundary Scan Verilog Description	403
Appendix E	Boundary Scan IEEE 1149.1 Virtual Tester	411
Appendix F	Generating Netlist by Register Transfer Level Synthesis (<i>NetlistGen</i>)	423
Index		427



<http://www.springer.com/978-1-4419-7547-8>

Digital System Test and Testable Design
Using HDL Models and Architectures

Navabi, Z.

2011, XVII, 435 p., Hardcover

ISBN: 978-1-4419-7547-8