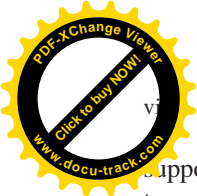


Preface

When I started this book, I thought I understood the world of on-chip debug—after all, I had been part of one of the leading startups in the area for 5 years and had been a participant in a number of standard and industry organizations that were leading the world of on-chip debug and instrumentation into the next wave. As I gathered my materials, I grew more impressed by the day and by the month at the body of work that this topic has accumulated, in industry and in academia, in every nook and cranny of the embedded systems business, from embedded processor, to bus architecture, to FPGA, to IP development; engineers have developed and customized a truly impressive range of on-chip debug and instrumentation solutions to address and support their products and to enable an increasingly capable infrastructure that does much more than the prosaic word debug implies and starts to address the full potential of what on-chip instrumentation can truly provide for the electronics industry.

This book came about, in part, because of the lack of a comprehensive discussion of on-chip debug instrumentation. This seems to have been an area where the experts come about from on-the-job experience and in ad hoc methods. On-chip debug is an integral part of most modern processor and system on-chip (SoC) design, but in my experience it is not a topic given in-depth discussion in engineering school (universities take note). Most engineers' experience of on-chip debug is limited to plugging into the JTAG port and running the software, with little understanding of what goes on within. This text tries to provide a general overview of the different types of on-chip debug that goes into a design.

This book is structured into three main sections; the first, Chaps. 1–7, is an introduction to the variety of concepts that make up on-chip debug, in particular looking at some of the history and well-established infrastructure, including an overview of JTAG from a debug, rather than test, point of view. It also looks at aspects of processor- and bus-level instrumentation and discusses multicore on-chip debug issues. The second section, Chaps. 8–11, addresses a number of the standards and industry efforts that are ongoing in areas ranging from instrument interfaces to JTAG advances, some of which, like Nexus and OCP-IP, I have been involved in, and others that have been a learning experience for me over the last year, all of which I believe will form the core basis for the next generation of on-chip debug. The third section, Chaps. 12–15, is a survey of some of the wide variety of commercially



supported solutions for on-chip debug, addressing a limited cross section of the types of on-chip instruments that are available for different processors and SoCs.

Some areas related to on-chip debug have been intentionally kept generic and out of the discussion to maintain the focus on the on-chip instrumentation. Notably, I have kept any detailed discussion of probes and host-based debugger software to a minimum, other than what is required to make the concepts of JTAG and trace understandable. This may seem unusual, but the reasons for this are two-fold. First, the topic of debug probe and software design is at least a book in itself. Second, the commercial business involved in probes and debug software is a significant business unit for most processor companies as well as the dozens of companies that provide probe and software solutions (many run by people I know) that address the range of debug options. To mention any one example in any detail would ignore the rest that are equally deserving of mention.

Few are of variety of instrumentation- and debug-related areas I cover are discussed exhaustively. This is due to both limitations on space and a large amount of supplemental detailed information available elsewhere for those who want to explore in more depth. Similarly, I have intentionally avoided discussion of some of the more advanced implementations, in order to keep the text accessible to a more general reader. For virtually all topics, I highly recommend the reader to directly contact the IP or chip vendor or standards group for more detailed and updated information on the topics. Those interested in instrumentation products can find an amount of online resources that address specific instrumentation solutions in minute detail. The amount of documentation available on MIPS EJTAG or ARM ETM, for example, can put page length of *War and Peace* to shame.

The standards-related activities are somewhat less well documented, in some cases because they are work in progress. However, there is a lot of follow-on information out there for those who search. So I have tried to focus on what I think are the interesting or unique parts of different instrumentation solutions, with the assumption that readers interested in more detail can find it.

I want to acknowledge a number of people in the industry who have helped me along the way, especially Rick Leatherman and the on-chip instrumentation team of the First Silicon Solutions group at MIPS, who got me started in thinking about on-chip instrumentation and who taught me far more they realize about on-chip debug technologies and the businesses involved. I also thank the current and past members of the Nexus IEEE 5000 Forum and members of the OCP-IP Debug Working Group, with special recognition to Bob Uvacek, my longtime compatriot in the working group.

Last, but by far not least, I want to acknowledge my family, without whom I am nothing. My wife Marcy, my daughters Courtney and Naomi, my son Eric, and my mom Rita Bickel Stollon (of blessed memory) were patient and understanding of the time I spent working on this book. Finally, I dedicate this book to my family but especially to my father Arthur Stollon (of blessed memory), who proofread everything I wrote while I was in school and taught me “be prepared to trudge thru the wilderness to get a change at the limelight”.

Dallas, TX

Neal Stollon



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