FinFET Circuit Design

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Abstract Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS at the nanoscale. FinFETs are double-gate devices. The two gates of a FinFET can either be shorted for higher perfomance or independently controlled for lower leakage or reduced transistor count. This gives rise to a rich design space. This chapter provides an introduction to various interesting FinFET logic design styles, novel circuit designs, and layout considerations.

Keywords Circuit design · FinFETs · Layout · Leakage power · Power optimization

1 Introduction

As nanometer process technologies have advanced, chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern. Even for nonportable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (very-large-scale integration) designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increased importance. This chapter explores how circuits based on FinFETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (complementary metal-oxide-semiconductor) at 22-nm and beyond, offer interesting delay–power tradeoffs.

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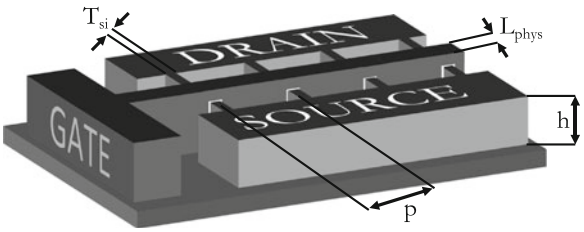


Fig. 1 Multi-fin FinFET [17]

The steady miniaturization of metal-oxide-semiconductor field-effect transistors (MOSFETs) with each new generation of CMOS technology has provided us with improved circuit performance and cost per function over several decades. However, continued transistor scaling will not be straightforward in the sub-22 nm regime because of fundamental material and process technology limits [1]. The main challenges in this regime are twofold: (a) minimization of leakage current (subthrehsold + gate leakage), and (b) reduction in the device-to-device variability to increase yield [2]. FinFETs have been proposed as a promising alternative for addressing the challenges posed by continued scaling. Fabrication of FinFETs is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing.

Figure 1 shows the structure of a multi-fin FinFET. The FinFET device consists of a thin silicon body, the thickness of which is denoted by T_{Si}, wrapped by gate electrodes. The current flows parallel to the wafer plane, whereas the channel is formed perpendicular to the plane of the wafer. Due to this reason, the device is termed *quasi-planar*. The independent control of the front and back gates of the FinFET is achieved by etching away the gate electrode at the top of the channel. The effective gate width of a FinFET is $2nh$, where n is the number of fins and h is the fin height. Thus, wider transistors with higher on-currents are obtained by using multiple fins. The fin pitch (p) is the minimum pitch between adjacent fins allowed by lithography at a particular technology node. Using spacer lithography, p can be made as small as half of the lithography pitch [3].

1.1 Shorted-Gate and Independent-Gate FinFETs

FinFET devices come in many flavors. In shorted-gate (SG) FinFETs, the two gates are connected together, leading to a three-terminal device. This can serve as a direct replacement for the conventional bulk-CMOS devices. In independent-gate (IG) FinFETs, the top part of the gate is etched out, giving way to two independent gates. Because the two independent gates can be controlled separately, IG-mode FinFETs offer more design options (Fig. 2).

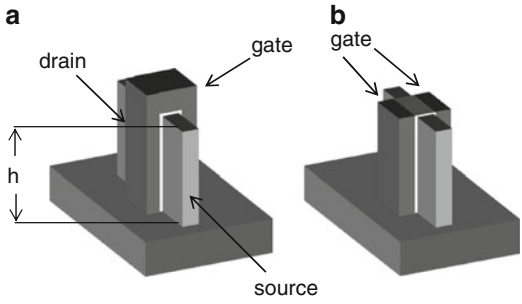


Fig. 2 (**a**) SG-mode FinFET; (**b**) IG-mode FinFET

2 Logic Design Using SG/IG-Mode FinFETs

The performance and power characteristics of FinFET logic gates using transistors in various connected configurations are explored next. Some guidelines for "back of the envelope" logic design using FinFETs are also presented. In general, three modes of FinFET logic gates are logically obvious: (1) SG-mode, in which FinFET gates are tied together; (2) low-power (LP)-mode, in which the back-gate bias is tied to a reverse-bias voltage to reduce subthreshold leakage [4]; and (3) IG-mode, in which independent signals drive the two device gates. Figure 3 shows the implementation of a two-input NAND gate in each of the above modes. A hybrid IG/LP-mode NAND gate, which employs a combination of LP and IG modes is also presented. Similarly, other Boolean functions can be implemented in CMOS styles in each of the above-mentioned modes. (V_{hi} and V_{low} are the corresponding reverse-bias voltages.)

Before proceeding with a discussion of FinFET NAND gates, let us consider some characteristics of the FinFET device that have a bearing on digital design. SPICE-simulated DC transfer characteristics, that is, I_{ds} vs. V_{gfs}, for a 32-nm *n*-type FinFET are shown in Fig. 4. Here V_{gfs} denotes the potential difference between the front gate (gf) and source terminals. The transistor's source terminal was tied to ground for these simulations and the drain was tied to the power supply. Transfer characteristics are presented for various back-gate voltages (V_{gbs}). The University of Florida double-gate (UFDG) SPICE model [5] was used for 32-nm FinFET simulations. The power supply was fixed at 1 V. Curves corresponding to SG, LP, and IG modes of operation are indicated. Similar results can be obtained for *p*-type FinFET.

The operating temperature was fixed at 70°C for all simulations. FinFET structures suffer from considerable self-heating. Their thermal simulations are shown to yield a temperature close to 70°C [6] if the switching activity is assumed to be 0.1.

The variation in on- and off-state FinFET currents, I_{on} and I_{off}, across the three modes of FinFET operations is notable. FinFETs offer the best drive strength in SG-mode. I_{on} reduces by about 60% in the IG and LP modes. Application of a

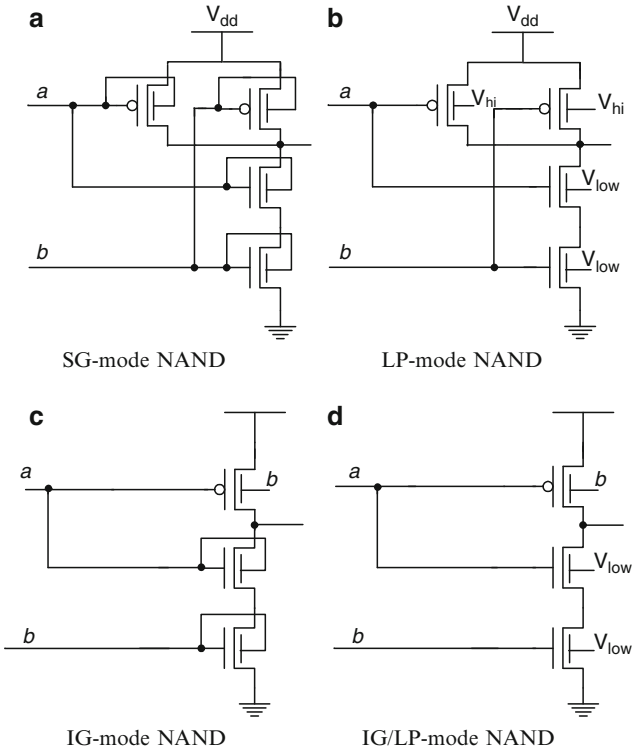


Fig. 3 Different FinFET-based NAND gate designs [4]

reverse bias on the back gate in the LP-mode leads to a further reduction in I_{on}, albeit at a smaller rate. However, a FinFET with one gate fed by logic 0, as in the pull-up *p*-type FinFET of an IG-mode NAND gate, is not a significantly better driver than a FinFET with a reverse-biased back-gate. On the other hand, I_{off} decreases much more rapidly with increasing reverse bias. A strong reverse-bias reduces I_{off} by more than an order of magnitude compared to the SG-mode, which displays the highest I_{off}.

It is useful to consider the implications of the above device characteristics on the design of an LP-mode FinFET inverter. Figure 5 plots the variation in average delay and leakage power against change in the back-gate bias voltage for a minimum-sized LP-mode inverter, driving a load four times its size and driven by a slope of 5 ps.

Both pull-up and pull-down were driven by a back-gate bias of equal strength in this experiment. For instance, if the strength of the back-gate bias was 0.2 V, a voltage of -0.2 V was used for the back-gate bias of the pull-down FinFET and a voltage of 1.20 V was used to bias the pull-up FinFET. The figure also depicts delay and leakage for an SG-mode inverter. It can be seen that inverter delay degrades sharply in going from the SG-mode to zero reverse-bias LP-mode, and more slowly with increasing reverse bias. The leakage current, however, strongly varies with

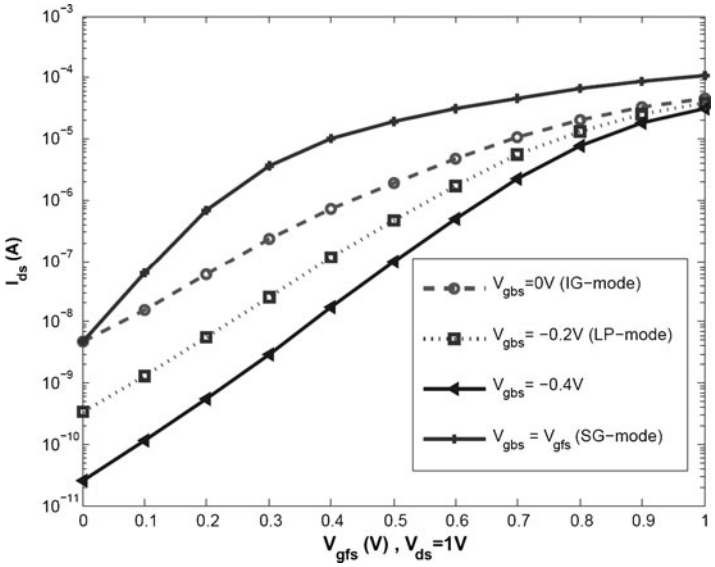


Fig. 4 Simulated I_{ds} vs. V_{gfs} characteristics for a 32-nm *n*-type FinFET

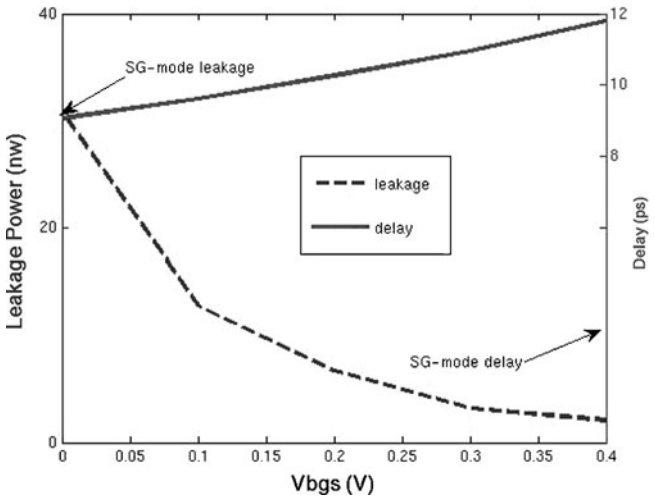


Fig. 5 LP-mode FinFET inverter delay and leakage power variation

back-gate bias. The leakage curve shows an initial sharp decline, but flattens out at back-gate bias voltages exceeding 0.26 V. Further increase in the bias can only lead to delay overheads without much corresponding savings in leakage. With this in mind, a suitable value for the back-gate bias for *n*-type FinFETs can be set to −0.26 V. For *p*-type FinFETs, the back-gate voltage was adjusted to 1.18 V to equalize rise and fall delays.

2.1 Design of Logic Gates

Let us revisit the NAND gate designs shown in Fig. 3. Let us consider transistor sizing for each gate. All logic gates are designed to have the minimum possible size that the available FinFET models allowed. All FinFETs in the pull-up and pull-down blocks, respectively, were sized equally. Let the ratio of the widths of a pull-up (W_p) and a pull-down FinFET (W_n) be denoted as β. To obtain β, we use the following considerations:

1. Electron mobility exceeds hole mobility by 2×.
2. The electrical width of a FinFET is quantized based on the number of fins in it. It is assumed that wider transistors can only be obtained by increasing the number of fins. The height of each fin is assumed to be fixed.
3. As we observed earlier, using a FinFET in the LP or IG modes reduces its drive strength by almost 60%.

Values for β, and estimates for input capacitance, average off-state current consumption under different input vectors, and delay (average of rise and fall delays) for each gate are shown in Table 1. Assuming a ratio of 2:1 between the electron and hole mobility, a matched CMOS NAND gate may be designed with $\beta = 1$. The SG-mode NAND gate can be obtained by directly translating the CMOS NAND design to FinFETs, while retaining the same sizing. Table 1 reports delay measurements obtained using HSPICE, under three load conditions: unloaded and with loads of 4 (FO4) and 20 (FO20) minimum-sized SG-mode FinFET inverters, respectively, for each design mode. An input slope of 5 ps was used to drive the gates.

In the LP-mode gate, the drive strength of every FinFET is reduced equally. Thus, we can continue to use $\beta = 1$. As expected, the average delay of the LP-mode gate is almost twice that of the SG-mode gate. On the other hand, the input capacitance of an LP-mode gate is only half that of an SG-mode gate, because only one FinFET gate is driven by the input signal. More significantly, leakage power, averaged over all input combinations, is reduced by over 90% because of threshold voltage control.

The IG-mode gate was designed to have asymmetric rise and fall delays. Only one transistor gate is used for pull-up in the IG-mode NAND gate. To achieve balanced rise and fall delays, the pull-up would need to be scaled up. However, using equally sized pull-up and pull-down, i.e., $\beta = 1$, yields savings in area, input capacitance, and

Table 1 Comparison of delay and leakage current for SG-, LP-, IG-, and IG/LP-mode NAND gates

Design mode	β	C_{in} (aF)	I_{off} (nA)	Unloaded delay (ps)	FO4 delay (ps)	FO20 delay (ps)
SG	1	340	4.44	1.31	5.05	13.94
LP	1	170	0.22	5.64	19.95	61.84
IG	1	255	3.41	2.89	10.21	20.12
IG/LP	1	170	0.42	3.44	28.82	60.32

diffusion capacitance at the gate output. As a result, under unloaded conditions, the IG-mode NAND gate has an average delay comparable to, or even better than, the SG-mode NAND gate, but consumes less area and power. Unfortunately, the asymmetry in the pull-up and pull-down drive strengths of an IG-mode gate can lead to large disparities in the rise and fall delays under conditions of greater load. If both transitions through a gate are critical, an IG-mode gate may not be suitable.

As an alternative, consider the IG/LP-mode design. In the fashion of an IG-mode gate, in the IG/LP-mode, parallel transistors, that is, the pull-up for a NAND and pull-down for a NOR gate, are merged. However, unlike the IG-mode design, delays are balanced by reducing the strength of the complementary series structure. This can be seen by comparing the IG- and IG/LP-mode NAND gate results in Table 1.

Strength reduction is achieved by tying the back gates of FinFETs in series to a strong reverse bias. Essentially, the faster transition is slowed down to match the transition made slow by merging transistors, in exchange for significant savings in leakage. At first sight, this might seem to be a large loss in performance. However, often an IG/LP-mode gate has better worst-case rise and fall delays than its IG-mode counterpart. For instance, IG/LP-mode NAND gates actually have a worst-case (rise) delay that is smaller than or comparable to their IG-mode counterparts, under all load conditions, because of reduced competition from the pull-down network during a rising transition at the output. The same observation applies to the falling transition for corresponding NOR gates. This might make IG/LP gates more useful in situations where both rising and falling transitions through a gate are critical.

Also, the IG/LP-mode NAND gate shows savings in excess of 56% and 33% in leakage, averaged across input vectors, and switched capacitance, respectively, compared to the IG-mode design, while retaining the same transistor area. In the interest of brevity, this section presented data only for two-input NAND gates. However, the design techniques examined are generally applicable. NOR and AND-OR-INVERT (AOI) gates can be designed using the same principles and similar trade-offs will be observed for power and delay. Including varied implementations of each logic gate, as proposed in this section, in a cell library provides a level of flexibility that might be used to obtain useful tradeoffs in the power-delay design space.

The circuits could be synthesized using a combination of logic gates from the FinFET cell library and, thereafter, the power–delay spectrum can be generated through various power optimization tools under relaxed/severe delay constraints [4].

3 Threshold Voltage Control Through Multiple Supply Voltages for Power-Efficient FinFET Interconnects

In modern circuits, interconnect efficiency is a central determinant of circuit efficiency. Moreover, as the technology is scaled down, the importance of efficient interconnect design is increasing. FinFET interconnect design can provide several new promising interconnect synthesis schemes.

A mechanism for improving FinFET efficiency, called *threshold voltage control through multiple supply voltages* (TCMS) is described here. The scheme is significantly different from conventional supply voltage schemes. A circuit design for a FinFET buffer using TCMS is developed. It is shown in [7] that on average TCMS can provide power savings of 50.4% and device area savings of 9.2% as compared to the state-of-art dual-V_{dd} interconnect synthesis schemes.

It has been demonstrated that digital logic circuits using FinFETs can be significantly more power-efficient than their counterparts implemented in bulk CMOS at the same gate length. Thus, directly translating bulk CMOS interconnects to FinFETs may also be expected to provide corresponding power savings. However, beyond the obvious technology-driven efficiency benefits, circuits can take advantage of FinFET's double-gate structure to further optimize power and performance.

An important FinFET characteristic is threshold voltage (V_{th}) controllability. The V_{th} at each gate of a FinFET can be controlled through the application of a voltage at the other gate. Because the V_{th} governs both transistor power consumption and delay, V_{th} controllability is a powerful tool for circuit optimization. We describe an innovative synthesis style for interconnect circuits with multiple supply voltages, which takes advantage of V_{th} controllability in connected-gate FinFETs. Traditionally, in multiple supply voltage circuits, power is saved through the use of a lower supply voltage on off-critical paths. For instance, a conventional dual supply voltage (V_{dd}) circuit may use the nominal high-performance V_{dd} for the technology process at hand and, on off-critical paths, a lower V_{dd}, which is typically 60–70% in magnitude compared to the higher V_{dd}.

In a significant departure from convention, a new multiple-V_{dd} scheme, called TCMS, which does not employ a lower V_{dd}, is described. Three supply voltages are used in TCMS: a nominal supply voltage (V_{dd}^{L}), a slightly higher supply voltage (V_{dd}^{H}), and a slightly negative supply voltage (V_{ss}^{H}). The design is based on the principle that in an overdriven FinFET inverter (an inverter that is driven by an input voltage that is higher than its V_{dd}), both leakage and output-current drive (and, thereby, delay) can be controlled simultaneously.

Subthreshold leakage is reduced because of an increase in the V_{th} of the leaking transistor, while current drive is increased because of the larger gate drive experienced by the active transistor. This allows both subthreshold leakage and device width, and, thereby, dynamic power consumption, to be reduced. TCMS is also a voltage-level shifter-free style of circuit design, that is, inverters tied to high and low V_{dd} are allowed to freely alternate, without the need for dedicated level shifters. Instead, level-shifting is built into inverters that require it, through the use of higher-V_{th} FinFETs. FinFETs with higher V_{th} are used at the input of buffers that are connected to V_{dd}^{H}, but driven by buffers operating at V_{dd}^{L} in order to eliminate static leakage current. This allows frequent use of overdriven buffers in TCMS interconnects, thereby increasing the attendant power savings obtainable through the use of overdriven inverters.

3.1 The Principle of TCMS

The V_{th} at each FinFET gate cannot only be controlled statically through the control of process parameters, such as channel-dopant concentration or the value of the gate work function, but also dynamically through the application of a voltage to the other gate (gate–gate coupling). A generalized model for the relationship between the threshold voltage ($V_{\text{th}_{\text{gf}}}$) at the front gate (gf) of a FinFET and the voltage applied to its back gate (gb) is derived in [8]. However, the following approximate relationship suffices.

$$V_{\text{th}_{\text{gf}}} \approx \begin{cases} V^0_{\text{th}_{\text{gf}}} - \delta(V_{\text{gbs}} - V_{\text{th}_{\text{gb}}}) & \textit{if } V_{\text{gbs}} < V_{\text{th}_{\text{gb}}}, \\ V^0_{\text{th}_{\text{gf}}} & \textit{otherwise}, \end{cases}$$

where s denotes the source terminal of the FinFET, δ is a positive value determined by the ratio of gate and body capacitances, and $V^0_{\text{th}_{\text{gf}}}$ is the minimum observed $V_{\text{th}_{\text{gf}}}$. The above equation is given for an n-type FinFET, but may also be used for a p-type FinFET with the usual changes in sign. If the FinFET is operated with both its gates tied together, the threshold voltages of both gates respond simultaneously to change in voltage at the other gate. As the above equation predicts, gate–gate coupling is observed only in the weak inversion region of operation. In the region of strong inversion, the presence of inversion charge in the channel shields FinFET gates from each other and no coupling is observed.

As mentioned earlier, TCMS is based on the observation that in an overdriven inverter, both subthreshold leakage and current drive can be controlled simultaneously. We illustrate this concept using Fig. 6, where inverter (a) is a so-called high-V_{dd} inverter, that is, it is connected to V^{H}_{dd} and V^{H}_{ss}. Inverter (b) is a low-V_{dd} inverter, that is, it is connected to V^{L}_{dd} and V^{L}_{ss}. The values of V^{H}_{dd}, V^{H}_{ss}, and V^{L}_{dd} are

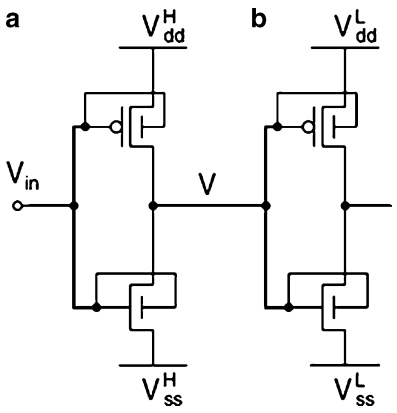


Fig. 6 Principle of TCMS [7]

1.08, −0.1 and 1.0 V, respectively. V_{ss}^{L} is assumed to be tied to a ground. Inverter (b) is, thus, overdriven.

From this point on, it is assumed that any inverter connected to V_{dd}^{H} is also connected to V_{ss}^{H} and similarly for the lower supply voltages. To illustrate the principle of TCMS, let V_{in} in Fig. 6 be held at the logic 0 voltage and, thus, $V = V_{dd}^{H}$. Then, subthreshold leakage through inverter (b) is determined by the leakage through the *p*-type FinFET, while the inverter's delay is determined, to a large extent, by the current through the *n*-type FinFET.

According to the above equation, the V_{th} of the *p*-type FinFET is increased due to the reverse-biased voltage of 0.08 V observed at its gates, thereby reducing subthreshold leakage. The V_{th} of the *n*-type FinFET, which is operating in the strong-inversion region, is not appreciably altered. Nevertheless, it experiences a forward-biased voltage of 1.08 V, which is higher than the normal gate drive of 1.0 V at the inverter input. This leads to a somewhat higher drive current. Similarly, the application of a logic 1 voltage at the circuit input leads to a reduction in the leakage of the *n*-type FinFET and improvement in the drive strength of the *p*-type FinFET.

SPICE-simulated DC transfer characteristics for an overdriven *n*-type FinFET is shown in Fig. 7. A PTM for 32 nm FinFETs, available from [9, 10], was used for this simulation. In the simulation, the drain terminal of the *n*-type FinFET was tied to V_{dd}^{L}, and the source terminal was tied to ground. The voltage at the gate terminals was swept from V_{ss}^{H} to V_{dd}^{H}. On-currents through the FinFET at normal drive ($V_{gs} = V_{dd}^{L}$) and overdrive ($V_{gs} = V_{dd}^{H}$) are indicated by I_{on}^{L} and I_{on}^{H} in the figure, respectively. Though it may not be evident on the logarithmic scale of Fig. 7, the value of I_{on}^{H} exceeds the value of I_{on}^{L} by about 3.4%. The relationship between the corresponding values of off-current I_{off}^{H} and I_{off}^{L}, respectively, is evident in Fig. 7. I_{off}^{H} is over 6× smaller in value than I_{off}^{L}.

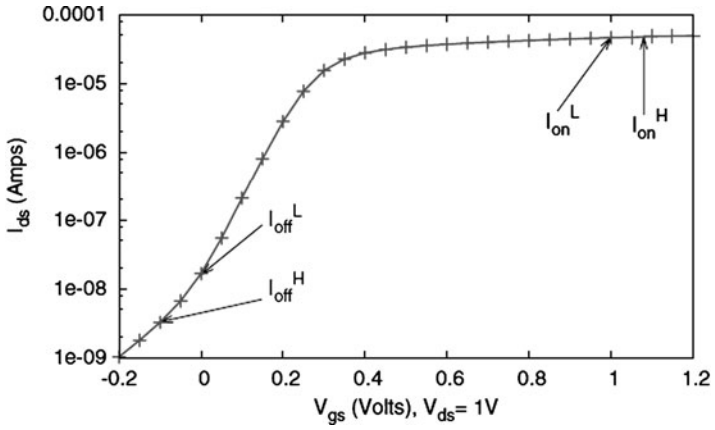


Fig. 7 Simulated $I_{ds}-V_{gs}$ characteristics for an overdriven 32 nm *n*-type FinFET [7]

3.2 Circuit Design Considerations

Next, we look at TCMS circuits in more detail.

3.2.1 Power Consumption in TCMS Circuits

The mechanisms governing power consumption in TCMS are considerably different from conventional multiple-V_{dd} schemes. Conventionally, the use of a lower supply voltage leads to lower dynamic and leakage power consumption in logic gates tied to it. In TCMS, on the other hand, power savings are observed mainly in overdriven inverters. Three mechanisms that govern the power consumption are observed.

1. Subthreshold leakage power consumption in overdriven inverters is reduced due to V_{th} control.
2. The use of a higher V_{dd} leads to higher short-circuit and leakage power consumption in inverters tied to it, as well as higher switching power consumption in capacitances driven by these inverters.

The following guidelines balance the above opposing mechanisms and minimize power consumption. Values for V_{dd}^{H} and V_{SS}^{H} need to be chosen carefully. Higher values lead to larger savings in subthreshold leakage power consumption through TCMS, but also, higher dynamic power consumption. Thus, circuits should be designed such that the parasitic capacitances charged through V_{dd}^{H} and the widths of high-V_{dd} inverters are minimized. Further, the circuit topology should allow repeated use of overdriven inverters in order to maximize power savings.

3.2.2 Exploratory Buffer Design for TCMS

A circuit that provides an ideal theoretical substrate to explore TCMS is a long interconnect wire, driven by identical buffers, inserted at regular intervals. The source and sink nodes are also assumed to be driven by identical buffers. The buffers comprise a pair of inverters in series, with the input inverter being smaller in size than the output inverter. Figure 8 depicts a link in this wire, designed to use

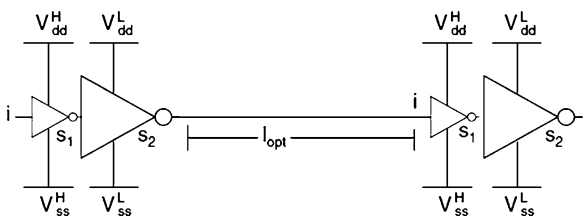


Fig. 8 A buffered link on an infinitely long identical interconnect wire [7]

TCMS. The size of each inverter (s_1 and s_2) is indicated below it in Fig. 8. The length of the link, l_{opt}, is also shown. The smaller inverter in each buffer is tied to V_{dd}^{H} and the larger buffer is overdriven. The design was chosen because of the following features that might help in maximizing power savings:

1. The size of the high-V_{dd} inverter is kept small.
2. The only parasitic capacitances charged through V_{dd}^{H} are the input capacitances of the larger inverters, and output capacitances of the smaller inverters. No wire capacitances, which are typically much larger in value than inverter parasitic capacitances, are charged through V_{dd}^{H}.
3. The larger inverters are overdriven and thus have a much higher I_{on}, presenting a further avenue for saving power: the size of the larger inverters may be reduced, while maintaining delay across the link. Shrinking the larger inverters also reduces the load on the high-V_{dd} inverters feeding them and allows their width to be reduced as well.
4. High- and low-V_{dd} inverters alternate, providing maximum opportunity for power savings. A significant challenge in the above design is the static leakage that would arise in all the high-V_{dd} buffers since they are driven by voltages lower than their power supply and will not switch off properly. To avoid the use of level-converters, high-V_{th} is used in high-V_{dd} buffers to eliminate the static leakage.

The TCMS buffer described above can now be used for low-power buffered interconnect synthesis. As suggested in [7], TCMS buffers outperform dual-V_{dd} buffer insertion schemes in terms of area (by 9% in fin-count) and power consumption (by 2×).

3.3 Logic Design Using TCMS

The concept of TCMS was illustrated through its application to a buffer chain in the previous section. However, TCMS can be extended to any logic gate based on SG-mode FinFET logic gates. This is explained next.

Consider the two-input NAND gate shown in Fig. 9. The power supply voltages for the NAND gates are V_{dd}^{L} and V_{ss}^{L}. Consider the two inputs a and b. They may be the outputs of a high-V_{dd} gate or a low-V_{dd} gate (a high-V_{dd} gate is connected to V_{dd}^{H} and V_{ss}^{H}, and a low-V_{dd} gate to V_{dd}^{L} and V_{ss}^{L}). During circuit synthesis, when this gate is embedded in a larger circuit, it might so happen that a is the output of a high-V_{dd} gate and b comes from a low-V_{dd} gate, or vice versa. Suppose the former is true. Thus, the FinFETs connected to input a follow the TCMS principle explained above. FinFETs connected to input b cannot employ the TCMS principle because there is no gate-to-source voltage difference to exploit.

On the other hand, if the power supply voltages for the NAND gate are V_{dd}^{H} and V_{ss}^{H}, then the FinFETs connected to input a will not be able to take advantage of the TCMS principle. Also, input b is from the output of a low-V_{dd} gate and is driving a

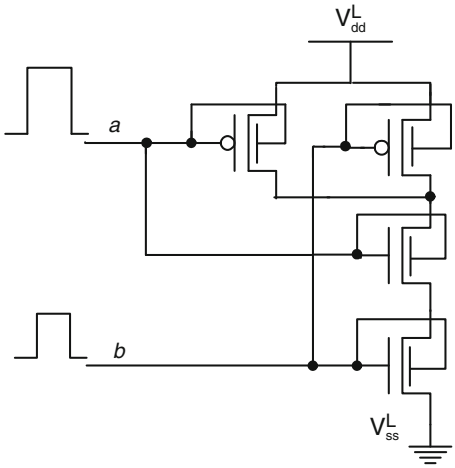


Fig. 9 TCMS principle employed on a NAND gate

high-V_{dd} gate. This results in an increased leakage current because the p-type FinFET is forward-biased by $V_{dd}^{H} - V_{dd}^{L}$. To avoid this problem, a level-converter may be used to restore the signal to V_{dd}^{H}. These level-converters may be combined with a flip-flop, as in the clustered voltage scaling (CVS) technique [11], to minimize the power for voltage-level restoration. In an "asynchronous" approach, such as extended clustered voltage scaling (ECVS) [12], level-converters may be inserted between logic gates connected to V_{dd}^{L} and V_{dd}^{H}. In such schemes, the power and delay overheads for the level-converters are large.

In the case of TCMS, using level-converters is not an attractive option, because power savings are obtained through the use of overdriven gates, the frequent use of which necessitates frequent level conversion. However, level conversion can be built into logic gates without requiring the use of level-converters [13], through the use of a high-V_{th} FinFET at the inputs of high-V_{dd} gates that need to be driven by a low-V_{dd} input voltage. FinFET V_{th} may be controlled through a number of mechanisms. For example, there are several process-related options to statically control the V_{th} of a FinFET, e.g., channel doping, gate work function engineering, or asymmetrical double gates [14].

The first step towards evaluating the utility of the TCMS principle for arbitrary logic circuits involves the design of technology libraries, consisting of high-V_{dd} cells, low-V_{dd} cells, low-V_{dd} cells that are being driven by high-V_{dd} cells, and high-V_{dd} cells that are being driven by low-V_{dd} cells. All these cells have to be characterized at both high-V_{th} and low-V_{th}. Thus, the design variables that need to be targeted are supply voltage, input gate voltage, and threshold voltage. Hence, for a two-input NAND gate of a given size, we have five design variables: supply voltage, gate input voltage for input a, gate input voltage for input b, V_{th} for FinFETs connected to input a, and V_{th} for FinFETs connected to input b.

If the V_{th} of a p-type FinFET connected to an input is high (low), then the corresponding n-type FinFET connected to the same input also has a high (low) V_{th}.

It can be easily seen that 32 two-input NAND gates of a particular size are possible, because of the five design variables. For example, one type of NAND gate may have a high supply voltage (V_{dd}^{H}, V_{SS}^{H}), a low-input *a* gate voltage, a high-input *b* gate voltage, a high V_{th} for FinFETs connected to input *a*, and a low V_{th} for FinFETs connected to input *b*.

Let 1 denote the case when either a high-supply voltage or a high-input gate voltage or a high V_{th} is used. Similarly, let 0 denote when either a low-supply voltage or a low-input gate voltage or a low V_{th} is used. Using this convention, the example NAND gate can be termed *nand10110*. The first 1 in nand10110 denotes a high-supply voltage; thereafter, 0 denotes a low-input *a* gate voltage, third 1 denotes a high-input *b* gate voltage, the fourth 1 represents the high V_{th} for input *a*, and the fifth 0 represents a low V_{th} for input *b*. Thus, 32 NAND gate modes are possible ranging from nand00000 to nand11111. However, certain combinations of design variables are not allowed: a logic gate with a high-supply voltage and low-input gate voltages cannot employ low-V_{th} transistors as this will lead to a large leakage current, as explained earlier. Thus, nand10000, nand10001, nand10010, nand10100, nand10101, nand11000, and nand11010 are not allowed. This leads to 25 NAND gate modes instead of 32.

Similarly, there are 25 NOR gate modes. Because the inverter is a one-input gate, it has three design variables: supply voltage, input gate voltage, and V_{th}. This leads to seven valid modes for inverters. For each NAND, NOR, and inverter mode, we include five sizes: X1, X2, X4, X8, and X16. These numbers denote the size relative to the minimum-sized logic gates. The library is characterized by simulating the delay, leakage, and short-circuit power consumption of each constituent cell in HSPICE. Transistor capacitance is also measured using HSPICE. To model interconnect delay and load, fanout and size-dependent wire load models were obtained by scaling the wire characteristics available as part of a 130-nm technology library, according to the method presented in [15].

A possible power minimization flow is shown in Fig. 10. It starts by mapping the logic netlist to low-V_{dd} gates with low-V_{th} and finding its delay-minimized configuration, using Synopsys Design Compiler. The library of low-V_{dd} gates with low-V_{th} is referred to as the SG library because of its use of SG FinFETs. Thereafter, in Phase I, the circuit is divided into alternate levels of high-V_{dd} and low-V_{dd} gates. The gates at odd levels are changed to high-V_{dd} gates with high-V_{th}. The gates at even levels are changed to other modes of low-V_{dd} gates to maintain circuit consistency, as will be clearer later.

Next, in Phase II, a linear programming-based algorithm is used to assign gate sizes and modes to the mapped circuit by selecting cells from the TCMS library. Cell selection is based on the algorithm presented in [16]. The linear programming formulation can be used for reducing both delay and power in the circuits. The iteration terminates when all the delay constraints are met and the change in power consumption between successive iterations is less than some prespecified percent [17]. The TCMS is shown to reduce both the overall power consumption and fin-count of the benchmark circuits by a factor of 3× under relaxed delay constraints. It also outperforms ECVS.

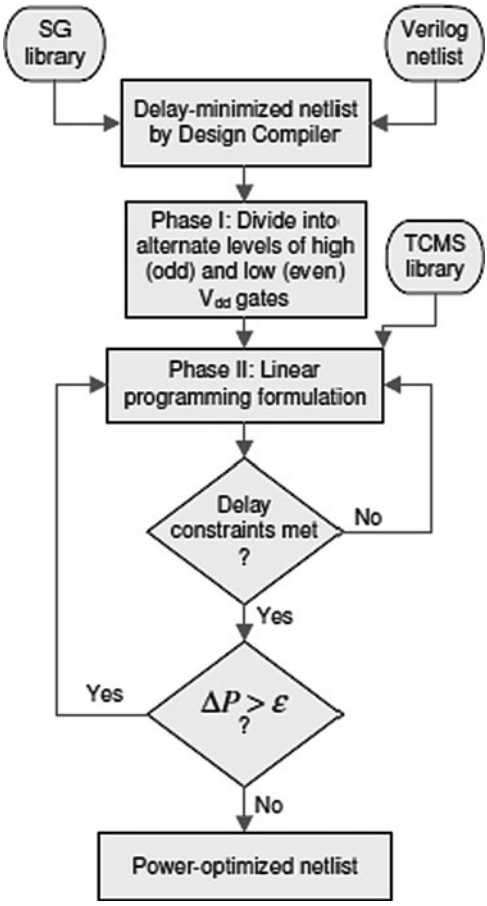


Fig. 10 A possible power-optimization flow

4 Schmitt Trigger

A Schmitt trigger is a high-performance circuit used to shape input pulses and reduce noise. It responds to a slow-changing input pulse with a fast-changing output transition. The voltage-transfer characteristics of the circuit show different switching thresholds for positive and negative going input slopes [18].

Consider the CMOS Schmitt trigger (CMOS-ST) shown in Fig. 11. It consists of an inverter followed by another inverter which is driven by positive feedback. The idea behind the circuit is that the switching threshold of the inverter depends upon the pull-up and pull-down ratio of the transistors. Increasing the ratio raises the switching threshold and vice versa. Adapting the ratio depending upon the direction of the transition results in a shift in threshold and the hysteresis effect [19].

Figure 12 shows the Schmitt trigger based on IG-mode FinFETs. The second inverter and the first inverter in the bulk CMOS case are clubbed together in a single IG-mode inverter. The independent control of the back gate reduces the number of

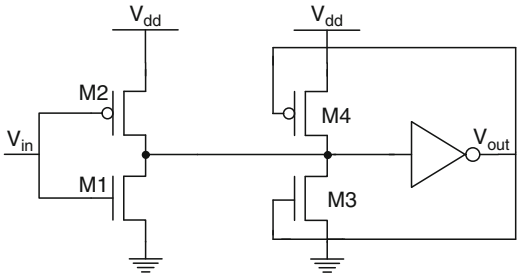


Fig. 11 CMOS Schmitt trigger

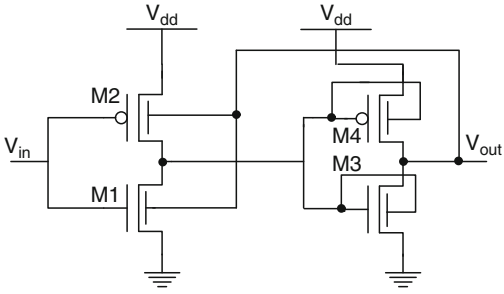


Fig. 12 IG-mode implementation of a FinFET Schmitt trigger

transistors in the circuit by two. Suppose that, initially, the input voltage $V_{\text{in}} = 0$. Then both the gates in the IG-mode p-type FinFET will be active because output voltage $V_{\text{out}} = 0$. This leads to a shift to the right of voltage-transfer characteristics of the inverter formed by FinFETs M1 and M2. On the other hand when $V_{\text{in}} = 1$, IG-mode n-FinFET M1 is active, leading to a shift to the left for the inverter. Figure 13 show the hysteresis loop created by this circuit.

The FinFET Schmitt trigger (FinFET-ST) created in this manner leads to a very large hysteresis window because of the contention between front and back gates of M1 and M2. The shape of the hysteresis window in FinFET-ST can be regulated using asymmetric FinFETs. In asymmetric FinFETs, the back-gate oxide thickness (t_{box}) is increased to approximately $10\times$ that of the front-gate oxide thickness (t_{fox}) to weaken its control on the gate channel, thereby reducing the contention between the front and back gates [20]. Let the ratio $t_{\text{box}}/t_{\text{fox}}$ be labeled S.

Table 2 gives the percentage gate area reduction, delay reduction, and power savings obtained by switching from CMOS-ST to FinFET-ST at iso-noise margins, at two different loading conditions [20]. The reduction in the power–area metrics can be attributed to: (1) reduced number of transistors in FinFET-ST decreases all components of power dissipation, and (2) during switching, the contention between M2 (M1) and the feedback inverter is replaced by a weaker contention offered by the back gates of FinFETs M1 and M2. The gate delays of CMOS-ST and FinFET-ST remain roughly the same due to the weaker contention offered by the back gates of FinFETs M1 and M2.

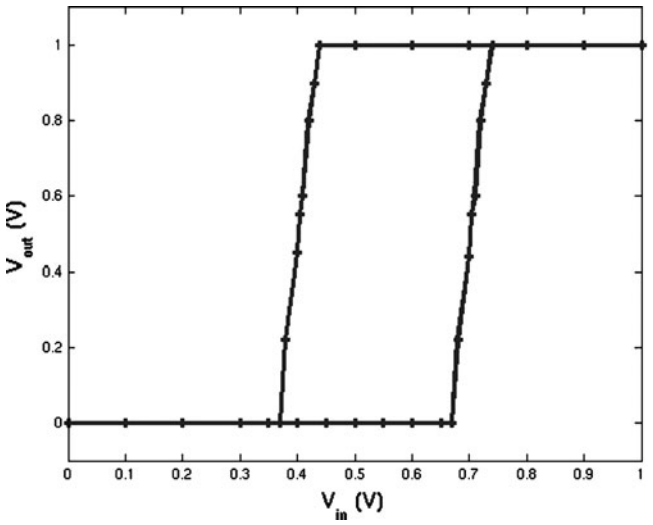


Fig. 13 DC transfer characteristics of IG-mode Schmitt trigger [20]

Table 2 Percent reduction in area, delay, and power of FinFET-ST w.r.t CMOS-ST at iso-noise margins under two different loading conditions [20]

		CL = 1 pF		CL = 1 fF	
$S = t_{box}/t_{fox}$	Gate area (%)	Power dissipation (%)	Delay (%)	Power dissipation (%)	Delay (%)
1	–	–	–	–	–
4	13	12	−7	20	−8
7	12	14	1	25	−0.4
10	10	11	1	24	−0.7

5 Latch Design Using SG/IG-Mode FinFETs

We next switch our attention to FinFET latch design.

5.1 SG-Mode Latch Design

Let us first consider the design of brute-force static FinFET latches. A brute-force latch consists of an inverter driving a transmission gate, which in turn drives a cross-coupled inverter. Careful sizing of the transistors needs to be done for the latch to become operational. The data transfer to the latch shown in Fig. 14 happens due to brute force. To be able to transfer data into the latch, the driver inverter I1 and transmission gate T1 must be stronger than feedback inverter I2. Figure 15 shows the circuit schematic of an SG-mode implementation of this latch. This

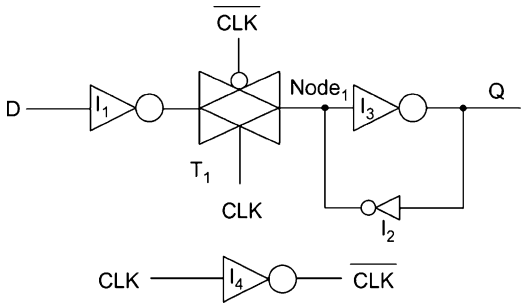


Fig. 14 Brute-force latch [21]

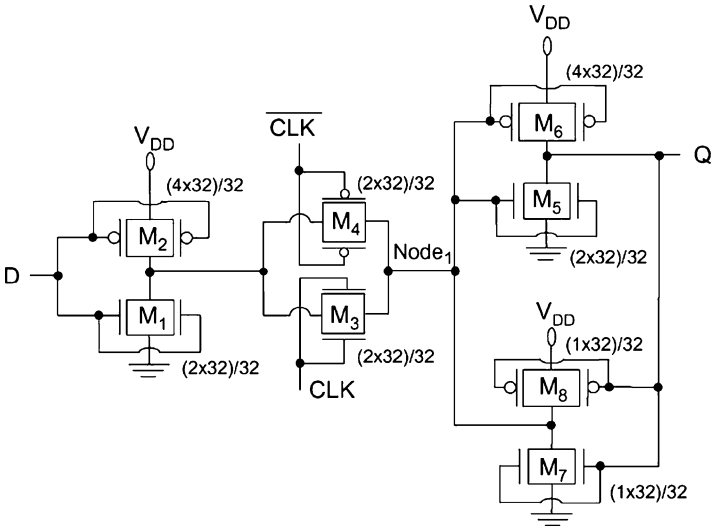


Fig. 15 Circuit schematic of the brute-force latch [21]

schematic has a direct one-to-one correspondence with the conventional bulk CMOS static latch. The driver inverter consisting of M1 and M2, and the transmission gate transistors (M3 and M4) must be sized stronger than the feedback inverter (M7 and M8). The corresponding sizes are shown in the figure. The size of each transistor is given as (number of fins $\times$ h/L_{phys}) [21].

5.2 IG-Mode FinFET Latch

Figure 16 shows the IG-mode implementation of a static FinFET latch [21]. The feedback inverter contains IG-mode transistors. The back gate of M8 is attached to V_{dd} and the back gate of M7 is reverse-biased to ground. This increases the threshold voltage of these transistors, leading to a weakened feedback inverter. Therefore, one does not need to size up the driver inverter and the transmission gate

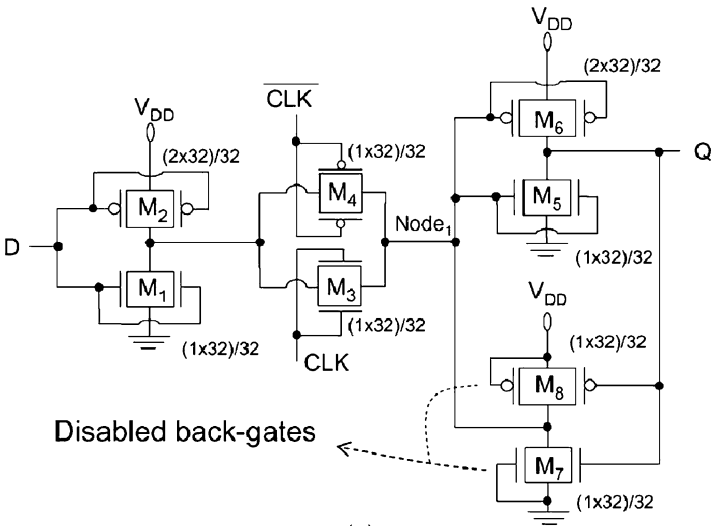


Fig. 16 Circuit schematic of an IG-mode brute-force latch [21]

in order to overpower the feedback inverter. This leads to smaller transistors in the latch. Consequently, we have significantly lower power consumption (switching + leakage) as compared to the SG-mode brute-force FinFET latch.

6 Precharge-Evaluate Logic Circuits

Next, we look at how dynamic logic circuits, such as domino, can exploit FinFETs.

6.1 FinFET Domino Logic Circuits with SG-Mode FinFETs

Domino logic circuits are preferentially used in high-performance architectures. However, they suffer from reliability problems due to the dynamic storage of charge. This effect worsens with technology scaling. Thus, noise immunity vs. speed and power tradeoffs need to be carefully investigated while designing dynamic logic circuits. SG/IG-mode FinFET domino logic provides excellent power–delay savings.

Figure 17 shows a standard footless domino logic circuit in SG-mode FinFET technology. During the precharge phase, the clock (CLK) signal is low, which charges the dynamic node. The output is low, which activates the keeper. During the precharge phase, the inputs must be low in order to avoid a direct short-circuit current path from the power supply to ground. This, in general, is achieved by intentionally delaying the clock signal from the preceding domino stages in a

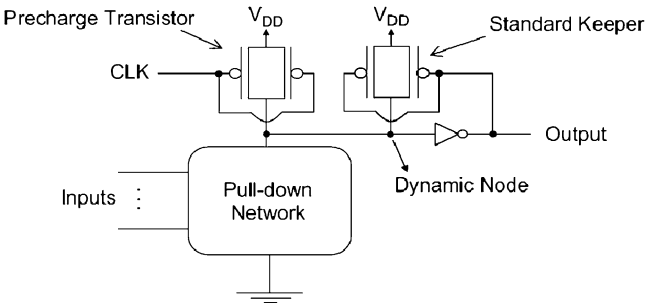


Fig. 17 SG-mode domino logic circuit [22]

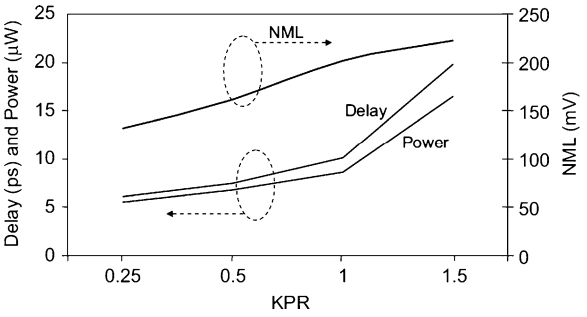


Fig. 18 Evaluation of power, delay, and noise margin of a 16-input OR gate for SG-mode domino in 32-nm technology [22]

multistage domino logic circuit. When the clock signal turns high, the circuit enters the evaluation phase. Provided the input combination provides a discharge path to ground, the dynamic node starts to discharge. However, the pull-down circuitry has to contend with the keeper transistors while it is trying to discharge the dynamic node [22].

Alternatively, if the dynamic node does not discharge during the evaluation phase, the keeper transistor prevents a change in the state of the dynamic node due to coupling noise, charge sharing and subthrehsold leakage.

Simulation results for a 16-input footless domino OR gate are shown in Fig. 18 for various keeper sizes (KPR). KPR is the ratio of keeper size to the size of one of the pull-down network transistors. NML represents the noise margin. NML is measured for the worst case assuming all the inputs of the OR gate are simultaneously excited by the same noise signal. As can be seen from the figure, NML is enhanced by almost 70% when KPR is increased from 0.25 to 1.5. However, this comes at the price of increased evaluation delay (by 3.3×) and power dissipation (by 3×). This problem can be alleviated in a FinFET design, as discussed next.

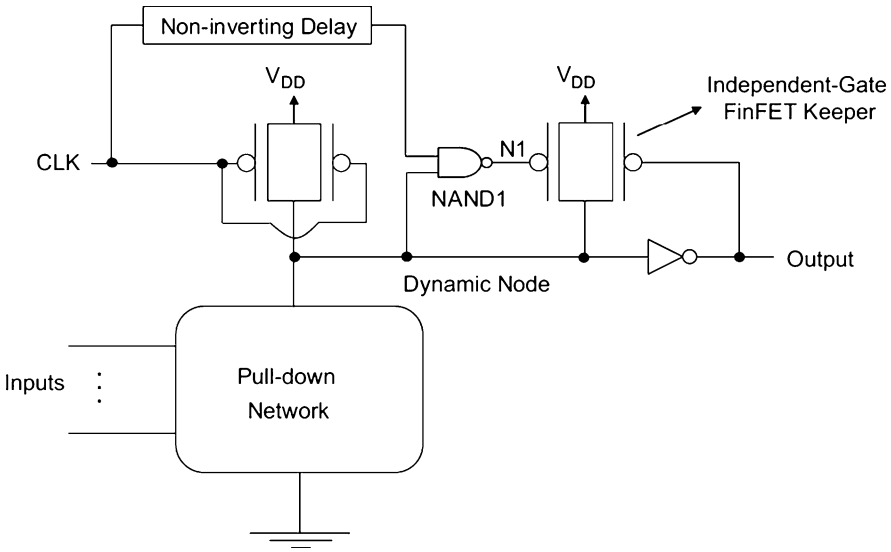


Fig. 19 Schematic of the IG-mode domino logic circuit [22]

6.2 *FinFET Domino Logic with IG-Mode FinFETs*

Figure 19 shows an innovative domino logic style made possible by IG-mode FinFETs. A variable-V_{th} keeper, based on the back-gate biasing technique, is used for simultaneous power and delay reduction at iso-noise margin as compared to the SG-mode FinFET domino circuit mentioned earlier [22].

The proposed circuit works as follows. In the precharge phase, the clock signal is low. The pull-down network is cut off. The keeper control signal N1 becomes high after a fixed delay. This biases one of the independent gates of the FinFET, thereby increasing the threshold voltage of the keeper FinFET. During the evaluation phase, when the clock changes to high and under a specific combination of input values, the dynamic node is discharged to ground. The evaluation speed is increased because of the lower contention current provided by the weakened keeper FinFET. The switching power is reduced because of the decreased contention current provided by the FinFET keeper despite the increased switched capacitance due to the inclusion of the noninverting delay element and NAND gate.

Alternatively, when the pull-down network is not activated, the dynamic node is at V_{dd}, and node N1 transitions to ground after some delay, thus shifting the bias of the IG-mode gate to ground. This essentially reduces the V_{th} of the keeper IG-FinFET. Hence, this FinFET operates with a low V_{th}, providing noise immunity that is similar to the standard SG-FinFET domino logic circuit with the same keeper transistor [22]. Thus, a variable-V_{th} keeper leads to shorter evaluation delay and reduced power consumption at almost iso-noise margins.

7 FinFET Layout

By now, we have some understanding of SG/IG-mode FinFET combinational/sequential circuits, however, not much at the physical level of abstraction. Because the design of digital VLSI circuits is often based on the standard cell approach, an understanding of layout issues in SG/IG-mode standard cells is important.

Let the gate width of a FinFET with a single fin be W_{min}. As mentioned earlier, the gate width of a multi-fin FinFET is quantized in the number of fins. The higher values of widths are achieved by connecting a number of fins (N_{FIN}) in parallel. Figure 20 shows an SG-mode FinFET in which four fins have been connected in parallel. The width of this device is $4W_{\text{min}}$. The area occupied by this device is proportional to $(N_{\text{FIN}} - 1)/P_{\text{FIN}}$, where P_{FIN} is the fin pitch defined by the process technology.

Currently, there are two different kinds of technologies used to define P_{FIN}. In particular, for the lithography-defined FinFET technology, P_{FIN} is set by the lithographic resolution of the process. On the other hand, in the spacer-defined technology, P_{FIN} can be reduced to half, thus enabling the use of sublithographic control of fin pitch. The device area also consists of the source/drain diffusion and gate underlap. This area remains the same in both types of process technologies. Another method for reducing the layout area is based on increasing W_{min}, which, in turn, amounts to increasing the fin height [23]. However, to keep the short-channel effects under control, arbitrarily large values of fin height cannot be chosen. A certain ratios need to be maintained among fin height, channel length, and fin width for process feasibility and reduced short-channel effects.

Figure 21 shows the layout of an IG-mode FinFET. In such a FinFET, the front and back gates have a separate contact and, thus, the fin pitch needs to be increased to accommodate the back-gate contact. Consequently, the fin pitch in IG-mode FinFETs is greater than the fin pitch in SG-mode FinFETs. The fin pitch in IG-mode FinFETs is given by $T_{\text{Si}} + \text{DR1} + 2(\text{DR2} + \text{DR3})$, where DR1, DR2, and DR3 are technology-specified design rules. Also, IG-mode FinFETs do not benefit from spacer lithography due to the increased fin pitch. Therefore, IG-mode devices are expected to have far inferior layout density as compared to that of SG-mode devices [23].

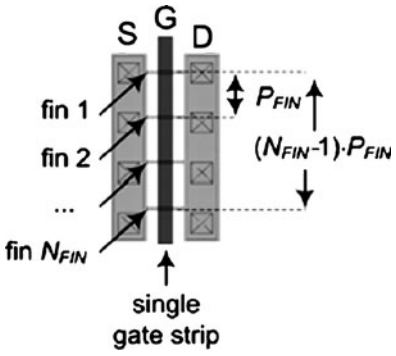


Fig. 20 SG-mode FinFET layout [23]

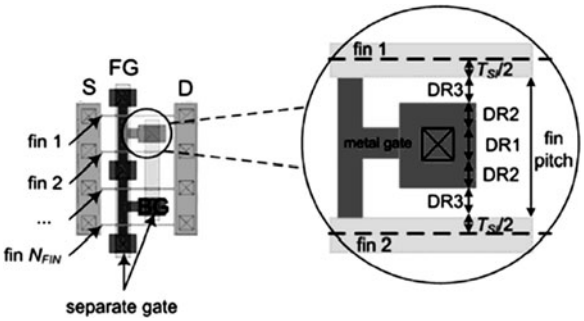


Fig. 21 IG-mode FinFET layout

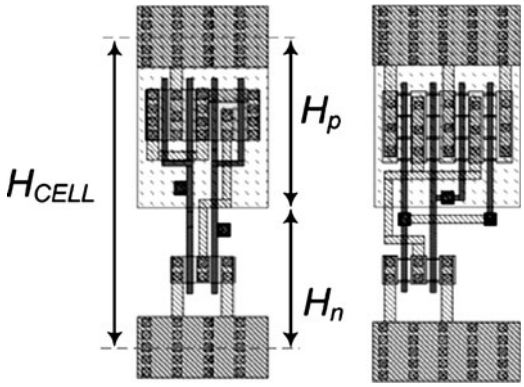


Fig. 22 Layout of 2× NOR2 in CMOS and SG-mode FinFET [23]

7.1 Layout Analysis of FinFET Standard Cells (SG/IG-Mode)

Figure 22 shows the layout of a 2× two-input NOR cell (referred to as NOR2) based on bulk CMOS and SG-mode FinFETs using lithography-defined technology. Figure 23 shows the layout of SG-mode FinFET in spacer technology. In Fig. 22, the standard cell height HCELL was nominally set to 14 tracks of metal 2, whereas the ground/supply rails were assumed to be 2.5 tracks tall.

In this layout, the height H_p corresponding to p-type FinFETs was set to 1.5 times the height H_n corresponding to n-type FinFETs. NAND, INV, AOI, and other kinds of standard library cells can be laid out in a similar fashion. Figure 24 shows the layout of a 2× NOR2 cell in IG-mode.

Table 3 gives the area results of FinFET 2× NOR2 cells (SG/IG-mode) normalized to the cell implemented in bulk CMOS using both spacer- and lithography-defined technologies. It can be seen from the table that the SG-mode NOR gate has superior layout density as compared to that of bulk CMOS when spacer-defined technology is used. On the other hand, SG-mode NOR and bulk CMOS NOR gates have comparable areas when lithography-defined technology is used. However, the

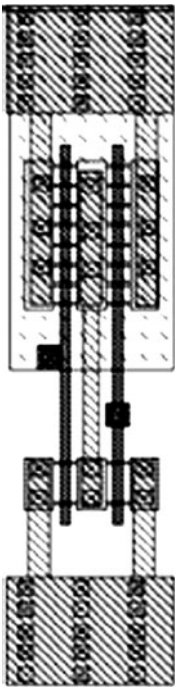


Fig. 23 SG-mode NOR2 layout in spacer technology [23]

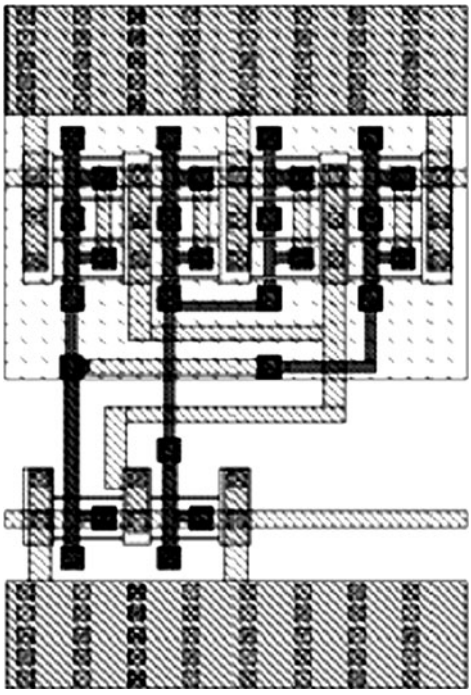


Fig. 24 IG-mode 2× NOR2 layout [23]

Table 3 Normalized area of 2× NOR2 cell w.r.t conventional CMOS layout [23]

	SG-mode	IG-mode
Lithography defined	1.1	2
Spacer defined	0.7	2

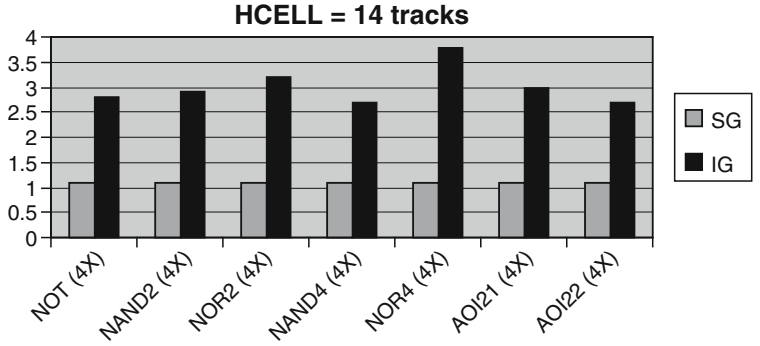


Fig. 25 Area of SG-mode and IG-mode cells using lithography-defined technology normalized w.r.t conventional CMOS technology [23]

IG-mode NOR gate occupies twice the area as compared to bulk CMOS. Similar trends are observed for other gates in the library implemented using lithography-defined technology, as shown in Fig. 25 [23]. Therefore, clever choices need to be made when area and leakage both are a major concern.

8 Oriented FinFETs

An added advantage of the FinFET is that it can be easily fabricated along different channel planes in a single die. Fabrication of conventional planar MOSFETs along any plane other than $\langle 100 \rangle$ is difficult due to increased process variations and interface traps. Furthermore, to obtain different transistor orientations, the devices have to be fabricated along trench sidewalls. With the advent of FinFETs, fabrication of transistors along the $\langle 110 \rangle$ plane has become feasible, leading to design of circuits using differently oriented transistors. Electron mobility is highest in the $\langle 100 \rangle$ plane and the hole mobility along the $\langle 110 \rangle$ plane. Thus, logic gates consisting of *p*-type FinFETs implemented in the $\langle 110 \rangle$ plane and *n*-type FinFETs in the $\langle 100 \rangle$ plane will be the fastest. This can be achieved by orienting the *p*-type FinFETs to be either perpendicular or parallel to the flat or notch of a $\langle 100 \rangle$ wafer and orienting the *n*-type FinFET fins to be rotated at a 45° angle . The non-Manhattan layout may pose certain yield issues [3].

To quantify the delay of the variously oriented transistors, simulations were performed using a double-gate HSPICE model, called BSIM [24], in conjunction with UFDG [5]. Figure 27 shows the variation in *p*-type (*n*-type) FinFET drain-to-

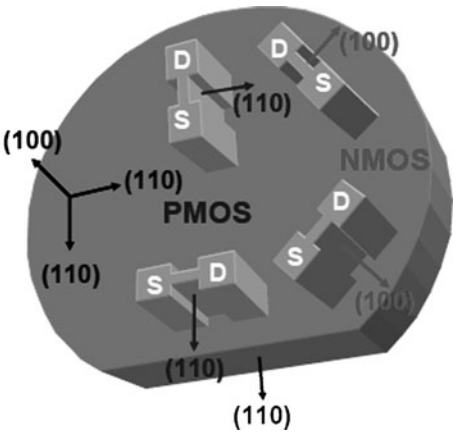


Fig. 26 Si wafer showing differently oriented transistors [3]

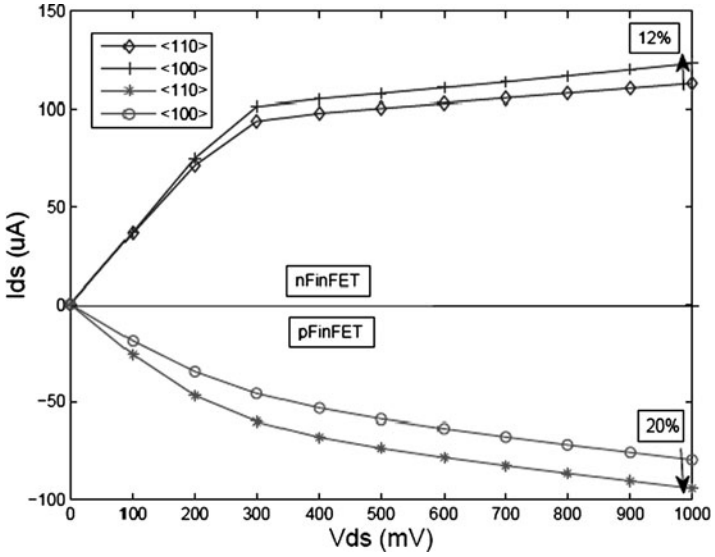


Fig. 27 I_{ds} vs. V_{ds} characteristics for *p*-type and *n*-type FinFETs in the ⟨110⟩ and ⟨100⟩ channel orientations

source current (I_{ds}) with drain-to-source voltage (V_{ds}) for different channel orientations at the 32-nm FinFET technology node. BSIM also takes into account the quantum-mechanical effects on carrier mobility for different channel orientations. As shown in Fig. 27, when the orientation changes from ⟨100⟩ to ⟨110⟩, the saturation current for *p*-type FinFETs increases by around 20%, whereas for *n*-type FinFETs, when the orientation changes from ⟨110⟩ to ⟨100⟩, it increases by 12%. There is a larger increase in the *p*-type FinFET current drive when the channel orientation changes because of the smaller dependence of the hole mobility

on velocity saturation. The change in carrier mobility due to transistor orientation is diminished by the velocity saturation effect.

8.1 Library Design Using Oriented FinFETs

To exploit oriented FinFETs, two additional kinds of libraries can be constructed: the oriented shorted-gate (OSG) and the oriented low-power (OLP) gate. The OSG library contains logic gates with a pull-up network that consists of *p*-type FinFETs oriented along the ⟨110⟩ plane, whereas the pull-down network uses *n*-type FinFETs in the ⟨100⟩ plane. Thus, these gates are faster than SG gates, as explained earlier. However, OSG logic gates incur an area penalty because of the oriented *p*-type FinFETs used in the pull-up network. OLP logic gates have oriented *p*-type FinFETs and a reverse voltage bias applied to the back gates of all their FinFETs in order to increase the effective V_{th} of the front gate. This allows leakage–delay tradeoffs. One needs to quantitatively study the performance and power characteristics of FinFET logic gates in various channel orientations.

The bar graphs in Fig. 28 show the percent decrease in delay (w.r.t. to ⟨100⟩ oriented gates) for a minimum-sized INV, NAND, and NOR gates in the ⟨110⟩ orientation and in the optimized orientation where the pull-up network is in the ⟨110⟩ plane and the pull-down network is in the ⟨100⟩ plane. The delay is the average of the rising and falling delays. The logic gates have been sized to closely match the rising and falling delays. For the ⟨110⟩ case, all the FinFETs in the logic gates are in the ⟨110⟩ plane. The reduction in delay when the INV is switched from the ⟨100⟩ plane to the optimized orientation is 8%, whereas the reduction in delay

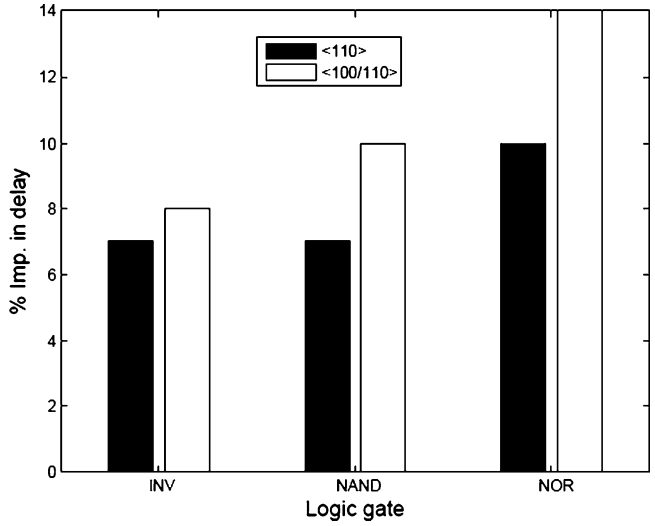


Fig. 28 Percent improvement in delay of various logic gates w.r.t ⟨100⟩ orientation

for the NAND (NOR) gate is 10% (14%). The reduction in delay for a NOR gate is maximum because the improvement in hole mobility has a maximal effect on stacked *p*-type FinFETs. There is also a reduction in delay when we move to the ⟨110⟩ orientation, despite degradation in electron mobility, because the increased hole mobility in this plane reduces the rising time delay. However, as expected, the delay reduction in the ⟨110⟩ orientation is smaller as compared to the optimal configuration because of the degraded electron mobility in the ⟨110⟩ plane. The delay reduction in the ⟨110⟩ plane for the INV is 7%, while the delay reduction for the NAND (NOR) gate is 7% (10%) [3].

Thus, a standard cell library consisting of OSG- and OLP-mode gates can be developed. This can further enrich the library comprising SG-, LP-, and IG-mode logic gates. Because the logic gates in the library offer power–delay tradeoffs, interesting delay-constrained power-optimized circuit netlists can be developed. Various gate-sizing techniques can be used to exploit the benefits of the unique standard cell libraries developed using FinFETs [3].

9 Conclusions

FinFETs are a promising substitute for bulk CMOS for meeting the challenges being posed by the scaling of conventional MOSFETs. Due to its double-gate structure, it offers innovative circuit design styles. In this chapter, we explored different kinds of cell libraries that are possible via SG-, LP-, IG-, and IG/LP-mode FinFET logic gates. We looked at power–delay tradeoffs made possible by these cell modes. We also discussed how delay-optimal FinFET gates can be obtained by fabricating *p*-type FinFETs in the ⟨110⟩ channel orientation and *n*-type FinFETs in the ⟨100⟩ orientation. This can further enrich the cell library. A power optimizer can be used to synthesize FinFET circuits using cells from these libraries under delay constraints. We also discussed an innovative circuit design technique called TCMS. It can be used for interconnect as well as logic synthesis. It offers power as well as area savings relative to conventional state-of-art dual-V_{dd} schemes.

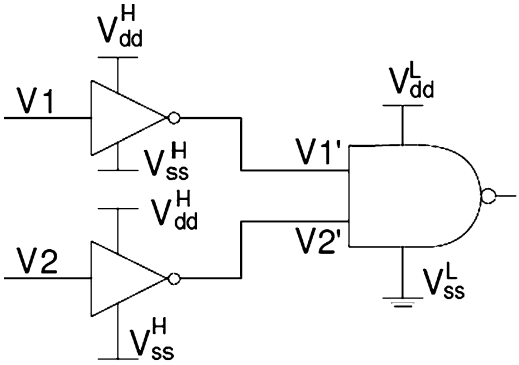
FinFETs also enable new sequential circuit designs. We studied new FinFET designs of the Schmitt trigger, latch, and domino logic circuits. An IG-mode Schmitt trigger offers superior power, delay, and area numbers relative to SG-mode Schmitt trigger at iso-delay margins. New IG-mode latch and domino logic circuits provide superior power and area at iso-delay margins. We also discussed the physical implementation of FinFET circuits. We showed that layouts based on spacer lithography occupy smaller area relative to lithography-defined layouts. We also found that IG-mode layout density is inferior to that of SG-mode and bulk CMOS technology because of the large area occupied by the intermediate contacts.

Exercises

1. Why are FinFETs termed *quasi-planar* devices?
2. Consider a two-input NOR gate.

(a) Draw the SG-mode implementation of the NOR gate.
(b) Size the NOR gate such that the worst-case rising and falling delays are matched. Assume that hole mobility is half of electron mobility.
(c) Draw an LP-mode implementation of the NOR gate.
(d) Suppose that the driving strength of SG-mode FinFETs is 1.5 times that of LP-mode FinFETs. If the delay of an SG-mode NOR gate is t_p, what is the delay of the LP-mode NOR gate.
(e) If the dynamic power consumption of the unloaded SG-mode NOR gate is P, what is the dynamic power consumption of the unloaded LP-mode NOR gate?
(f) What is the worst-case leakage vector of a two-input NOR gate?
(g) If the worst-case leakage power of an SG-mode NOR gate is L, what is the worst-case leakage of an LP-mode NOR gate. (Assume that the leakage of an IG-mode FinFET is 10% that of an SG-mode FinFET.)
(h) If we double the number of fins in all IG-mode FinFETs, how are the delay, leakage, and dynamic power consumption of the LP-mode NOR gate affected?

3. Consider the figure shown below



Let $V_{dd}^{H} = 1.08$ V, $V_{ss}^{H} = -0.8$ V, $V_{dd}^{L} = 1.0$ V, and $V_{ss}^{L} = 0$ V. Assume all the following leakage numbers for the different input vectors are in nW.

Leakage power for a high-V_{dd} inverter:	
1	385.22
0	150.00

Leakage power for a low-V_{dd} NAND gate driven by high-V_{dd} inputs:	
00	2.83
01	52.36
10	50.95
11	150.2

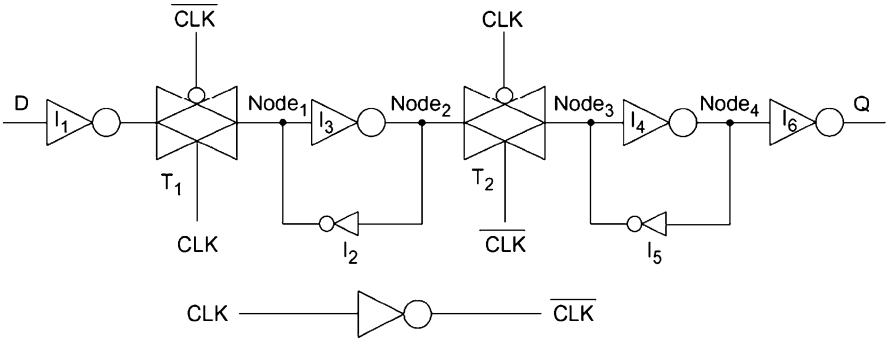
Also, consider an implementation of the circuit where all the gates are driven using V_{dd}^{L} and ground.

Leakage power for a low-V_{dd} inverter:	
1	343.21
0	127.38

Leakage power for a low-V_{dd} NAND gate:	
00	14.06
01	230.3
10	210.6
11	636.4

(a) Compare the leakage of the TCMS and low-V_{dd} circuits across all input vector combinations.
(b) Which circuit leaks less and why?
(c) Explain how the circuit shown above makes use of the TCMS concept?
(d) Assuming that the inverters see an input capacitance of 170 aF, what is the dynamic power consumption under two different scenarios: TCMS and low-V_{dd}. (Assume switching activity = 0.1 and operational frequency = 1 GHz.)
(e) Compare the total power consumption under the two scenarios?

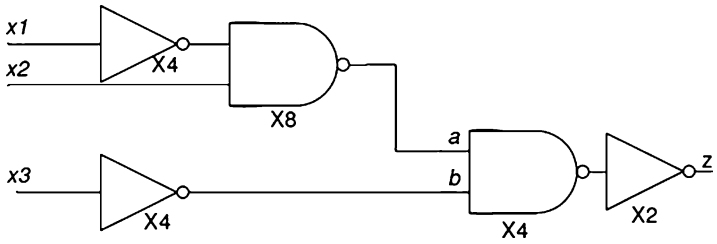
4. Consider the circuit shown in the figure below:



(a) What does the above circuit do?
(b) Which transistors need to be sized stronger and which weaker in order for the above circuit to operate?
(c) Draw an SG-mode circuit schematic of the above circuit.
(d) Taking inspiration from Sect. 5.2, draw an IG-mode implementation of the above circuit. (Bias p-type FinFETs to V_{dd} and n-type FinFETs to ground)
(e) Which transistors were changed to IG-mode FinFETs and why?
(f) Comment on the sizing of the IG-mode implementation of the circuit?
(g) Which implementation is expected to have better average propagation delay and why?
(h) Which implementation is expected to have better average leakage current and why?

(i) Which implementation is expected to have a lower clock power consumption and why?

5. Consider the circuit shown below



(a) Divide the circuit into levels.
(b) Divide the circuit into alternate levels of V_{dd}^{H} and V_{dd}^{L} such that a minimum number of level-converters are required. (Assume that the input level is the same as that of the V_{dd} of the input gate.)
(c) Which gates need to employ high-V_{th} in order to avoid the need for level-converters?

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