Preface

After enjoying a three-decade ride as the top semiconductor technology for implementing integrated circuits (ICs), the era of single-gate complementary metal-oxide semiconductors (CMOS) is coming to an end. Waiting in the wings as replacements are various interesting new nanotechnologies. In the past decade, a contender for replacing bulk CMOS technology has been double-gate field-effect transistor technology, most manufacturable of which are FinFETs. There are also other contenders, such as nanowires, carbon nanotubes, graphene nanoribbons, resonant tunneling diodes, quantum cellular automata, etc. We may also soon see hybrid nano/CMOS designs in which the memory has been implemented in a new technology, while the processing elements have been implemented in CMOS.

Although these nanotechnologies have attracted significant attention over the last decade, the emphasis of interest, as expected, has been more on their physics, chemistry, and fabrication aspects. However, interesting new nanoelectronic circuit designs are beginning to emerge that herald an exciting new era of IC design. These designs deal with both logic as well as interconnect.

Our aim in this book is to introduce readers to the emerging design paradigms in various nanotechnologies, and to bridge the existing gap between nanodevice research and nanosystems design. The book focuses on state-of-the-art research activities, yet, at the same time, covers the fundamental principles behind the nanotechnology developments. The ultimate goal is to expose the great potential of nanoelectronic technology and the unique challenges it poses along the device-to-system spectrum. A rich set of references is included at the end of each chapter to give pointers to readers who want to dig deeper. In addition, some exercises are also included in each chapter to allow the use of the book for a first-year graduate-level course on nanoelectronic circuit design.

The book is organized by grouping together chapters on each nanotechnology. Chapter 1 introduces various nanotechnologies. Chapters 2 and 3 deal with FinFET logic and memory design. Chapter 4 describes a nano/CMOS dynamically reconfigurable architecture. Chapters 5–7 discuss nanowire-based ICs and architectures. Chapters 8 and 9 describe how reliable logic circuits and field-programmable gate

arrays can be built using nanotubes. Chapter 10 deals with circuit design based on graphene nanoribbon transistors. Chapter 11 compares copper, nanotube, graphene, and optics for implementing interconnects on chips. Chapters 12 and 13 discuss circuit design with resonant tunneling diodes and quantum cellular automata, respectively. The chapters are fairly independent of each other. Thus, any subset can be chosen for a one-semester course.

Last, but not the least, Niraj would like to thank his father, Dr. Chintamani Jha, his wife, Shubha, and his son, Ravi, for their encouragement and understanding. Deming would like to thank his wife, Li, and his sons, Jeffrey and Austin, for their love and understanding.

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