

Chapter 2

RADIO-FREQUENCY POWER HARVEST

Passive wireless microsystems harvest their operational power from the radio-frequency waves emitted from their base stations. Based on the characteristics of the wireless links with base stations, passive wireless microsystems are loosely classified as inductively-coupled also known as near-field-coupled and electromagnetically-coupled also known as far-field-coupled. The boundary that separates the near-field and far-field is defined as $\frac{\lambda}{2\pi}$ where λ is the wavelength of the signals. Near-field-coupling is viable for frequencies up to a few ten MHz, mainly due to the low resonant frequency of the planar coupling coils. Near-field-coupling has been widely used in applications such as biomedical implants where a high degree of the absorption of electromagnetic waves by living bodies exists at high frequencies. The key characteristics of a near-field-coupled passive wireless microsystem include a large voltage at the coupling coils of the microsystem and weak interferences from neighboring devices due to the close distance between the base station and the passive wireless microsystem. Far-field-coupling, on the other hand, is used at ultra-high frequencies (UHF) and microwave frequencies, such as ISM 900 MHz and 2.4 GHz bands. A high data rate, a small antenna dimension, and a long link distance are the key characteristics of far-field-coupled passive wireless microsystems. The fact that the maximum EIRP of base stations in North America can not exceed 4 W in UHF bands limits the maximum distance between a far-field-coupled microsystem and its base station to a few meters [42]. The efficiency of power harvest from RF waves determines the maximum distance over which a reliable wireless link between a base station and a passive wireless microsystem can be established. The efficiency of radio-frequency power harvest is determined by a number of factors including the efficiency of the antenna of the microsystem, the accuracy of power matching between

the antenna and the voltage multiplier, and the power efficiency of the voltage multiplier that converts the received RF signal to a dc voltage from which the microsystem is powered.

This chapter deals with power harvest from radio-frequency waves. The chapter is organized as the follows : Section 2.1 investigates the figure-of-merits that characterize the performance of RF power harvesters. Section 2.2 focuses on the design of voltage multipliers for passive wireless microsystems in the far field of the antenna of the base stations. In Section 2.3, power-matching and gain-boosting using a LC network is investigated. Section 2.4 presents power-matching and gain-boosting using a step-up transformer. Frequency tuning mechanisms for power-matching and gain-boosting using a LC network and that using a step-up transformer are also addressed. The measurement results of the proposed power-matching network, together with the measurement results of a LC power-matching network are compared. The chapter is concluded in Section 2.5.

2.1 Characterization of Radio-Frequency Power Harvest

The efficiency of power harvest from a radio-frequency wave determines the maximum distance over which a reliable link between a base station and a passive wireless microsystem can be established. It also sets the complexity subsequently the functionality of the microsystem. The efficiency of a radio-frequency power harvesting system is determined by the efficiency of the antenna of the microsystem, the accuracy of impedance matching between the antenna and the voltage multiplier of the microsystem, and the power efficiency of the voltage multiplier that converts a received RF signal to a dc voltage from which the microsystem is powered.

2.1.1 Power Matching

The radiation resistance of the antenna of passive wireless microsystems has a typical value of 50Ω at the desired frequency. The input impedance of voltage multipliers typically has a reactance component, owing to the capacitance of rectifying diodes or MOSFETs. An impedance transformation network is therefore required to transform the input impedance of the voltage multiplier to 50Ω .

Consider Fig.2.1 where an impedance transformation network is inserted between the antenna represented by voltage source V_a and radiation resistance R_a and the voltage multiplier represented by resistor R_L . Note that to simplify analysis, the input impedance of the voltage multiplier is assumed to be purely resistive. Note that a pure resistive input impedance of voltage multipliers can be obtained by employing a shunt inductor that resonates out the reactive part of the input impedance of the voltage multiplier [42]. The function of

the impedance transformation network is two-fold : (i) It provides a matching impedance to the antenna to maximize the power transmission from the antenna to the voltage multiplier and to minimize the reflection of the signals. (ii) It provides a large voltage gain such that the voltage at the input of the voltage multiplier or the output of the impedance transformation network is maximized. If we assume that the impedance transformation network is lossless, the power delivered to the impedance transformation network will be the same as that delivered to the load. A large voltage at the input port of the voltage multiplier will reduce the power loss at the voltage multiplier. As a result, the overall power efficiency of the power harvesting path is improved. The power delivered to the load R_L is given by [43]

$$P_L = \frac{V_L^2}{R_L} = \frac{A_v^2 V_a^2}{R_L}, \quad (2.1)$$

where A_v is the voltage gain provided by the impedance transformation network.

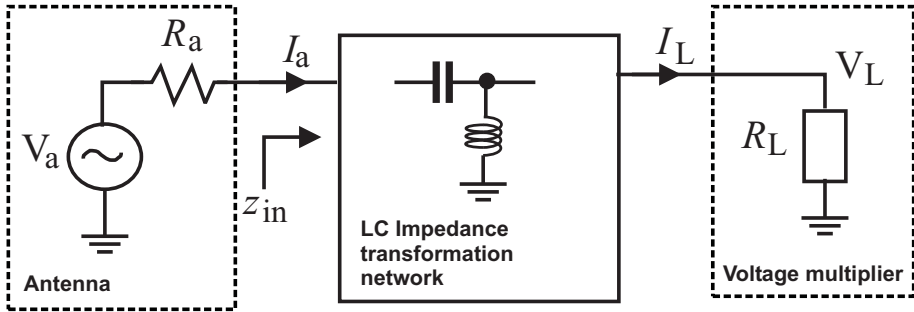


Figure 2.1. Power-matching and gain-boosting using an impedance transformation network.

The maximum power will be delivered from the antenna to the impedance transformation network when

$$R_a = z_{in}^* \quad (2.2)$$

is satisfied, where z_{in} is the input impedance of the impedance transformation network and the superscript $*$ denotes complex conjugation. Since in this case

$$I_a = \frac{V_a}{R_a + z_{in}} = \frac{V_a}{2R_a}, \quad (2.3)$$

we obtain the maximum power delivered from the antenna to the impedance transformation network

$$P_{L,max} = |I_a^2| \Re [z_{in}] = \frac{V_a^2}{4R_a}. \quad (2.4)$$

Eq.(2.4) is also the maximum power delivered to the load provided that the impedance transformation network is lossless. Equating (2.1) and (2.4) yields the relation between the voltage gain of the impedance transformation network and the load resistance at which the power delivered to the load is maximized

$$A_v = \frac{1}{2} \sqrt{\frac{R_L}{R_a}}. \quad (2.5)$$

Eq.(2.5) reveals that the voltage gain of the lossless impedance transformation network is proportional to the square-root of the load resistance.

2.1.2 Power Efficiency

The power efficiency of a voltage multiplier is defined as the ratio of the output power of the voltage multiplier, denoted by P_{out} , to the power at the input of the voltage multiplier, denoted by P_{in}

$$\eta_V = \frac{P_{out}}{P_{in}}. \quad (2.6)$$

The power efficiency of voltage multipliers is less than 100% due to the power consumption of rectifying devices of voltage multipliers.

The power efficiency of an impedance transformation network is defined as the ratio of the power delivered to the multiplier, denoted by P_L , to the power available at the input of the impedance transformation network, denoted by P_{in}

$$\eta_I = \left. \frac{P_L}{P_{in}} \right|_{z_{in}=R_a}. \quad (2.7)$$

Note that power-matching condition

$$z_{in} = R_a \quad (2.8)$$

must be met at the input of the impedance transformation network for the maximum power transfer from the antenna to the impedance transformation network. The power efficiency of impedance transformation networks is less than 100% due to the resistive loss of these networks.

The global power efficiency of a RF power harvester is defined as the ratio of the incident power of the RF signal to the dc power at the output of the voltage multiplier

$$\eta = \frac{\text{DC output power}}{\text{Incident RF power}}. \quad (2.9)$$

The incident RF power, denoted by P_{RF} , is quantified by Friis relation [44]

$$P_{RF} = P_B G_B G_M \left(\frac{\lambda}{4\pi r} \right)^2, \quad (2.10)$$

where P_B is the amount of the power that the base station provides to its antenna, G_B is the gain of the antenna of the base station, G_M is the gain of the antenna of the passive wireless microsystem, λ is the wave length, and r is the distance between the passive wireless microsystem and its base station. Often, the effective isotropically radiated power, denoted by P_{EIRP} , is used. It is obtained from

$$P_{EIRP} = P_B G_B. \quad (2.11)$$

2.2 Voltage Multipliers

Wireless communications between a near-field passive wireless microsystem, such as a biomedical implant or a smart card, and its base station is established using an inductive link, much like a transformer with the base station connected to the primary winding of the transformer and the passive wireless microsystem connected to the secondary winding of the transformer. One of the key characteristics of this inductive link is the large voltage at the secondary winding. As a result, RF-to-DC conversion can be carried out using a diode bridge even with the voltage loss across the diodes accounted for. The dc voltage at the output of the diode bridge is sufficiently large to power the passive wireless microsystem. To minimize the voltage loss across the diodes so as to improve RF-to-DC conversion efficiency, Schottky diodes, which typically have a low forward conduction voltage, are widely used [4, 6]. Schottky diodes, however, are not available in standard CMOS processes. Instead, MOSFET-based diodes formed by connecting the gate and drain together can be used for rectification such that the voltage rectifier can be implemented using standard CMOS technologies. Not that there is a voltage loss of at least one device threshold voltage when MOSFET-diodes are used.

Wireless communications between a far-field passive wireless microsystem, such as a RFID tag or a wireless microsensor, and its base station is established

using a radio-frequency wave. Unlike near-field inductive links, the voltage at the antenna of the passive wireless microsystem is small, typically a few hundred mV. Diode bridge-based rectification approaches become very inefficient as the voltage loss across the diodes is significant as compared with the amplitude of the incoming RF signal. Voltage multipliers that are evolved from the well-know voltage doubler are required to perform RF-to-DC conversion and at the same time to yield a dc voltage that is many times the amplitude of the incoming RF signal.

This section investigates design techniques for voltage multipliers of passive wireless microsystems. The design constraints of voltage multipliers and the techniques that improve the power efficiency of voltage multipliers are studied. The principle and operation of diode bridges, both half-wave and full-wave diode bridges, are readily available in standard texts on microelectronics and will therefore not be presented here.

2.2.1 Voltage Doubler

Shown in Fig.2.2 is the schematic of a widely used voltage doubler. It consists of a voltage peak detector formed by D2 and C2 and a voltage clamper formed by D1 and C1. If we assume that the diodes are ideal, i.e. the forward conduction voltage is zero, and let the amplitude of the input ac voltage be V_m , it can be shown that voltage of the output of the voltage doubler is $2V_m$. To demonstrate this, let us assume initially $V_{C1} = 0$, $V_{C2} = 0$, and $C_1 = C_2$.

During the first negative half-cycle of the input voltage, D1 will be forward biased. C1 in this case will be charged to a voltage equal to the peak amplitude V_m of the input. During the following positive half cycle of the input voltage, D1 will be reverse biased and therefore will not conduct current. The voltage across C1 will remain unchanged and will add on to the input voltage, in other word, $V_1 = v_{in} + V_m$ during this half cycle. Since D2 is forward biased, C_2 will be charged all the way to $2V_m$.

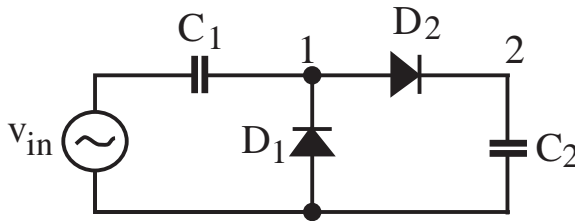


Figure 2.2. Voltage doubler.

2.2.2 Cockcroft-Walton Voltage Multiplier

To obtain a dc voltage that is more than $2V_m$, a multi-stage configuration of voltage doublers is needed. Perhaps the most cited early implementation of voltage multipliers is Cockcroft-Walton voltage multiplier shown in Fig.2.3 [20]. The efficient multiplication of Cockcroft-Walton voltage multiplier will only occur if the capacitance of the coupling capacitors C is much larger as compared with the stray capacitance C_s at the coupling nodes [21]. This is because the clocking signals ϕ and $\bar{\phi}$ only drive the first two coupling capacitors. All other coupling capacitors are connected in series with the stray capacitors. The effectiveness of Cockcroft-Walton voltage multiplier largely diminishes in monolithic integration where stray capacitance C_s and C become comparable.

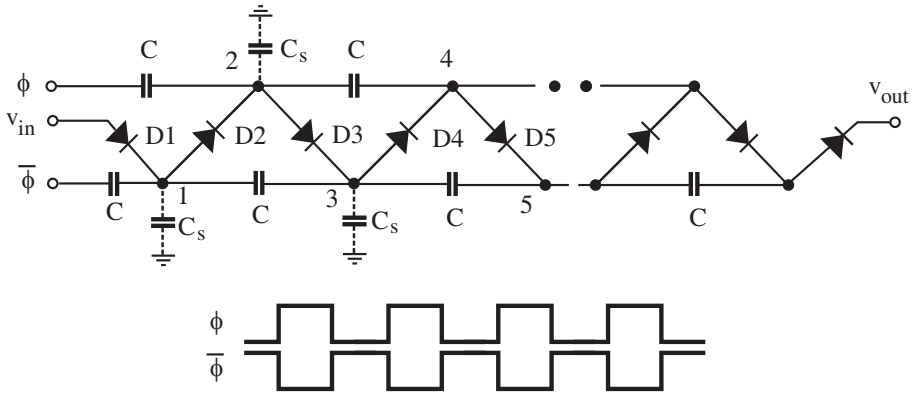


Figure 2.3. Cockcroft-Walton voltage multiplier [20].

2.2.3 Dickson Voltage Multipliers

Dickson modified Cockcroft-Walton voltage multiplier by injecting clocking signals ϕ and $\bar{\phi}$ to all the coupling nodes, as shown in Fig.2.4, such that both the coupling and stray capacitors are driven by the clocking signals directly [21]. The drawback of Cockcroft-Walton voltage multiplier is therefore eliminated. Because these capacitors are connected in parallel, the shunt capacitor connected to the output node of the Dickson voltage multiplier must withstand the full output voltage. It was shown in [34] that the output voltage of a N-stage diode-based Dickson voltage multiplier is given by

$$V_{DC} = N(V_m - V_T), \quad (2.12)$$

where V_T is the forward conduction voltage of the diodes and N is the number of stages. To boost the output voltage, the threshold voltage of the rectifying

diodes must be minimized. Schottky diodes are widely used in Dickson voltage multipliers due to their low forward conduction voltage, large saturation current, low junction capacitance, and small series resistance [34].

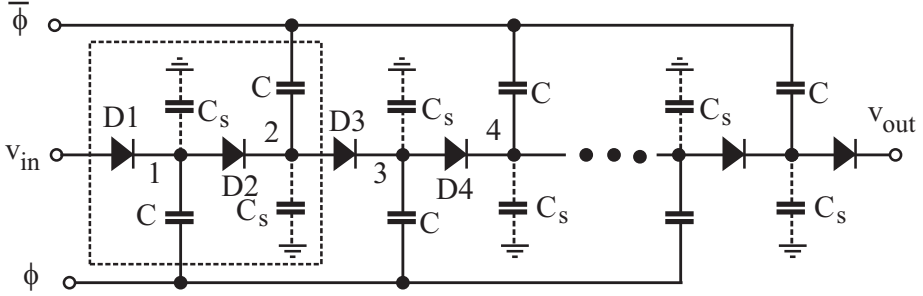


Figure 2.4. Dickson voltage multiplier with diode switches [21].

Dickson voltage multipliers can also be implemented using MOSFET diodes, as shown in Fig.2.5. pMOS Dickson voltage multipliers can also be constructed in a similar way. The advantage of these configurations is their full compatibility with standard CMOS technologies with a main drawback of the voltage loss across the MOSFET devices of at least one threshold voltage. This is accompanied with a low power efficiency, especially when the amplitude of the input voltage is low.

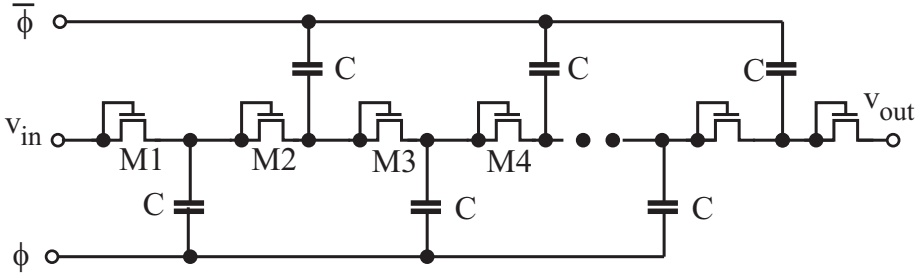


Figure 2.5. Dickson voltage multiplier with nMOS diodes.

The preceding Dickson voltage multiplier with MOSFET diodes suffers from the drawback of the voltage loss of at least one threshold voltage across the MOSFETs. The observation that the voltage drop across of the drain and source of a MOSFET is low if the device is operated in the triode region suggests that the voltage loss of MOSFET diodes can be minimized by connecting a MOSFET working in the triode in parallel with each of the MOSFET diodes, as shown in Fig.2.6 [22]. We term this voltage multiplier Dickson voltage multiplier with static charge transfer switches. The operation of this voltage

multiplier is depicted as follows : When $\phi = 0$, V_1 is initially zero and transistor M1A is on. C_1 is charged by the input voltage. Note that without transistor M1B, the maximum voltage of V_1 will only reach $V_m - V_T$, where V_m is the amplitude of V_{in} and V_T is the threshold voltage of MOSFETs. Since M2A is off, the gate voltage of M1B is at V_{DD} and M1B is in the triode. As a result, $V_{1,max} = V_m - V_{ds1} \approx V_m$. The drawback of the voltage loss of Dickson voltage multipliers is therefore removed. It was demonstrated in [22] that with $v_{in} = 1.5V$ and $I_{out} = 10\mu A$, the output voltage of a 4-stage Dickson voltage multiplier with static charge transfer switches is approximately 4 V. The output voltage of a corresponding conventional Dickson voltage multiplier is only 2 V.

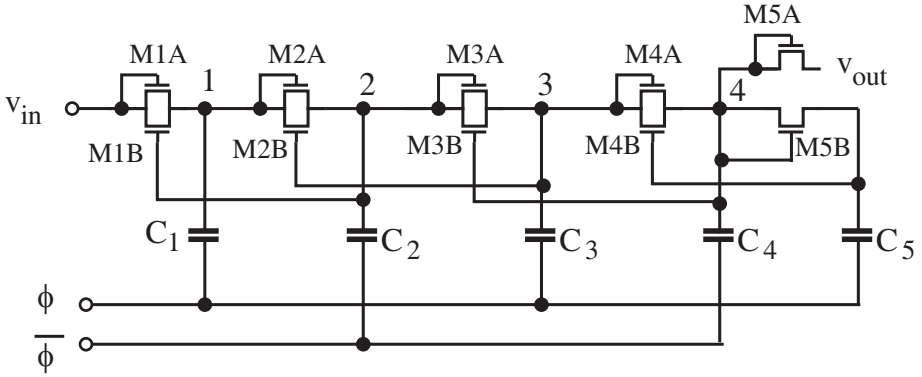


Figure 2.6. Dickson voltage multiplier with static charge transfer switches [22].

San *et al.* proposed bootstrapped gate transfer switches to replace MOSFET diodes of Dickson voltage multiplier, as shown in Fig.2.7 [23]. For each transistor, there are five additional transistors $M_{1a,...,5a}$ and one capacitor C_a are added. When $\phi = 1$, $M_{1a,3a,5a}$ are ON while $M_{2a,4a}$ are OFF. As a result, $V_{B,C} = 0$, $V_A = V_m$, and C_a is charged to V_m . In the following phase where $\phi = 0$, $M_{1a,3a,5a}$ are OFF and $M_{2a,4a}$ are ON. The voltage of the capacitor C_a is applied between the gate and drain of M_2 . For MOSFETs in the triode, $V_{DS} \leq V_{GS} - V_T$ must be satisfied. Referring to Fig.2.7(b), re-write the preceding condition for the MOSFET in the triode

$$V_D - V_S \geq V_D - V_b - V_S - V_T, \quad (2.13)$$

where V_b is the voltage applied between the gate and the drain of the MOSFET. It follows that $V_b - V_T > 0$. It becomes evident that if $V_b > V_T$, M_2 will be in the triode region and V_{DS2} will be small. It was shown in [23] that the output voltage of a 4-stage Dickson voltage multiplier with bootstrapped gate

transfer switches, $C_{1-4} = 15 \text{ pF}$, $C_{out} = 30 \text{ pF}$, $f = 5 \text{ MHz}$, and $V_m = 2 \text{ V}$, is 9 V approximately. The output voltage is only 4 V approximately with static charge transfer switches. The power conversion efficiency is increased from 40% approximately with static charge transfer switches to above 90% with bootstrapped gate transfer switches.

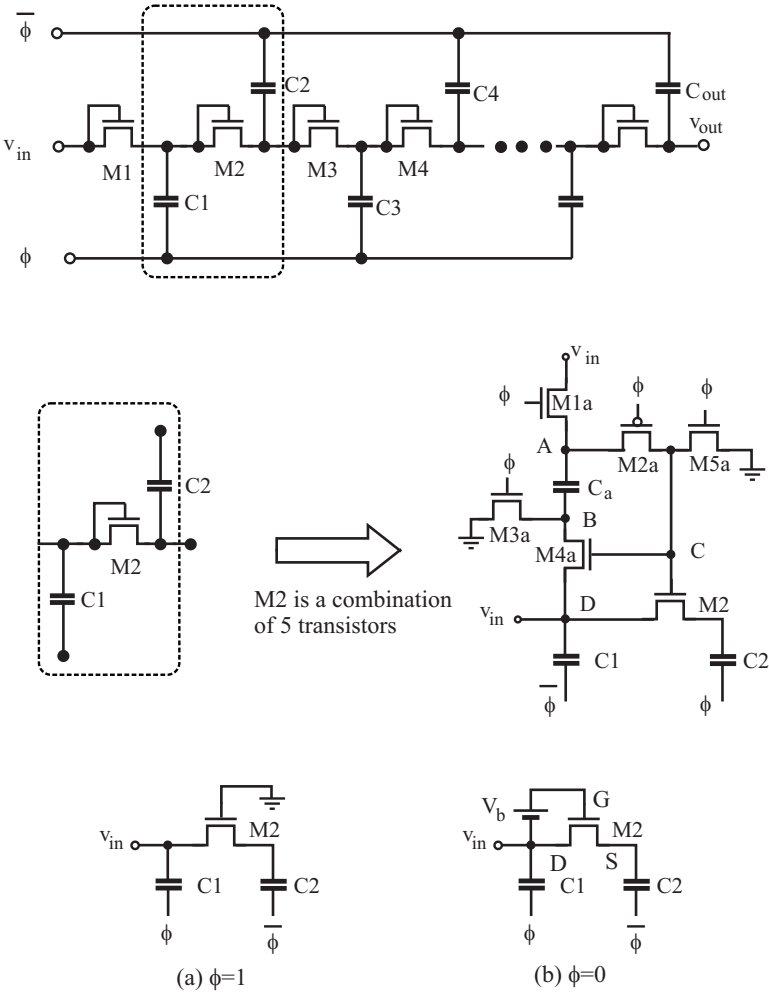


Figure 2.7. Dickson voltage multiplier with bootstrapped gate transfer switches [23].

2.2.4 Modified Dickson Voltage Multipliers

Dickson voltage multiplier requires non-overlapping clock signals ϕ and $\bar{\phi}$. For power telemetry, only one RF signal is available. Dickson voltage multiplier therefore can not be used directly. The fact that the clocking signal

ϕ and $\bar{\phi}$ are applied to every coupling node of Dickson voltage multiplier suggests that if $\bar{\phi}$ and v_{in} terminals are grounded and the RF input is connected to ϕ terminal, as shown in Fig.2.8, each section, as highlighted in the figure, becomes a voltage doubler. This configuration is termed modified Dickson voltage multiplier, in distinction from the original Dickson voltage multiplier studied earlier. Because the input signal is coupled to every other node of the diode chain, the effect of the stray capacitance is suppressed effectively. Clearly if a fully differential input is available, v_{in+} and v_{in-} can be coupled to $C_{1,3,5,\dots}$ and $C_{2,4,6,\dots}$ to further improve the performance.

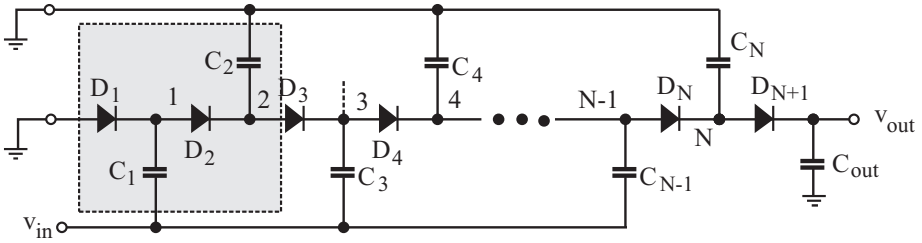


Figure 2.8. Modified Dickson voltage multiplier with diode switches.

The schematic of modified Dickson voltage multipliers with nMOS-diodes is shown in Fig.2.9 and that with pMOS-diode is shown in Fig.2.10. Because the voltage drop across the drain and source of the MOSFETs is at least one threshold voltage, the efficiency of this voltage multiplier is lower as compared with that of its Schottky-diode counterpart. To overcome this drawback, native nMOS transistors whose threshold voltage is approximately zero have been used [24, 25]. The main drawback is that native MOS structure is not generally supported. Also, the large channel resistance of native MOSFETs deteriorates the performance.

2.2.5 Mandal-Sarpeshkar Voltage Multiplier

To overcome the drawback of modified Dickson voltage multiplier with MOSFET-diodes, Mandal and Sarpeshkar proposed a low-power high power efficiency voltage multiplier with its configuration shown in Fig.2.11 [26]. It is ready to verify that once a load is connected between nodes 1 and 2, the current flowing through the load is always in the same direction. A key advantage of this voltage multiplier is the low voltage drop across switching MOSFETs. As a result, a large voltage exists at the output of the rectifying cell and is given by $V_{out,max} = V_m - (V_{DS,n} + V_{SD,p})$. The modular configuration of Mandal-Sarpeshkar voltage multiplier offers the flexibility of adjusting the size of each stage to obtain optimal performance.

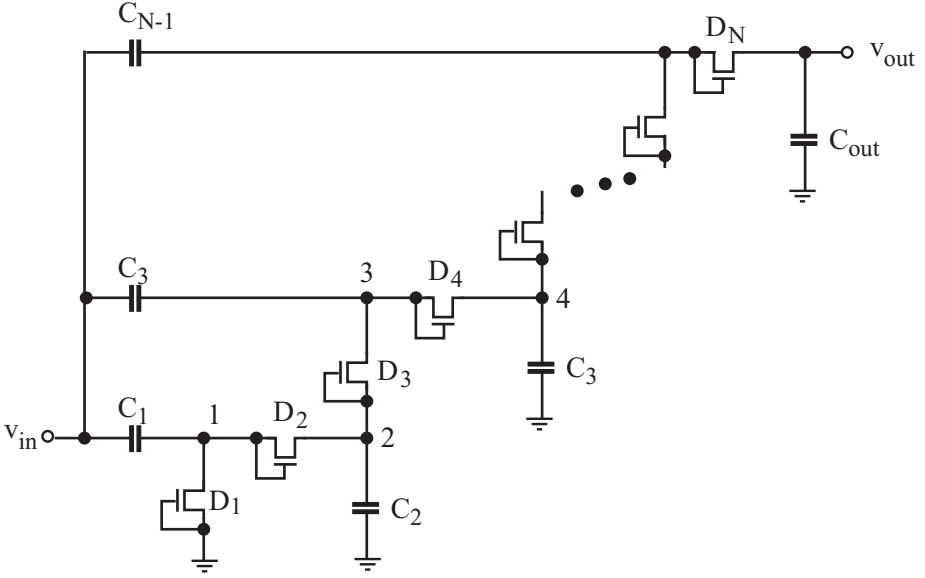


Figure 2.9. Modified Dickson voltage multiplier with nMOS transistors.

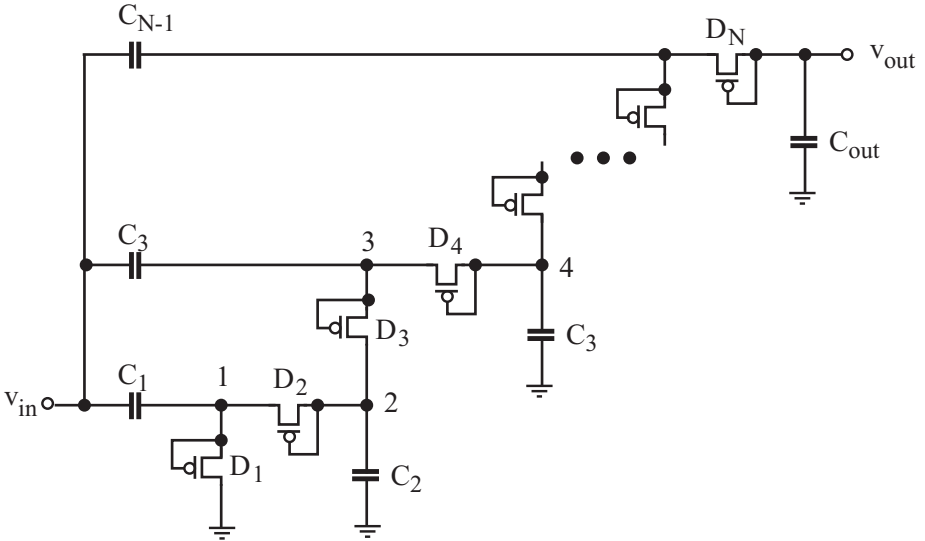


Figure 2.10. Modified Dickson voltage multiplier with pMOS transistors.

2.2.6 Voltage Multiplier with V_T -Cancellation

Umeda *et al.* proposed an elegant mechanism shown in Fig. 2.12 to minimize the voltage drop across MOSFET switches so as to increase the power efficiency of voltage multipliers [27]. For M_1 , because

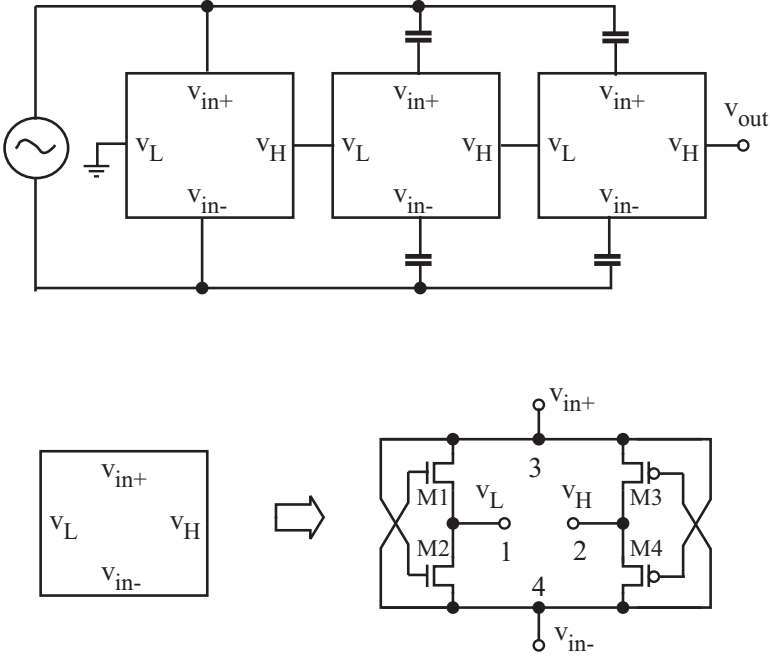


Figure 2.11. Mandal-Sarpeshkar voltage multiplier. If $v_{in+} = V_m$ and $v_{in-} = 0$, $M_{2,3}$ are in the triode (provided that V_m is large enough) and $M_{1,4}$ are off. The voltage drop across $M_{2,3}$ is low [26].

$$V_{G1} = V_m + V_b, \quad (2.14)$$

where V_{G1} is the gate voltage of $M1$, we have

$$V_{out} = 2(V_{GS,max} - V_T) = 2(V_m + V_b - V_T). \quad (2.15)$$

If we set $V_b = V_T$, then $V_{out} = 2V_m$ follows. The power efficiency loss caused by the threshold voltage of MOSFETs is eliminated completely. The required compensation voltage V_b can be obtained in various ways. The approach given in [27] used an external voltage source and a switched capacitor array to generate a set of V_b for all the transistors.

Nakamoto *et al.* proposed an internal threshold voltage generation mechanism to eliminate the voltage drop across MOSFETs without the need for an external voltage source, as shown in Fig.2.13 [28]. The voltage dividers formed by R_1 and M_{1a} , and R_2 and M_{2a} provide the required gate voltages for M_1 and M_2 , respectively. These voltages are held by C_{1a} and C_{2a} , respectively. The values of R_1 and R_2 should be made large to minimize the static

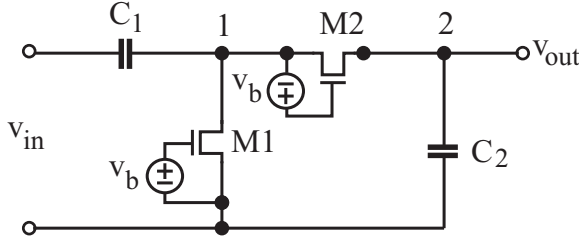


Figure 2.12. Umeda voltage multiplier with external threshold voltage cancellation [27].

power consumption of the compensation transistors $M_{1a,2a}$. Implemented in a $0.35\mu\text{m}$ CMOS technology with an input at 953 MHz, the power efficiency of Nakamoto voltage multiplier at 4-meter distance from a 4 W base station is 36.6% while that of Umeda voltage multiplier is only 16.6%.

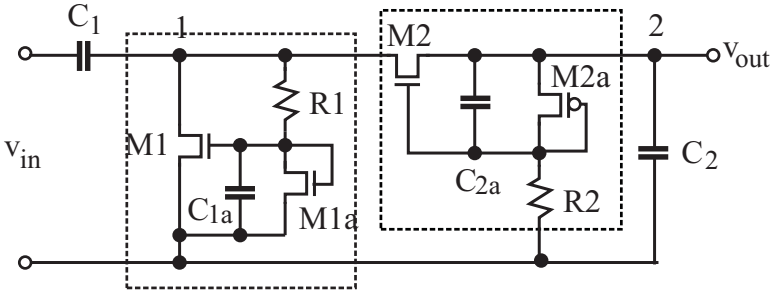


Figure 2.13. Nakamoto voltage multiplier with internal threshold voltage cancellation [28].

2.2.7 Bergeret Voltage Multiplier

Bergeret *et al.* pointed out that an important reason of the low power efficiency of Dickson voltage multipliers including modified Dickson is the propagation of high-frequency signals throughout the circuits [45]. The large area associated with multi-stage voltage multipliers gives rise to a higher substrate loss, subsequently a low power efficiency. Bergeret *et al.* modified the configuration of conventional voltage multiplier by only using a single-stage rectifier to generate a dc voltage. This voltage is then used to power a low-frequency VCO whose outputs, together with the output of the single-stage rectifier, are used to drive a high-efficiency voltage multiplier proposed in [46, 47]. It was demonstrated that this voltage multiplier improved the power efficiency by 14% over the conventional modified Dickson voltage multiplier and the output voltage is 1.5 times that of the modified Dickson voltage multiplier.

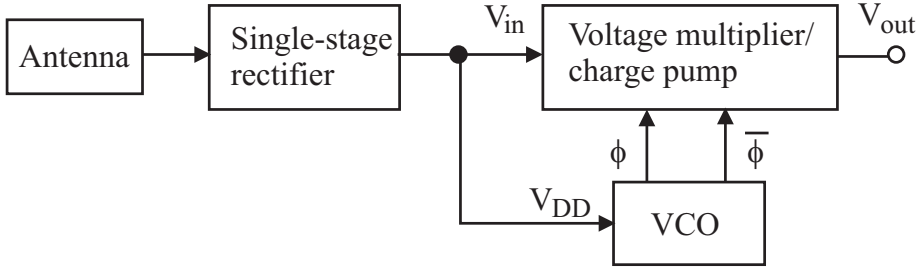


Figure 2.14. Voltage multiplier proposed by Bergeret *et al.* [45].

2.3 Power-Matching and Gain-Boosting Using LC Tanks

Voltage multipliers implemented in standard CMOS technologies suffer from a low efficiency. It was shown in [34] that to boost the power efficiency of the voltage multiplier, the amplitude of the voltage from the antenna of passive wireless microsystems must be maximized. The radiation resistance of the antenna of a passive wireless microsystem is determined by the dimension and type of the antenna. The finite antenna dimension of the passive wireless microsystem limits the voltage across the antenna to be small. As a result, an impedance transformation network that converts the input impedance of the downstream voltage multiplier to the matching impedance of the antenna for the maximum power transmission is inserted between the antenna and the voltage multiplier. In [48], a shunt inductor power-matching network between the antenna and voltage multiplier was employed to resonate out the capacitive part of the input impedance of the voltage multiplier. No attempt, however, was made to match the real part of the input impedance of the multiplier to the radiation resistance of the antenna, leaving the task of power-matching entirely to the voltage multiplier. De Vita and Iannaccone proposed a LC power-matching network that consists of one floating inductor, a shunt capacitor, and a grounded inductor [42]. The grounded inductor is used to resonate out the input capacitance of the downstream voltage multiplier while the LC network provides the matching impedance and voltage gain. The LC power-matching network used by Shameli *et al.* consists of a grounded inductor and a floating capacitor [25].

Power-matching and gain-boosting can be achieved simultaneously by inserting a passive impedance transformation network consisting of a spiral inductor and a metal-insulator-metal (MIM) capacitor between the antenna and the multiplier, as shown in Fig.2.1 [25]. The impedance transformation network provides a matching impedance to the antenna in order to maximize the power transmission from the antenna to the impedance transformation network at the carrier frequency. At the same time, it resonates at the carrier frequency

such that the voltage at the output of the impedance transformation network or the input of the following voltage multiplier is maximized. Since spiral inductors suffer from both a resistive loss mainly due to the ohmic loss of the spiral and a capacitive loss due to the shunt capacitance between the spiral and the substrate, power matching, power loss, and voltage gain of the impedance transformation network must be considered simultaneously in design.

To maximize the amount of the power transferred from the antenna to the impedance transformation network, the impedance transformation network in Fig.2.1 must be designed in such a way that

$$z_{in} = R_a. \quad (2.16)$$

Fig.2.15 shows a simplified schematic of a power-matching and gain-boosting network using a shunt spiral inductor and a series MIM capacitor. To simplify analysis, the MIM capacitor is assumed to be ideal and is represented by an ideal capacitor C . The spiral inductor is modeled using the RLC network with R_s and R_p the series and shunt parasitic resistances, respectively, and C_p the parasitic shunt capacitance. The voltage multiplier is modeled using resistor R_L in parallel with capacitor C_L .

To facilitate analysis, the branch consisting R_s and L_p is replaced with its equivalent parallel $R'_s \sim L'_p$ network shown in Fig.2.15 with R'_s and L'_p given by [49]

$$\begin{aligned} L'_p &= L_p \left[1 + \left(\frac{R_s}{\omega L_p} \right)^2 \right], \\ R'_s &= R_s \left[1 + \left(\frac{\omega L_p}{R_s} \right)^2 \right]. \end{aligned} \quad (2.17)$$

For practical spiral inductors, $\omega L_p \gg R_s$ holds, i.e. the reactance of the inductor is much larger than the resistance of the inductor. As a result, $L'_p \approx L_p$ follows.

It is conveniently to show that the matching condition for the maximum power transfer at node A can be shifted to node B. Moving the impedance matching point from node A to node B will greatly simplify analysis, as to be seen shortly. The impedance matching condition in this case becomes

$$Z_{in} = Z_s^*. \quad (2.18)$$

Let

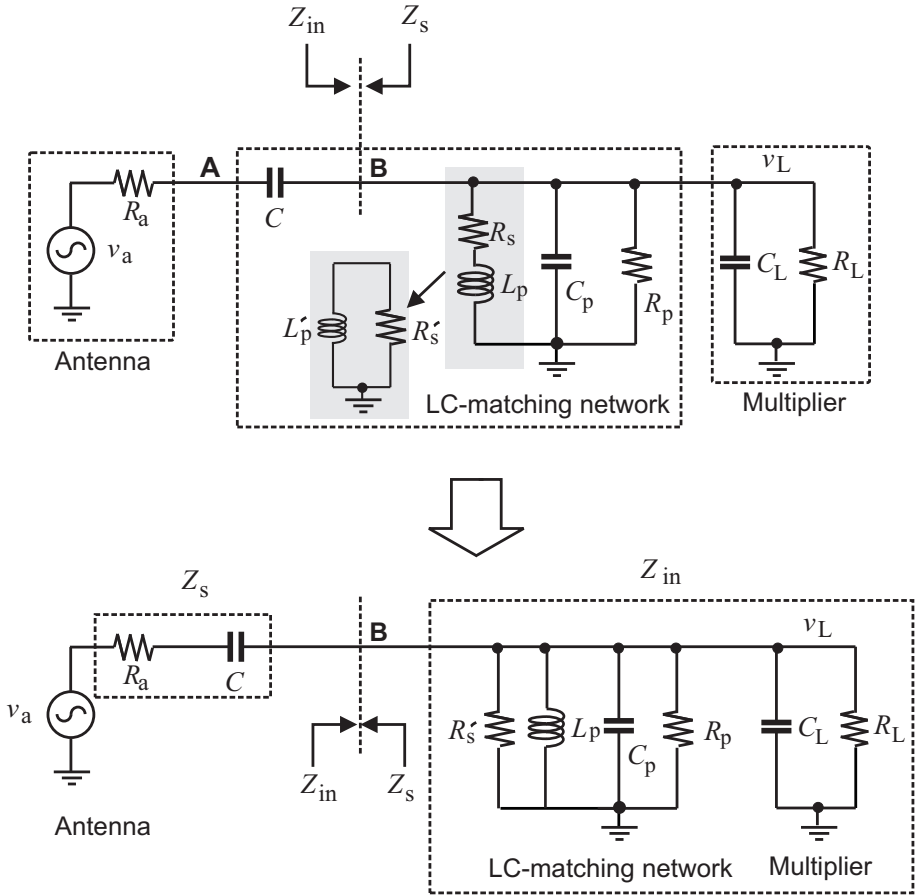


Figure 2.15. Power-matching and gain-boosting network using a shunt spiral inductor and a series MIM capacitor.

$$Z_{in} = R_{in} + jX_{in}, \quad (2.19)$$

and

$$Z_s = R_s + jX_s, \quad (2.20)$$

where R_{in} and X_{in} are the resistance and reactance of the impedance looking into the impedance transformation network, R_s and X_s are the resistance and reactance of the impedance looking into the source network. Submitting these results into (2.18) yields

$$\begin{aligned} R_{in} &= R_s, \\ X_{in} &= -X_s. \end{aligned} \quad (2.21)$$

Since

$$Y_{in} = \frac{1}{Z_{in}} = \frac{R_{in} - jX_{in}}{R_{in}^2 + X_{in}^2}, \quad (2.22)$$

and

$$Y_s = \frac{1}{Z_s} = \frac{R_s - jX_s}{R_s^2 + X_s^2}, \quad (2.23)$$

if $R_{in} = R_s$ and $X_{in} = X_s$, we have

$$Y_L = Y_s^*. \quad (2.24)$$

Eq.(2.24) confirms that impedance matching is the same as admittance matching in maximizing power transfer.

The input impedance Z_{in} is given by

$$\begin{aligned} Z_{in} &\approx R_{eq} || j\omega L_p \\ &= \frac{j\omega R_{eq}^2 L_p + \omega^2 R_{eq} L_p^2}{R_{eq}^2 + (\omega L_p)^2}, \end{aligned} \quad (2.25)$$

where

$$R_{eq} = R'_s || R_p || R_L \quad (2.26)$$

is the total shunt resistance. Note that we have neglected the shunt capacitances in (2.25) to simplify analysis because the gain provided by the impedance transformation network is mainly due to R_{eq} , as to be seen shortly. Matching the impedance at node B yields

$$R_a = \frac{\omega^2 R_{eq} L_p^2}{R_{eq}^2 + (\omega L_p)^2}, \quad (2.27)$$

and

$$\frac{1}{\omega C} = \frac{\omega R_{eq}^2 L_p}{R_{eq}^2 + (\omega L_p)^2}. \quad (2.28)$$

It follows from (2.27) that

$$\frac{R_{eq}}{R_a} = Q_p^2 + 1, \quad (2.29)$$

where

$$Q_p = \frac{R_{eq}}{\omega L_p} \quad (2.30)$$

is the quality factor of the shunt $R \sim L$ network consisting of the spiral inductor and the voltage multiplier with the shunt capacitances neglected. Similarly, one can show from (2.28) that the frequency at which the impedance matching condition is satisfied is given by

$$\omega = \omega_o \sqrt{1 + \frac{1}{Q_p^2}}, \quad (2.31)$$

where

$$\omega_o = \frac{1}{\sqrt{L_p C}} \quad (2.32)$$

is the resonant frequency of the ideal LC impedance transformation network.

Let us now matching the admittance at node B. Because

$$Y_{in} = \frac{1}{R_{eq}} + j \left[\omega C'_p - \frac{1}{\omega L_p} \right], \quad (2.33)$$

and

$$Y_s = \frac{1}{R_a + \frac{1}{j\omega C}} = \frac{\omega^2 C^2 R_a + j\omega C}{1 + (\omega R_a C)^2}, \quad (2.34)$$

where

$$C'_p = C_L + C_p. \quad (2.35)$$

we have

$$\frac{1}{R_{eq}} = \frac{\omega^2 R_a C^2}{1 + (\omega R_a C)^2}, \quad (2.36)$$

and

$$\omega C'_p - \frac{1}{\omega L_p} = -\frac{\omega C}{1 + (\omega R_a C)^2}, \quad (2.37)$$

Solving (2.36) yields

$$\frac{R_{eq}}{R_a} = Q_a^2 + 1, \quad (2.38)$$

where

$$Q_a = \frac{1}{\omega R_a C} \quad (2.39)$$

is the quality factor of $R_a \sim C$ network. Solving (2.37) and noting that $Q_a \gg 1$ yield the frequency at which the admittance matching is satisfied

$$\omega \approx \frac{\omega_p}{\sqrt{1 + \frac{C}{C'_p}}}, \quad (2.40)$$

where

$$\omega_p = \frac{1}{\sqrt{L_p C'_p}} \quad (2.41)$$

is the resonant frequency of the shunt network.

The impedance transformation network is lossy due to the power dissipation of R'_s and R_p . To maximize the amount of the power transferred from the antenna to the multiplier, the power loss of the impedance transformation network must be minimized. Since $\omega L_p \gg R_s$ holds for spiral inductors, we have from (2.17)

$$R'_s \approx \frac{(\omega L_p)^2}{R_s}. \quad (2.42)$$

Further from (2.40) we have

$$(\omega L_p)^2 = \frac{1}{\omega^2 (C + C'_p)^2}. \quad (2.43)$$

Substitute (2.43) into (2.42)

$$R'_s = \frac{1}{R_s \omega^2 C^2 \left(1 + \frac{C'_p}{C}\right)^2}. \quad (2.44)$$

Further from (2.38) with $Q_a \gg 1$, we have

$$R_{eq} R_a = \frac{1}{(\omega C)^2}. \quad (2.45)$$

Making use of (2.45), (2.44) becomes

$$R'_s = \frac{R_{eq} R_a}{R_s \left(1 + \frac{C'_p}{C}\right)^2}. \quad (2.46)$$

Substituting (2.26) into (2.46) yields

$$R'_s = \left[\frac{R_a}{R_s} \left(\frac{C}{C + C'_p} \right) - 1 \right] (R_L || R_p). \quad (2.47)$$

It is seen from (2.47) that C'_p lowers R'_s . This is echoed with an increase in the ohmic loss of the inductor.

The power efficiency of the impedance transformation network is obtained from

$$\eta_I = \frac{P_L}{P_{in}}, \quad (2.48)$$

where P_L is the amount of power delivered to the voltage multiplier and P_{in} is the amount of power available at the input of the impedance transformation network. By assuming that there is no loss in capacitor C , P_{in} is the amount of power at node B, i.e. the input port of the shunt network consisting of the spiral inductor and the voltage multiplier.

$$P_{in} = \frac{V_L^2}{R_{eq}}, \quad (2.49)$$

and

$$P_L = \frac{V_L^2}{R_L}. \quad (2.50)$$

It follows that

$$\eta_I = \frac{P_L}{P_{in}} = \frac{R_{eq}}{R_L}. \quad (2.51)$$

Since

$$\frac{1}{R_{eq}} = \frac{1}{R'_s} + \frac{1}{R_p} + \frac{1}{R_L}, \quad (2.52)$$

making use of (2.47), we can write (2.52) as

$$\frac{1}{R_{eq}} = \left(\frac{1}{R_p} + \frac{1}{R_L} \right) \frac{\frac{R_a}{R_s} \left(\frac{C}{C + C'_p} \right)^2}{\frac{R_a}{R_s} \left(\frac{C}{C + C'_p} \right)^2 - 1}. \quad (2.53)$$

Substituting (2.53) into (2.48) yields

$$\eta_I = \frac{1 - \frac{R_s}{R_a} \left(1 + \frac{C'_p}{C} \right)}{1 + \frac{R_L}{R_p}}. \quad (2.54)$$

Since $\frac{R_L}{R_p} \ll 1$ typically holds, making use of

$$\frac{1}{1+x} \approx 1 - x, \quad (2.55)$$

when $|x| \ll 1$, we can write (2.54) as

$$\eta_I \approx 1 - \frac{R_s}{R_a} \left(1 + \frac{C'_p}{C} \right) - \frac{R_L}{R_p}. \quad (2.56)$$

It is evident from (2.56) that the power efficiency of the impedance transformation network is less than 100% due to the non-zero parasitic series resistance R_s , the finite parasitic shunt resistance R_p , and the shunt capacitance C'_p . To increase η_I , R_s and C'_p should be minimized while R_p should be maximized.

As pointed out earlier, the overall power efficiency of the power harvester can be improved if a large voltage gain is provided by the impedance transformation network. The power delivered to the impedance transformation network is computed from

$$P_L = \frac{V_L^2}{R_{eq}} = \frac{A_v^2 V_a^2}{R_{eq}}, \quad (2.57)$$

where

$$A_v = \frac{V_L}{V_a} \quad (2.58)$$

is the voltage gain of the impedance transformation network. The maximum power delivered to the impedance transformation network is given by

$$P_{L,max} = \frac{V_a^2}{4R_a}. \quad (2.59)$$

Equating (2.57) and (2.59) yields the optimal voltage gain of the impedance transformation network at which the maximum power transfer takes place

$$A_v = \frac{1}{2} \sqrt{\frac{R_{eq}}{R_a}}. \quad (2.60)$$

Substituting (2.26) and (2.47) into (2.60), we arrive at

$$A_v = \frac{1}{2} \sqrt{\frac{R_p || R_L}{R_a} \left[1 - \frac{R_s}{R_a} \left(1 + \frac{C'_p}{C} \right) \right]}. \quad (2.61)$$

We comment on the preceding development :

- If $R_L > R_p$, $R_p || R_L$ will be dominated by R_p . Increasing R_L beyond R_p will no longer improve $R_p || R_L$ subsequently the voltage gain.
- To improve the voltage gain of the impedance transformation network, R_s must be made much smaller than R_a . Minimizing the resistive loss of the spiral inductor is critical.

- Parasitic shunt capacitances of the spiral inductor C'_p increases the effect of conductive loss by a factor of $\left(1 + \frac{C'_p}{C}\right)$. To minimize its effect, $C'_p \ll C$ is essential.
- The power efficiency of the impedance transformation network can be further analyzed by neglecting the shunt capacitances C_p and C_L for simplicity. The maximum power delivered to the impedance transformation network is given by

$$P_{in} = \frac{V_a^2}{4R_a} \quad (2.62)$$

and the current flowing from the antenna to the impedance transformation network at the maximum power transfer is given by

$$I_{in} = \frac{V_a}{2R_a}. \quad (2.63)$$

The power delivered to the voltage multiplier is obtained from

$$P_L = R_L I_L^2. \quad (2.64)$$

Since

$$\begin{aligned} I_L &= \left| \frac{R'_p || (j\omega L_p)}{R'_p || (j\omega L_p) + R_L} \right| I_{in} \\ &= \frac{R'_p}{\sqrt{Q_L^2 + \left(1 + \frac{R_L}{R'_p}\right)^2}}, \end{aligned} \quad (2.65)$$

where $R'_p = R_p || R'_s$ and

$$Q_L = \frac{R_L}{\omega L_p}. \quad (2.66)$$

Note that since R_L is typically smaller than R_p and R'_s , $R_L \approx R_{eq}$ holds. As result, $Q_L \approx Q_p$. The power efficiency of the impedance transformation network is obtained from

$$\begin{aligned}
\eta_I &= \frac{P_L}{P_{in}} \\
&= \frac{R_L}{R_a} \left[\frac{1}{Q_L^2 + \left(1 + \frac{R_L}{R_p}\right)^2} \right].
\end{aligned} \tag{2.67}$$

When R_L is small, i.e. $R_L \ll \omega L_p$ and $R_L \ll R_p$, we have

$$\eta_I \approx \frac{R_L}{R_a}. \tag{2.68}$$

The power efficiency of the LC impedance transformation network in this case is directly proportional to R_L . It is interesting to note from (2.56) that

$$\begin{aligned}
\eta_I &\approx 1 - \frac{R_s}{R_a} \left(1 + \frac{C'_p}{C}\right) - \frac{R_L}{R_p} \\
&= \frac{R_L}{R_a} \left[\frac{R_a}{R_L} - \frac{R_s}{R_L} \left(1 + \frac{C'_p}{C}\right) - \frac{R_a}{R_p} \right].
\end{aligned} \tag{2.69}$$

Since $R_a \ll R_L$, R_p and $R_s \ll R_L$ typically hold, (2.69) is simplified to

$$\eta_I \approx \frac{R_L}{R_a}. \tag{2.70}$$

When R_L is large, i.e. $R_L \gg \omega L_p$, we have

$$\eta_I \approx \frac{(\omega L_p)^2}{R_a R_L}. \tag{2.71}$$

The power efficiency in this case is inversely proportional to R_L . Fig.2.16 plots η_I at 2.4 GHz with an ideal inductor of inductance $L_p = 10.6$ nH and $R_a = 50\Omega$. As can be seen that η_I rises with R_L approximately linearly when R_L is small and decreases with R_L when R_L is large. An optimal R_L thus exists.

To quantify the dependence of the output voltage and power efficiency of the LC impedance transformation network on the resistive load, the power harvester with a LC impedance transformation network is analyzed. The voltage

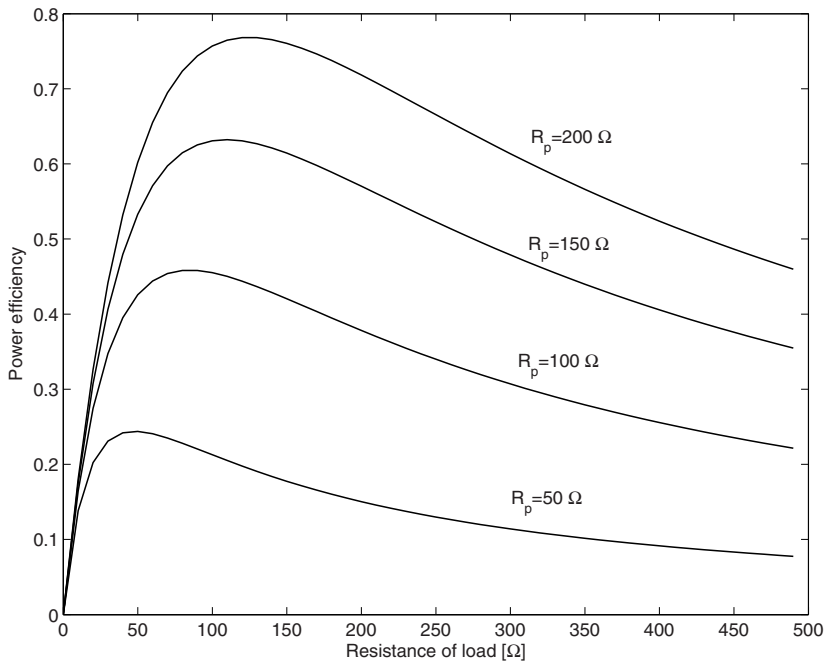


Figure 2.16. Power efficiency of LC impedance transformation network.

multiplier is modeled as an ideal resistor for simplicity. The inductor is an octagonal spiral inductor of 5.5 turns with its outer radius $222 \mu\text{m}$ and spiral width $15 \mu\text{m}$. Fig.2.17 shows the dependence of the output voltage and power efficiency of the LC impedance transformation network on the resistance of the load. It is seen that the output voltage increases with the load resistance in the nonlinear fashion that follows a square-root profile. The power efficiency arises with the load resistance when the load resistance is low and levels off when the load resistance becomes large. Also, the profile of the power efficiency agrees with that given in Fig.2.16. A trade-off between the power efficiency of the impedance transformation network and its output voltage, which will affect the power efficiency of the downstream voltage multiplier, is needed.

2.4 Power-Matching and Gain-Boosting Using Transformers

A step-up transformer is characterized by a small voltage and a large current in the primary winding and a large voltage and a small current in the secondary winding. The relation between the current and voltage of the primary winding

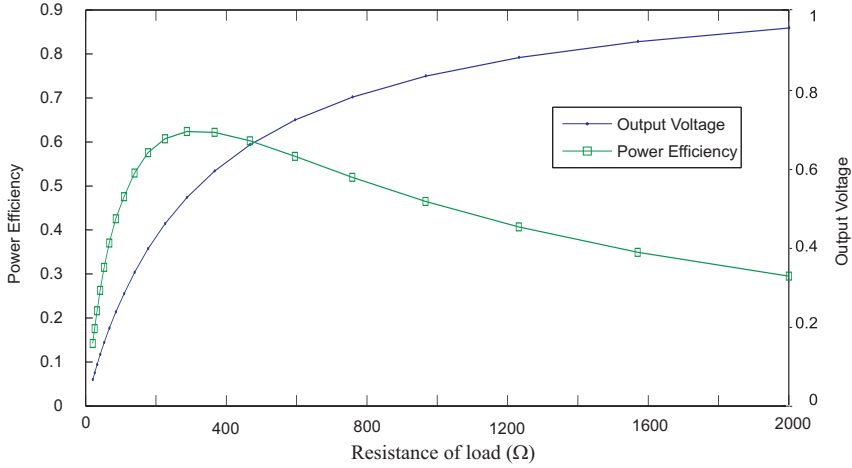


Figure 2.17. Dependence of the power efficiency of LC impedance transformation network on the resistance of the load. The spiral inductor is a 5.5-turn octagonal spiral implemented in TSMC-0.18 μm CMOS technology with its outer radius 222 μm and spiral width 15 μm . The input voltage is a 2.4-GHz 1-V sinusoid.

and those of the secondary winding of a lossless step-up transformer are given by

$$\frac{I_1}{I_2} = \frac{n_2}{n_1} \quad (2.72)$$

and

$$\frac{V_1}{V_2} = \frac{n_1}{n_2}, \quad (2.73)$$

where I_1, I_2 and V_1, V_2 are the current and voltage of the primary winding and secondary winding, respectively, n_1 and n_2 are the turns of the primary winding and that of the secondary winding, respectively. With $n_2 > n_1$, we have $I_2 < I_1$ and $V_2 > V_1$. By employing a step-up transformer, the same power can be delivered from the primary winding to the secondary winding with a higher voltage at the secondary winding. It is evident that by letting n large, the voltage of the secondary winding of the transformer will be larger than that of its primary winding while the current of the secondary winding will be smaller than that of its primary winding. The loss of the primary winding will therefore be dominated by its ohmic loss due to its large current while the loss of the secondary winding will be dominated by its spiral-substrate loss due to its large number of turns. These observations are critical as they

reveal that the series loss of a step-up transformer with a large turn ratio is dominated by that of the primary winding while its shunt loss is dominated by that of the secondary winding. Soltani and Yuan pointed out that since the primary winding has a fewer turns, its series loss can be effectively reduced by increasing the width of the spiral of the primary winding. The width of the primary winding can be set to such a value that both windings will have approximately the same silicon area. The shunt loss of the secondary winding, on the other hand, can be lowered effectively by reducing the width of the spiral of the secondary winding. Note that since the current of the secondary winding is small, reducing the width of the spiral of the secondary winding will not overly increase its resistive loss [29].

Fig. 2.18 shows the equivalent circuit of a power harvester with a step-up transformer. The transformer is represented using the narrow-band model given in [50, 51]. Capacitors C_1 and C_2 are used to resonate out the self-inductance of the primary winding and that of the secondary winding, respectively.

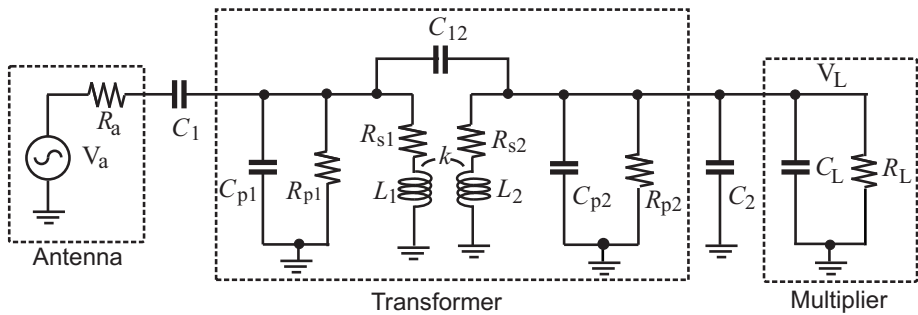


Figure 2.18. Equivalent circuit of a power harvester with a step-up transformer power-matching and gain-boosting network. C_{p1} and R_{p1} are the parasitic shunt capacitance and shunt resistance of the primary winding, respectively, R_{s1} is the parasitic series resistance of the primary winding, L_1 is the inductance of the primary winding, C_{p2} and R_{p2} are the parasitic shunt capacitance and shunt resistance of the secondary winding, respectively, R_{s2} is the parasitic series resistance of the secondary winding, L_2 is the inductance of the secondary winding, C_1 and C_2 are the series capacitance at the primary winding and the shunt capacitance at the secondary winding, respectively. They are used form LC resonant networks with L_1 and L_2 , respectively.

Because the voltage of the primary winding is small, the resonance of the primary winding will only create a small voltage gain from the antenna to the primary winding. The large current of the primary winding demands that the cross-sectional area of the spiral of the primary winding be large. This can be achieved by using multiple metal layers that are connected using vias for the primary winding. Further, since the primary winding has a fewer turns, its spiral can be implemented using lower metal layers without encountering a significant substrate loss. Of course, this arrangement is technology-dependent.

The preceding arrangement is for TSMC-0.18 μm CMOS technology used to fabricate the power harvester with a step-up transformer. The objective of any configuration of the primary winding is to minimize the resistive loss of the winding. The resonance at the secondary winding, on the other hand, is significant due to its large self-inductance needed to produce a large voltage gain.

To analyze the voltage gain obtained from the resonance of the secondary winding, we follow the approach used for analysis of the power harvester with a LC impedance transformation network given in Section 2.3, specifically L_2 is separated from the rest of the transformer, as shown in Fig.2.19 . A Thévenin equivalent circuit is used to represent the overall effect of the matching network excluding L_2 and C_2 . To further simplify analysis, we use

$$C'_2 = C_2 + C_{p2} + C_L \quad (2.74)$$

and

$$R'_2 = R_{p2} || R_L \quad (2.75)$$

to account for all shunt capacitances and resistances at the secondary winding, respectively. Note that the simplified circuit has the same topology as that of Fig.2.15. The approach used for the analysis of the circuit in Fig.2.15 can thus be followed to analyze the circuit in Fig.2.19.

Thévenin voltage V_T is obtained by open-circuiting the secondary winding and deriving the voltage across the series resistance R_{s2} and mutual inductance M due to V_a with L_1 and C_1 resonated out, i.e.

$$j\omega L_1 + \frac{1}{j\omega C} = 0, \quad (2.76)$$

$$V_T = \frac{j\omega M}{R_a + R_{s1}} V_a, \quad (2.77)$$

where

$$M = K \sqrt{L_1 L_2} \quad (2.78)$$

is the mutual inductance and K the coupling coefficient of the transformer. Thévenin impedance is obtained by short-circuiting V_a and applying a test voltage source over R_{s2} and M with L_1 and C_1 resonated out

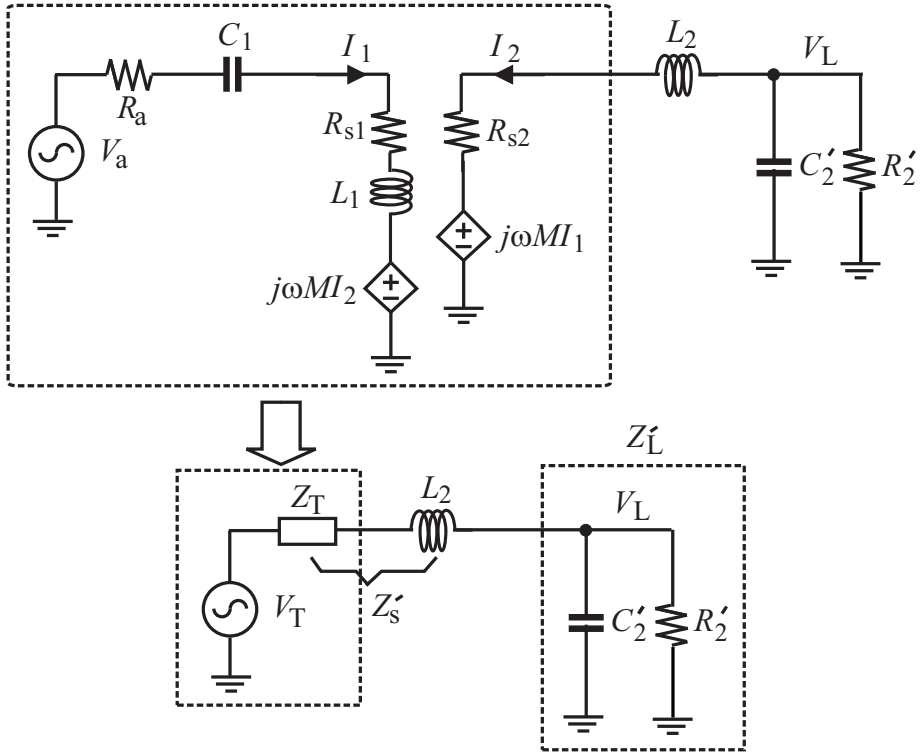


Figure 2.19. Thévenin equivalent circuit of step-up transformer power-matching and gain-boosting network.

$$Z_T = R_{s2} + \frac{(\omega M)^2}{R_a + R_{s1}}. \quad (2.79)$$

It is seen from (2.79) that Thévenin impedance is purely resistive. Also, it has two components: the series resistance of the secondary winding and the resistance of the primary winding referred to the secondary winding.

To find out the voltage gain from V_T to V_L , we notice that for the maximum power transfer,

$$Z'_L = (Z'_s)^* \quad (2.80)$$

is required. Since

$$Z'_L = R'_2 \parallel \frac{1}{j\omega C'_2} \quad (2.81)$$

and

$$Z'_s = Z_T + j\omega L_2, \quad (2.82)$$

the magnitude of the voltage gain is obtained from

$$\left| \frac{V_L}{V_T} \right| = \left| \frac{Z'_L}{Z'_L + Z'_s} \right| = \frac{1}{2} \sqrt{1 + \left(\frac{\omega L_2}{Z_T} \right)^2}. \quad (2.83)$$

Substituting (2.79) into (2.83) yields

$$\left| \frac{V_L}{V_T} \right| = \frac{1}{2} \sqrt{1 + \left[\frac{R_{s2}}{\omega L_2} + \frac{\omega^2 M^2}{\omega L_2 (R_a + R_{s1})} \right]^{-2}}. \quad (2.84)$$

The quality factor of the secondary winding satisfies

$$Q_2 = \frac{\omega L_2}{R_{s2}} \gg 1 \quad (2.85)$$

and

$$Q_1 = \frac{\omega L_1}{R_a + R_{s1}} \quad (2.86)$$

is the equivalent quality factor of the primary winding [52]. Making use of (2.85) and (2.86), we can write (2.84) as

$$\left| \frac{V_L}{V_T} \right| = \frac{1}{2} \sqrt{1 + \left(\frac{Q_2}{k^2 Q_1 Q_2 + 1} \right)^2}. \quad (2.87)$$

It is seen from (2.87) that a large voltage gain of the step-up transformer matching network can be obtained by (i) boosting the mutual inductance M , (ii) lowering the series resistance of the primary winding, (iii) lowering the series resistance of the secondary winding, and (iv) increasing the self inductance of the secondary winding. There are two ways to increase the mutual inductance M : increase the coupling coefficient or increase the turn ratio. The former can only be achieved by using a stacked configuration while the latter requires a large number of the turns of the secondary winding. The series resistance of the primary winding can be lowered effectively by increasing the spiral width of the primary winding and by using multiple metal layers connected together

using vias. The self-inductance of the secondary winding and the coupling coefficient can be increased simultaneously by reducing the width of the spiral of the secondary winding so that more turns can be accommodated for a given silicon area. This, however, is at the cost of the increased series resistance of the secondary winding. Fortunately, the current of the secondary winding of the step-up transformer is small as compared with that of the primary winding, its resistive winding loss is not of a critical concern.

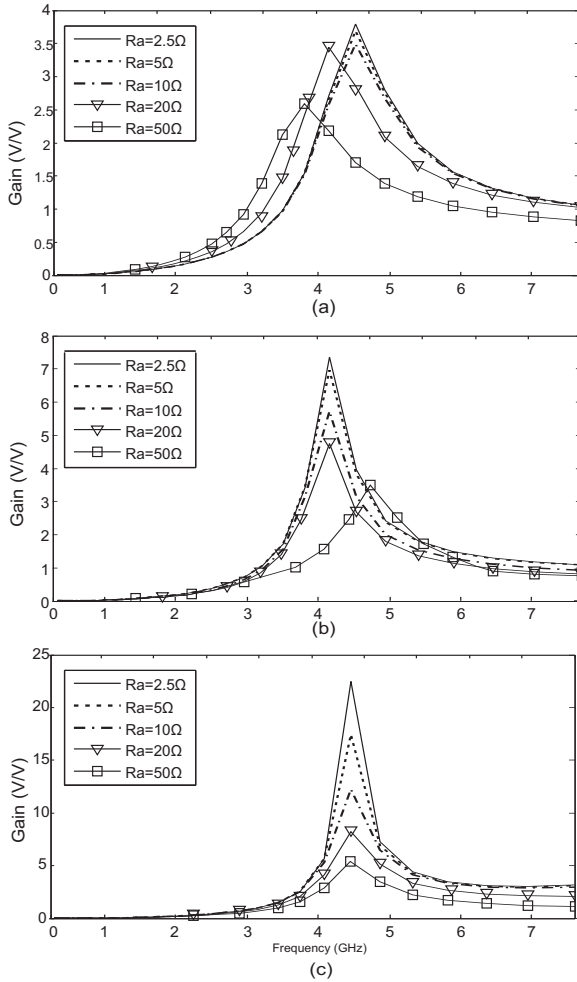


Figure 2.20. Simulated voltage gain of power-matching and gain-boosting networks for different values of radiation resistance. (a) LC matching network (spiral width = $5\mu m$). (b) LC matching network with reduced spiral width (spiral width = $1.5\mu m$). (c) Step-up transformer matching network (spiral width in primary winding : $5\mu m$, spiral width in secondary winding : $1.5\mu m$). The load resistance is fixed at $R_L = 40k\Omega$. The power harvesters are implemented in TSMC-0.18 μm CMOS technology (Copyright (c) IEEE).

To find out the overall voltage gain, i.e. the voltage gain from the antenna to the output of the impedance transformation network, we make use of Fig.2.19. Since this circuit itself is a LC impedance transformation network, we can use (2.60) to write the voltage gain from V_T to V_L

$$A_v = \frac{V_L}{V_T} = \frac{1}{2} \sqrt{\frac{R'_2}{Z_T}}. \quad (2.88)$$

Note that Z_T is purely resistive. Substituting R'_2 and Z_T with their values, the overall voltage gain of the transformer matching network is obtained

$$\begin{aligned} A_v &= \frac{1}{2} \left(\frac{\omega M}{R_a + R_{s1}} \right) \sqrt{\frac{R'_2}{Z_T}} \\ &= \frac{1}{2} \sqrt{\frac{R_L || R_{p2}}{\frac{R_{s2}}{A_{ind}^2} + R_a + R_{s1}}}, \end{aligned} \quad (2.89)$$

where

$$A_{ind} = \frac{\omega M I_1}{V_a} = \frac{\omega M}{R_a + R_{s1}} \quad (2.90)$$

is the voltage gain from V_a to V_T . Let us now comment on the preceding development :

The effect of the series resistance of the secondary winding is scaled down by A_{ind}^2 . This finding is significant as it allows us to use more turns with reduced spiral width in the secondary winding to boost the voltage gain without a large shunt loss. To increase A_{ind} , the mutual inductance of the transformer M must be increased and R_{s1} must be decreased. As mentioned earlier that there are two ways to increase M : increase the coupling coefficient or increase the turn ratio. The former can be achieved by using a stacked configuration while the latter requires more turns of the secondary winding.

The series resistance of the primary winding R_{s1} is low due to the small number of the turns of the primary winding and the use of multi-layer spirals connected using vias, the effect of the series loss of the primary winding is small.

The step-up transformer matching technique is particularly attractive for antennas with a low R_a . Since in (2.89) all terms except R_a are small, reducing R_a will significantly increase A_v . Reducing the source impedance below $R_{s1} + \frac{R_{s2}}{A_{ind}^2}$ will not contribute further to the voltage gain.

When R_a is large, from (2.90) A_{ind} will be small. In this case, a large voltage gain can be achieved by reducing the spiral width of the secondary. This is because reducing the spiral width will reduce the winding area subsequently the shunt capacitance of the secondary winding [5]. The series loss of the secondary winding, however, is also increased. This will in turn lower the overall voltage gain. When R_a is significantly larger than $R_{s1} + \frac{R_{s2}}{A_{ind}^2}$, it will dominate the denominator of (2.89). An increase in R_{s2} in this case will have a less impact on the overall voltage gain. Decreasing the spiral width of the secondary winding is beneficial to the overall gain when the radiation resistance is large. It should be noted that an additional gain obtained is due to the resonance of the secondary winding with C'_{p2} as quantified by (2.87).

Although the step-up transformer impedance transformation network should be designed in such a way that it resonates precisely at the carrier frequency, parameter spreading from process variation will cause the resonant frequency of the impedance transformation network to deviate from the carrier frequency. It is therefore highly desirable that the resonant frequency of impedance transformation network can be tuned. The resonant frequency of the LC impedance transformation network can be tuned by placing a variable capacitor C_v in parallel with the voltage multiplier, as shown in Fig.2.21. Rewriting (2.40)

$$\omega_o \approx \frac{1}{\sqrt{L_p(C + C'_p)}}, \quad (2.91)$$

we observe that both C and C'_p can be adjusted to tune the resonant frequency of the LC impedance transformation network. Varying C will affect the voltage gain of the impedance transformation network. This is clearly undesirable. On the other hand, it is observed from (2.61) that the dependence of the voltage gain on the shunt capacitance C'_p in Fig.2.15 is governed by a much weaker function. This observation reveals that the variable capacitor required to tune the resonant frequency of the LC impedance transformation network should be placed in parallel with C'_p , as shown in Fig.2.21.

Similarly, the resonant frequency of the transformer impedance transformation network can be tuned by replacing C_1 and C_2 in Fig.2.18 with variable capacitors C_{v1} and C_{v2} respectively, as shown in Fig.2.22.

To tune the resonant frequency of the step-up transformer impedance transformation network of Fig.2.22, both capacitors C_{v1} and C_{v2} have to be adjusted. Lowering the resonant frequency using capacitors will result in a roll-off in the voltage gain. A key advantage of using a step-up transformer instead of an inductor for power-matching and gain-boosting is the reduced effect of the resistive loss of the secondary winding, as described by (2.89). By reducing the resonant frequency using capacitors, the mutual inductance M will remain unchanged while the circuit will operate at a lower frequency. This will result

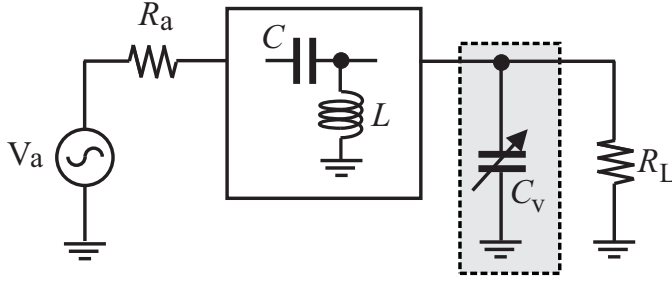


Figure 2.21. Frequency tuning in power-matching and gain-boosting network using a LC network.

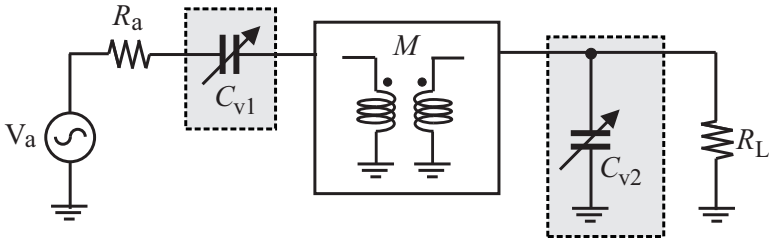


Figure 2.22. Frequency tuning in power-matching and gain-boosting using a step-up transformer network.

in a reduction in A_{ind} , as expected from (2.90). Fig.2.23(a) shows the gain roll-off caused by tuning down the resonant frequency of the step-up transformer. Fig.2.23(b) shows the dependence of the resonant frequency and voltage gain on C_{v2} . As can be seen that the voltage gain drops from 5.0 at 3.7 GHz to 4.35 at 2 GHz.

To validate the preceding findings, a step-up transformer impedance matching and gain boosting network is designed in TSMC-0.18 μm 1.8V 6-metal CMOS technology with thick metal options. The primary winding has 1.5 turns and is implemented using metal layers 3 to 5 with identical thickness of 1 μm . These metal layers are connected using vias to minimize the winding resistance. The secondary winding has 5.5 turns and is implemented using the top metal layer with thickness 2.3 μm . The width of the spiral in the primary winding is 8 μm and that in the secondary winding is 1.5 μm . For the purpose of comparison, a LC matching network with the same loading condition is also implemented. The inductor of the LC matching network has a 4.5-turn spiral implemented using the top metal layer of width 5 μm . On-wafer probing is conducted using a Cascade Microtech RF-1 probe station with four MH5 positioners, RF and DC probes. Since the design is to be tested using an off-chip RF source, the choice of the source impedance is set to 50 Ω . To measure the output voltage, the power-matching circuits are connected to dual-half-wave

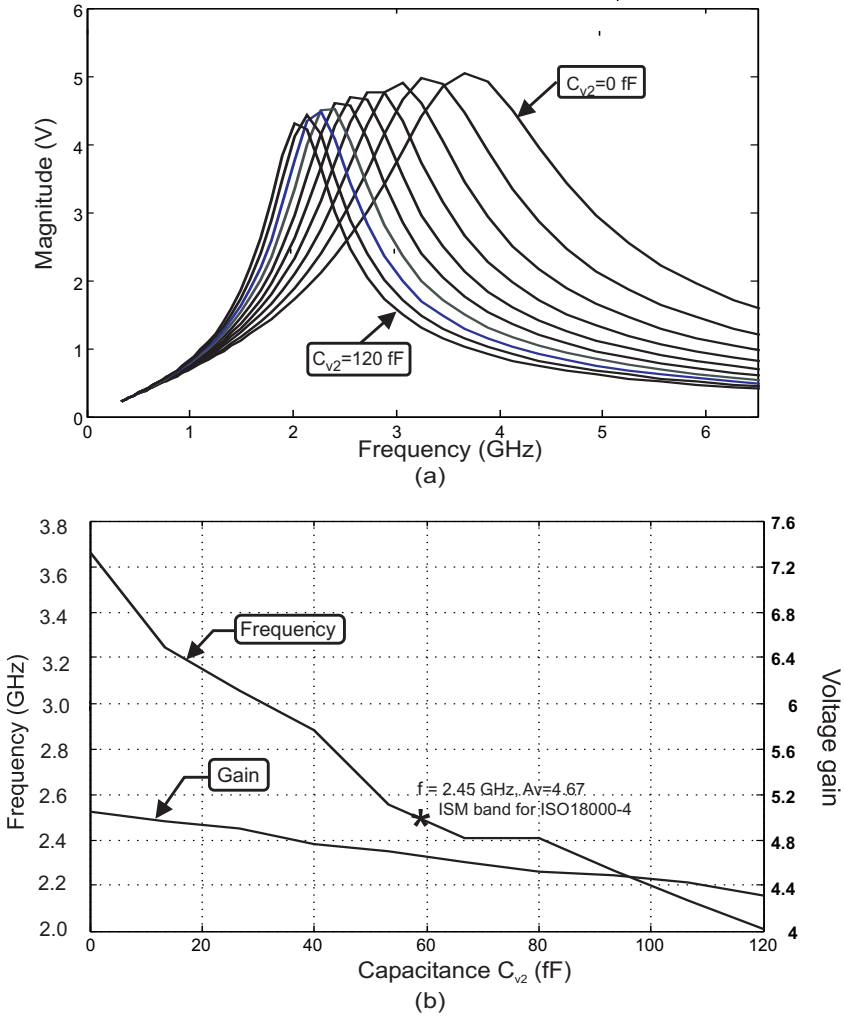


Figure 2.23. (a) Simulated dependence of the voltage gain of transformer impedance transformation network on C_{v2} and C_{v1} . (b) Simulated dependence of resonant frequency and voltage gain of transformer impedance transformation network on C_{v2} . note that C_{v1} is also varied with C_{v2} to maintain that the resonant condition is on the primary side (Copyright (c) IEEE).

rectifiers, each consisting of two diode-connected standard PMOS devices, one rectifying the positive and the other rectifying the negative half of the signal coming from the output of the matching network.

The sensitivity measurement of the power harvester with the step-up transformer impedance transformation network and that with the LC impedance transformation network is performed by measuring the dc output voltage for different levels of input signal power and the results are shown in Fig.2.24. It

is observed that the larger the load resistance, the larger the output voltage. The sensitivity of the power harvester with the step-up transformer impedance transformation network is more than twice that with the LC matching network.

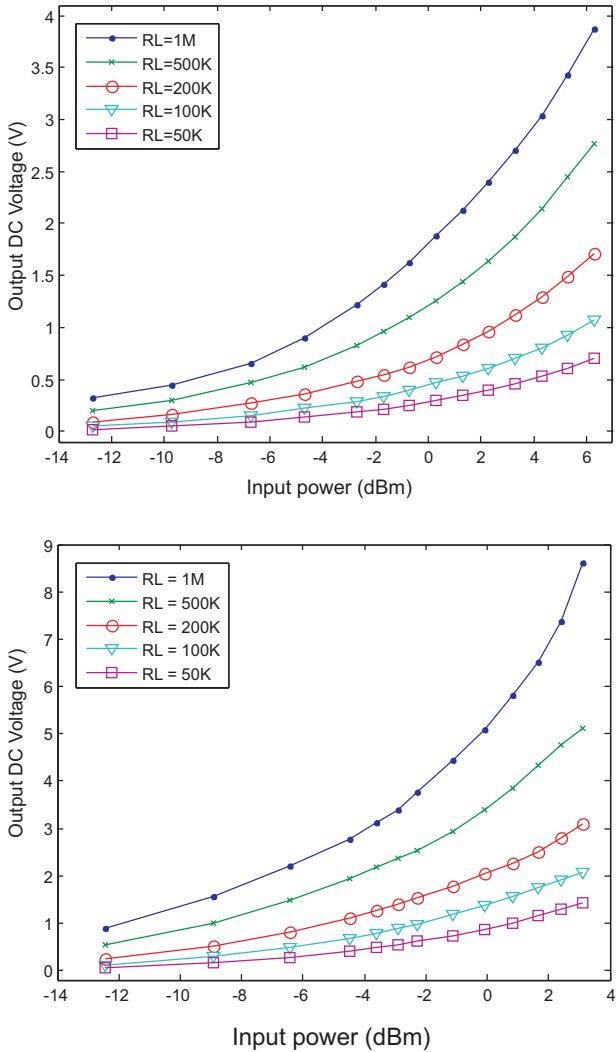


Figure 2.24. (a) Measured output voltage of the power harvester with a LC power-matching and gain-boosting network. (b) Measured output voltage of the power harvester with a step-up transformer power-matching and gain-boosting network (Copyright (c) IEEE).

Fig.2.25 plots the output DC voltage of both power harvesters. The output voltage of the power harvester with the LC matching network peaks at 3.5

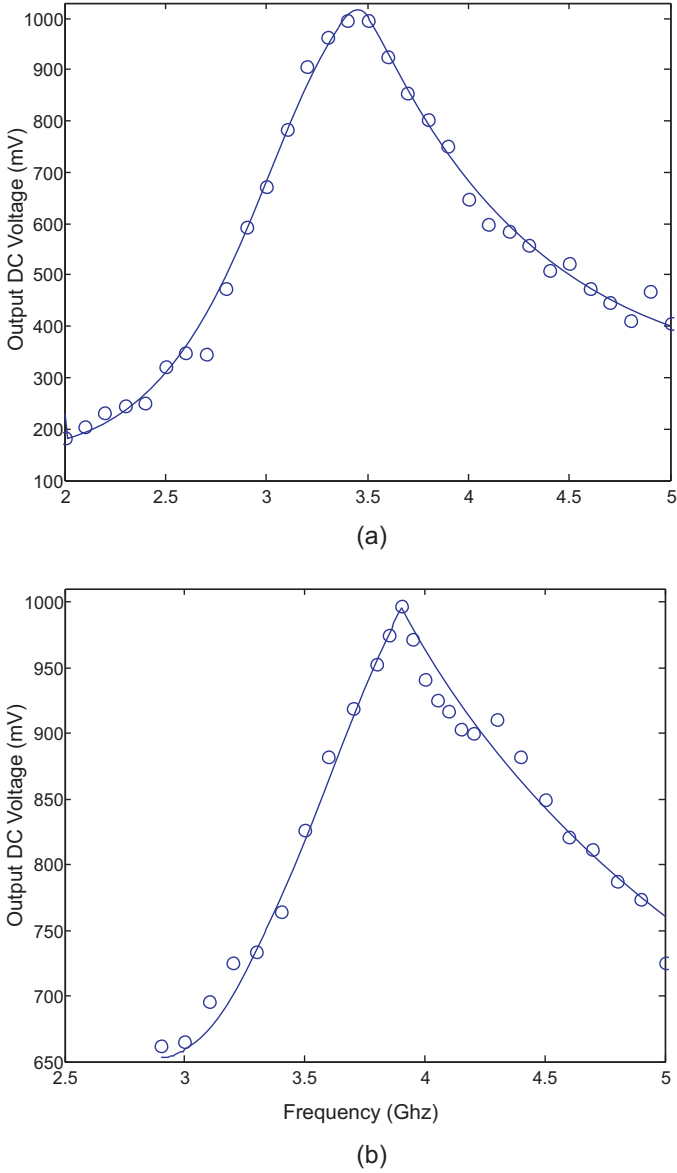


Figure 2.25. (a) Measured DC output voltage of the power harvester with a LC power-matching and gain-boosting network (Input power -4 dBm). (b) Measured DC output voltage of the power harvester with a step-up transformer power-matching and gain-boosting network (Input power -11.9 dBm) (Copyright (c) IEEE).

GHz approximately whereas that with the step-up transformer matching network peaks at 3.8 GHz approximately. Although the the impedance matching

networks are designed to peak at 2.45 GHz, parameter spreading caused by process variations gives rise to a large deviation of the resonant frequency. These observations re-affirm the importance of having the capability to tune the resonant frequency of power-matching and gain-boosting networks.

2.5 Chapter summary

The chapter started with the characterization of radio-frequency power harvesting systems. Power matching conditions have been derived and the maximum amount of the power delivered to the load has been obtained. Figure-of-merits such as power efficiency have been introduced. We have shown that the overall efficiency of a RF power harvester is determined by the efficiency of the antenna of the microsystems, the accuracy of power matching between the antenna and the voltage multiplier of the microsystem for the maximum power transmission, and the power efficiency of the voltage multiplier that converts a received RF signal to a dc voltage from which the microsystem is powered.

We have shown that power-matching and gain-boosting can be achieved simultaneously by inserting a passive impedance transformation network consisting of a spiral inductor and a metal-insulator-metal capacitor between the antenna and the multiplier. The impedance transformation network provides a matching impedance to the antenna to maximize the power transmission from the antenna to the impedance transformation network at the carrier frequency. At the same time, it resonates at the carrier frequency such that the voltage at the output of the impedance transformation network or the input of the voltage multiplier is maximized. The power efficiency of the LC power-matching and gain-boosting network is affected by the resistive loss mainly due to the ohmic loss of the spiral and capacitive loss due to the shunt capacitance between the spiral and the substrate of the spiral inductor. To increase the voltage gain of the LC impedance transformation network, the inductance must be increased. This, however, is echoed with the increased series and shunt losses of the inductor, and will result in the reduction of the overall power efficiency of the power harvester.

To further increase the voltage gain, a step-up transformer impedance-matching and gain-boosting to improve the efficiency of power harvest of passive wireless microsystems has been presented. A step-up transformer is characterized by a small voltage and a large current in the primary winding and a large voltage and a small current in the secondary winding. By employing a step-up transformer, the same power can be delivered from the primary winding to the secondary winding with a higher voltage at the secondary winding. Since the voltage of the secondary winding of the transformer will be larger than that of its primary winding while the current of the secondary winding will be smaller than that of its primary winding. The loss of the primary winding is dominated by its ohmic loss due to its large current while the loss of the

secondary winding is dominated by its spiral-substrate loss due to its large number of turns. Because the primary winding has a fewer turns, its series loss can be effectively reduced by increasing the width of the spiral of the primary winding. The width of the primary winding can be set to such a value that both windings will occupy approximately the same silicon area. The shunt loss of the secondary winding, on the other hand, can be lowered effectively by reducing the width of the spiral of the secondary winding. Note that since the current of the secondary winding is small, reducing the width of the spiral of the secondary winding will not overly increase its resistive loss.

The design techniques of voltage multipliers for power harvest of wireless microsystems have been investigated. For a passive wireless microsystem in the near field of the antenna of its base station, because inductive coupling is used, RF-to-DC conversion can be carried out using a diode bridge and the dc voltage at the output of the diode bridge is sufficiently large to power the passive wireless microsystem. Schottky diodes are widely used to further improve power efficiency. For a passive wireless microsystem in the far field of the antenna of its base station, the voltage at the antenna of the passive wireless microsystem is small and diode bridge-based rectification approaches become very inefficient. Voltage multipliers that perform both RF-to-DC conversion and voltage boosting are needed. Cockcroft-Walton voltage multiplier is a multi-stage configuration of voltage doublers. The effectiveness of Cockcroft-Walton voltage multiplier diminishes in monolithic integration where stray capacitances are large. Dickson voltage multiplier remove the drawback of Cockcroft-Walton voltage multiplier by injecting clocking signals into all the coupling nodes. Dickson voltage multiplier with MOSFET diodes, however, suffers from the drawback of low power efficiency due to the voltage loss of one threshold voltage across each MOSFET. Dickson voltage multiplier with static charge transfer switches minimizes this voltage loss and achieves a better power efficiency. Dickson voltage multiplier with bootstrapped gate transfer switches further improves power efficiency. Dickson voltage multipliers require a non-overlapping clock, which is not available in passive wireless microsystems. Modified Dickson voltage multipliers evolved from Dickson voltage multipliers can perform both RF-to-DC conversion and voltage boosting, and are therefore widely used in passive wireless microsystems. Modified Dickson voltage multipliers with MOSFET-diodes exhibit a low power efficiency due to the voltage loss across MOSFET diodes. The voltage multiplier by Mandal and Sarpeshkar exhibits a high power efficiency. The voltage multiplier with threshold voltage cancellation proposed by Umeda *et al.* utilizes an external voltage source to minimize the voltage drop across MOSFET switches so as to increases the power efficiency of the voltage multiplier. The voltage multiplier proposed by Nakamoto *et al.* employs an internal threshold voltage generation

mechanism to eliminate the voltage drop across MOSFETs without the need for an external voltage source.



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