

---

# Contents

<b>Preface to the Second Edition</b> .....	XIX
<b>Preface to the First Edition</b> .....	XXIII

---

## Part I General Background

---

<b>1 Introduction</b> .....	5
1.1 Evolution of integrated circuit technology .....	7
1.2 Evolution of design objectives .....	10
1.3 The problem of power distribution .....	14
1.4 Deleterious effects of power distribution noise .....	20
1.4.1 Signal delay uncertainty .....	21
1.4.2 On-chip clock jitter .....	21
1.4.3 Noise margin degradation .....	24
1.4.4 Degradation of gate oxide reliability .....	24
1.5 Summary .....	25
<b>2 Inductive Properties of Electric Circuits</b> .....	27
2.1 Definitions of inductance .....	28
2.1.1 Field energy definition .....	28
2.1.2 Magnetic flux definition .....	30
2.1.3 Partial inductance .....	35
2.1.4 Net inductance .....	40

2.2	Variation of inductance with frequency . . . . .	43
2.2.1	Uniform current density approximation . . . . .	44
2.2.2	Inductance variation mechanisms . . . . .	45
2.2.3	Simple circuit model . . . . .	49
2.3	Inductive behavior of circuits . . . . .	52
2.4	Inductive properties of on-chip interconnect . . . . .	54
2.5	Summary . . . . .	58
<b>3</b>	<b>Properties of On-Chip Inductive Current Loops . . . . .</b>	<b>59</b>
3.1	Introduction . . . . .	59
3.2	Dependence of inductance on line length . . . . .	60
3.3	Inductive coupling between two parallel loop segments . . . . .	67
3.4	Application to circuit analysis . . . . .	68
3.5	Summary . . . . .	69
<b>4</b>	<b>Electromigration . . . . .</b>	<b>71</b>
4.1	Physical mechanism of electromigration . . . . .	72
4.2	Electromigration-induced mechanical stress . . . . .	75
4.3	Steady state limit of electromigration damage . . . . .	76
4.4	Dependence of electromigration lifetime on the line dimensions . . . . .	78
4.5	Statistical distribution of electromigration lifetime . . . . .	81
4.6	Electromigration lifetime under AC current . . . . .	82
4.7	A comparison of aluminum and copper interconnect technologies . . . . .	83
4.8	Designing for electromigration reliability . . . . .	86
4.9	Summary . . . . .	86
<b>5</b>	<b>Decoupling Capacitance . . . . .</b>	<b>89</b>
5.1	Introduction to decoupling capacitance . . . . .	90
5.1.1	Historical retrospective . . . . .	90
5.1.2	Decoupling capacitor as a reservoir of charge . . . . .	91
5.1.3	Practical model of a decoupling capacitor . . . . .	93
5.2	Impedance of power distribution system with decoupling capacitors . . . . .	97
5.2.1	Target impedance of a power distribution system . . . . .	97
5.2.2	Antiresonance . . . . .	100
5.2.3	Hydraulic analogy of hierarchical placement of decoupling capacitors . . . . .	104

5.3	Intrinsic vs intentional on-chip decoupling capacitance	109
5.3.1	Intrinsic decoupling capacitance .....	110
5.3.2	Intentional decoupling capacitance .....	114
5.4	Types of on-chip decoupling capacitors .....	116
5.4.1	Polysilicon-insulator-polysilicon (PIP) capacitors .....	117
5.4.2	MOS capacitors .....	119
5.4.3	Metal-insulator-metal (MIM) capacitors .....	127
5.4.4	Lateral flux capacitors .....	129
5.4.5	Comparison of on-chip decoupling capacitors ..	133
5.5	On-chip switching voltage regulator .....	135
5.6	Summary .....	137
<b>6</b>	<b>Scaling Trends of On-Chip Power Distribution Noise</b> .....	<b>139</b>
6.1	Scaling models .....	140
6.2	Interconnect characteristics .....	142
6.2.1	Global interconnect characteristics .....	144
6.2.2	Scaling of the grid inductance .....	144
6.2.3	Flip-chip packaging characteristics .....	145
6.2.4	Impact of on-chip capacitance .....	147
6.3	Model of power supply noise .....	148
6.4	Power supply noise scaling .....	150
6.4.1	Analysis of constant metal thickness scenario ..	150
6.4.2	Analysis of the scaled metal thickness scenario	151
6.4.3	ITRS scaling of power noise .....	153
6.5	Implications of noise scaling .....	157
6.6	Summary .....	158
<b>7</b>	<b>Conclusions</b> .....	<b>159</b>

---

## Part II Design of Power Systems

---

<b>8</b>	<b>High Performance Power Distribution Systems</b> ....	<b>165</b>
8.1	Physical structure of a power distribution system ....	166
8.2	Circuit model of a power distribution system .....	167
8.3	Output impedance of a power distribution system ...	170
8.4	A power distribution system with a decoupling capacitor .....	173

8.4.1	Impedance characteristics . . . . .	173
8.4.2	Limitations of a single-tier decoupling scheme . . . . .	177
8.5	Hierarchical placement of decoupling capacitance . . . . .	179
8.6	Resonance in power distribution networks . . . . .	186
8.7	Full impedance compensation . . . . .	192
8.8	Case study . . . . .	194
8.9	Design considerations . . . . .	197
8.9.1	Inductance of the decoupling capacitors . . . . .	197
8.9.2	Interconnect inductance . . . . .	198
8.10	Limitations of the one-dimensional circuit model . . . . .	199
8.11	Summary . . . . .	202
<b>9</b>	<b>On-Chip Power Distribution Networks . . . . .</b>	<b>203</b>
9.1	Styles of on-chip power distribution networks . . . . .	204
9.1.1	Basic structure of on-chip power distribution networks . . . . .	204
9.1.2	Improving the impedance characteristics of on-chip power distribution networks . . . . .	209
9.1.3	Evolution of power distribution networks in Alpha microprocessors . . . . .	210
9.2	Die-package interface . . . . .	212
9.3	Other considerations . . . . .	217
9.4	Summary . . . . .	219
<b>10</b>	<b>Computer-Aided Design and Analysis . . . . .</b>	<b>221</b>
10.1	Design flow for on-chip power distribution networks . . . . .	222
10.2	Linear analysis of power distribution networks . . . . .	227
10.3	Modeling power distribution networks . . . . .	229
10.4	Characterizing the power current requirements of on-chip circuits . . . . .	236
10.5	Numerical methods for analyzing power distribution networks . . . . .	238
10.6	Allocation of on-chip decoupling capacitors . . . . .	245
10.6.1	Charge-based allocation methodology . . . . .	247
10.6.2	Allocation strategy based on the excessive noise amplitude . . . . .	248
10.6.3	Allocation strategy based on excessive charge . . . . .	249
10.7	Summary . . . . .	251

<b>11 Closed-Form Expressions for Fast <i>IR</i> Drop Analysis</b>	<b>253</b>
11.1 Background of FAIR . . . . .	254
11.2 Analytic <i>IR</i> drop analysis . . . . .	256
11.2.1 One power supply and one current load . . . . .	257
11.2.2 One power supply and multiple current loads . .	259
11.2.3 Multiple power supplies and one current load . .	260
11.2.4 Multiple power supplies and multiple current loads . . . . .	263
11.3 Locality in power grid analysis . . . . .	265
11.3.1 Principle of spatial locality in a power grid . . .	265
11.3.2 Effect of spatial locality on computational complexity . . . . .	269
11.3.3 Exploiting spatial locality in FAIR . . . . .	270
11.3.4 Error correction windows . . . . .	271
11.4 Experimental results . . . . .	272
11.5 Summary . . . . .	276
<b>12 Conclusions</b> . . . . .	<b>279</b>

---

## Part III Noise in Power Distribution Networks

---

<b>13 Inductive Properties of On-Chip Power Distribution Grids</b> . . . . .	<b>285</b>
13.1 Power transmission circuit . . . . .	285
13.2 Simulation setup . . . . .	288
13.3 Grid types . . . . .	288
13.4 Inductance versus line width . . . . .	293
13.5 Dependence of inductance on grid type . . . . .	294
13.5.1 Non-interdigitated versus interdigitated grids . .	294
13.5.2 Paired versus interdigitated grids . . . . .	295
13.6 Dependence of Inductance on grid dimensions . . . . .	296
13.6.1 Dependence of inductance on grid width . . . . .	296
13.6.2 Dependence of inductance on grid length . . . . .	298
13.6.3 Sheet inductance of power grids . . . . .	298
13.6.4 Efficient computation of grid inductance . . . . .	299
13.7 Summary . . . . .	301

<b>14</b>	<b>Variation of Grid Inductance with Frequency</b>	<b>303</b>
14.1	Analysis approach	303
14.2	Discussion of inductance variation	305
14.2.1	Circuit models	305
14.2.2	Analysis of inductance variation	308
14.3	Summary	310
<b>15</b>	<b>Inductance/Area/Resistance Tradeoffs</b>	<b>313</b>
15.1	Inductance vs. resistance tradeoff under a constant grid area constraint	313
15.2	Inductance vs. area tradeoff under a constant grid resistance constraint	318
15.3	Summary	320
<b>16</b>	<b>Inductance Model of Interdigitated Power and Ground Distribution Networks</b>	<b>323</b>
16.1	Basic four-pair structure	324
16.2	Power and ground distribution network with a large number of interdigitated pairs	325
16.3	Comparison and discussion	330
16.4	Summary	334
<b>17</b>	<b>On-Chip Power Noise Reduction Techniques</b>	<b>337</b>
17.1	Ground noise reduction through an additional low noise on-chip ground	339
17.2	Dependence of ground bounce reduction on system parameters	341
17.2.1	Physical separation between noisy and noise sensitive circuits	342
17.2.2	Frequency and capacitance variations	343
17.2.3	Impedance of an additional ground path	345
17.3	Summary	346
<b>18</b>	<b>Noise Issues in On-Chip Power Distribution Networks</b>	<b>349</b>
18.1	Scaling effects in chip-package resonance	350
18.2	Propagation of power distribution noise	352
18.3	Local inductive behavior	355
18.4	Summary	359

<b>19 Conclusions</b> .....	361
-----------------------------	-----

---

## Part IV Placement of On-Chip Decoupling Capacitance

---

<b>20 Effective Radii of On-Chip Decoupling Capacitors</b>	367
20.1 Background .....	369
20.2 Effective radius of on-chip decoupling capacitor based on target impedance .....	371
20.3 Estimation of required on-chip decoupling capacitance	373
20.3.1 Dominant resistive noise .....	374
20.3.2 Dominant inductive noise .....	375
20.3.3 Critical line length .....	378
20.4 Effective radius as determined by charge time .....	380
20.5 Design methodology for placing on-chip decoupling capacitors .....	386
20.6 Model of on-chip power distribution network .....	386
20.7 Case study .....	389
20.8 Design implications .....	395
20.9 Summary .....	396
 <b>21 Efficient Placement of Distributed On-Chip Decoupling Capacitors</b> .....	399
21.1 Technology constraints .....	400
21.2 Placing on-chip decoupling capacitors in nanoscale ICs	401
21.3 Design of a distributed on-chip decoupling capacitor network .....	404
21.4 Design tradeoffs in a distributed on-chip decoupling capacitor network .....	409
21.4.1 Dependence of system parameters on $R_1$ .....	410
21.4.2 Minimum $C_1$ .....	411
21.4.3 Minimum total budgeted on-chip decoupling capacitance .....	412
21.5 Design methodology for a system of distributed on-chip decoupling capacitors .....	414
21.6 Case study .....	417
21.7 Summary .....	421

<b>22 Simultaneous Co-Design of Distributed On-Chip Power Supplies and Decoupling Capacitors.....</b>	<b>423</b>
22.1 Problem formulation.....	425
22.2 Simultaneous power supply and decoupling capacitor placement .....	426
22.3 Case study .....	428
22.4 Summary .....	432
<b>23 Conclusions .....</b>	<b>433</b>

---

**Part V Multi-Layer Power Distribution Networks**

---

<b>24 Impedance Characteristics of Multi-Layer Grids ..</b>	<b>439</b>
24.1 Electrical properties of multi-layer grids.....	441
24.1.1 Impedance characteristics of individual grid layers .....	441
24.1.2 Impedance characteristics of multi-layer grids ..	444
24.2 Case study of a two layer grid .....	446
24.2.1 Simulation setup .....	447
24.2.2 Inductive coupling between grid layers.....	447
24.2.3 Inductive characteristics of a two layer grid ...	451
24.2.4 Resistive characteristics of a two layer grid ....	452
24.2.5 Variation of impedance with frequency in a two layer grid .....	454
24.3 Design implications.....	455
24.4 Summary .....	456
<b>25 Multi-Layer Interdigitated Power Distribution Networks .....</b>	<b>459</b>
25.1 Single metal layer characteristics .....	461
25.1.1 Optimal width for minimum impedance .....	463
25.1.2 Optimal width characteristics .....	466
25.2 Multi-layer optimization .....	469
25.2.1 First approach - equal current density .....	470
25.2.2 Second approach - minimum impedance .....	476
25.3 Discussion.....	478
25.3.1 Comparison.....	478
25.3.2 Routability .....	479
25.3.3 Fidelity .....	482



25.3.4 Critical frequency .....	483
25.4 Summary .....	484
<b>26 Conclusions .....</b>	<b>487</b>
<hr/>	
<b>Part VI Multi-Voltage Power Network Systems</b>	
<hr/>	
<b>27 Multiple On-Chip Power Supply Systems .....</b>	<b>493</b>
27.1 ICs with multiple power supply voltages .....	494
27.1.1 Multiple power supply voltage techniques .....	495
27.1.2 Clustered voltage scaling (CVS) .....	497
27.1.3 Extended clustered voltage scaling (ECVS) ...	498
27.2 Challenges in ICs with multiple power supply voltages	499
27.2.1 Die area .....	500
27.2.2 Power dissipation .....	500
27.2.3 Design complexity .....	501
27.2.4 Placement and routing .....	501
27.3 Optimum number and magnitude of available power supply voltages .....	504
27.4 Summary .....	509
<b>28 On-Chip Power Distribution Grids with Multiple Supply Voltages .....</b>	<b>511</b>
28.1 Background .....	513
28.2 Simulation setup .....	514
28.3 Power distribution grid with dual supply and dual ground .....	516
28.4 Interdigitated grids with DSDG .....	519
28.4.1 Type I interdigitated grids with DSDG .....	519
28.4.2 Type II interdigitated grids with DSDG .....	521
28.5 Paired grids with DSDG .....	523
28.5.1 Type I paired grids with DSDG .....	524
28.5.2 Type II paired grids with DSDG .....	525
28.6 Simulation results .....	528
28.6.1 Interdigitated power distribution grids without decoupling capacitors .....	529
28.6.2 Paired power distribution grids without decoupling capacitors .....	536

28.6.3 Power distribution grids with decoupling capacitors .....	537
28.6.4 Dependence of power noise on the switching frequency of the current loads .....	541
28.7 Design implications .....	544
28.8 Summary .....	546
<b>29 Decoupling Capacitors for Multi-Voltage Power Distribution Systems .....</b>	<b>549</b>
29.1 Impedance of a power distribution system .....	551
29.1.1 Impedance of a power distribution system ....	552
29.1.2 Antiresonance of parallel capacitors .....	555
29.1.3 Dependence of impedance on power distribution system parameters .....	556
29.2 Case study of the impedance of a power distribution system .....	559
29.3 Voltage transfer function of power distribution system .....	564
29.3.1 Voltage transfer function of a power distribution system .....	564
29.3.2 Dependence of voltage transfer function on power distribution system parameters .....	566
29.4 Case study of the voltage response of a power distribution system .....	569
29.4.1 Overshoot-free magnitude of a voltage transfer function .....	571
29.4.2 Tradeoff between the magnitude and frequency range .....	573
29.5 Summary .....	577
<b>30 Conclusions .....</b>	<b>579</b>
<hr/>	
<b>Part VII Final Comments and Supplementary Material</b>	
<hr/>	
<b>Closing Remarks .....</b>	<b>583</b>
<b>Appendices</b>	
<b>A Estimate of Initial Optimal Width for Interdigitated Power/Ground Network .....</b>	<b>591</b>

<b>B</b>	<b>First Optimization Approach for Multi-Layer Interdigitated Power Distribution Network.....</b>	<b>593</b>
<b>C</b>	<b>Second Optimization Approach for Multi-Layer Interdigitated Power Distribution Network.....</b>	<b>595</b>
<b>D</b>	<b>Mutual Loop Inductance in Fully Interdigitated Power Distribution Grids with DSDG.....</b>	<b>597</b>
<b>E</b>	<b>Mutual Loop Inductance in Pseudo-Interdigitated Power Distribution Grids with DSDG.....</b>	<b>599</b>
<b>F</b>	<b>Mutual Loop Inductance in Fully Paired Power Distribution Grids with DSDG.....</b>	<b>601</b>
<b>G</b>	<b>Mutual Loop Inductance in Pseudo-Paired Power Distribution Grids with DSDG.....</b>	<b>603</b>
	<b>References.....</b>	<b>605</b>
	<b>Index.....</b>	<b>633</b>
	<b>About the Authors.....</b>	<b>639</b>

Power Distribution Networks with On-Chip Decoupling  
Capacitors

Jakushokas, R.; Popovich, M.; Mezhiba, A.V.; Köse, S.;  
Friedman, E.G.

2011, XXV, 644 p., Hardcover

ISBN: 978-1-4419-7870-7