

Preface

1 Abstract

Low volume production of FPGA-based products is quite effective and economical because they are easy to design and program in shortest possible time. The generic reconfigurable resources in an FPGA can be programmed to execute a vast variety of applications at mutually exclusive times. However, the flexibility of FPGAs makes them much larger, slower, and more power consuming than their counterpart ASICs. Consequently, FPGAs are unsuitable for applications requiring high volume production, high performance or low power consumption. The main theme of this work is to reduce area of FPGAs by introducing heterogeneous hard-blocks (such as multipliers, adders etc) in FPGAs, and by designing application specific FPGAs. Automatic FPGA layout generation techniques are employed to decrease non-recurring engineering (NRE) costs and time-to-market of application specific heterogeneous FPGA architectures.

This work initially presents a new environment for the exploration of mesh-based heterogeneous FPGA architectures. An architecture description mechanism allows to define new heterogeneous blocks. A variety of automatic and manual options can be selected to optimize floor-planning of heterogeneous blocks on the FPGA architecture. The exploration environment later allows to test different benchmark circuits on the newly defined heterogeneous FPGA architecture. An automatic FPGA layout generator is presented which generates a tile-based FPGA layout for a subset of architectures generated by our exploration environment. We have successfully taped-out a 1024 Look-Up Table based mesh FPGA architecture using 130nm 6-metal layer CMOS process of ST.

The Heterogeneous FPGA exploration environment is further enhanced to explore application specific FPGAs. If a digital product is required to provide multiple functionalities at exclusive times, each distinct functionality represented by an application circuit is efficiently mapped on an FPGA. Later, the FPGA is reduced for the given set of application circuits. This reduced FPGA is proposed and termed here as an Application Specific Inflexible FPGA (ASIF). The main idea is to perform prototyping, testing and even initial shipment of a design on an FPGA; later it can be migrated to an ASIF for high volume production. ASIF generation techniques can also be employed to generate a single configurable ASIC core that can perform multiple tasks at different times. An ASIF for 20 MCNC benchmark circuits is found to be 82% smaller than a traditional mesh-based unidirectional FPGA required to map any of these circuits. An ASIF can also be reprogrammed to execute new or modified circuits,

but unlike FPGAs, at a very limited scale. A new CAD flow is presented which can map new application circuits on an ASIF. An automatic ASIF hardware generator is also presented.

2 Dedication

Dedicated to my parents, and to Scamoail, Hasan, Omer and Asma.

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Architectures

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