

# Preface

Repair techniques for nanoscale memories are becoming more important to cope with ever-increasing “errors” causing degraded yield and reliability. In fact, without repair techniques, even modern CMOS LSIs, such as MPUs/SoCs, in which memories have dominated the area and performances, could not have been successfully designed. Indeed, various kinds of errors have been prominent with larger capacity, smaller feature size, and lower voltage operations of such LSIs. The errors are categorized as hard/soft errors, timing/voltage margin errors, and speed-relevant errors. Hard/soft errors and timing/voltage margin errors, which occur in a chip, are prominent in a memory array because the array comprises memory cells having the smallest size and largest circuit count in the chip. In particular, coping with the margin errors is vital for low-voltage nanoscale LSIs, since the errors rapidly increase with device and voltage scaling. Increase in operating voltage is one of the best ways to tackle the issue. However, this approach is unacceptable due to intolerably increased power dissipation, calling for other solutions by means of devices and circuits. Speed-relevant errors, which are prominent at a lower voltage operation, comprise speed-degradation errors of the chip itself and intolerably wide chip-to-chip speed-variation errors caused by the ever-larger interdie design-parameter variation. They must also be solved with innovative devices and circuits. For the LSI industry, in order to flourish and proliferate, the problems must be solved based on in-depth investigation of the errors.

Despite the importance, there are few authoritative books on repair techniques because the solutions to the problems lie across different fields, e.g., mathematics and engineering, logic and memories, and circuits and devices. This book systematically describes the issues, based on the authors’ long careers in developing memories and low-voltage CMOS circuits. This book is intended for both students and engineers who are interested in the yield, reliability, and low-voltage operation of nanoscale memories. Moreover, it is instructive not only to memory designers, but also to all digital and mixed-signal LSI designers who are at the leading edge of such LSI developments.

Chapter 1 describes the basics of repair techniques. First, after categorizing sources of hard/soft errors, the reductions by means of redundancy, error checking

and correction (ECC), and their combination are comprehensively described. Second, after defining the minimum operating voltage  $V_{\min}$ , reductions of timing/voltage margin errors are described in terms of  $V_{\min}$ . Finally, reduction techniques for speed-relevant errors are briefly discussed.

Chapter 2 deals with a detailed explanation of the redundancy techniques for repairing hard errors (faults), where faulty memory cells are replaced by spare memory cells provided on the chip in advance. Various yield models and calculations are introduced and various practical circuits and architectures that the authors regard as important for higher yield and reliability are discussed. The chapter also describes the devices for memorizing the addresses of faults and testing techniques for redundancy.

Chapter 3 describes the details of the ECC techniques to cope with both hard and soft errors, where extra bits (check bits) are added to original data bits, thereby enabling error detection and/or correction. After mathematical preparations, various error-correcting codes used for the techniques and their practical implementations in various memory LSIs are discussed. This is followed by the estimation of the reduction in hard-error and soft-error rates using ECC. Testing techniques for ECC are also described.

Chapter 4 deals with the combination of the redundancy and ECC. Combining both the techniques generates a synergistic effect and dramatically enhances the repair capability. It is especially effective for random-bit errors. After quantitative estimation of the synergistic effect, the application to the repair of faults due to device mismatch is discussed as a promising application of the effect.

Chapter 5 systematically describes challenges to ultra-low-voltage nanoscale memories and the repair techniques to accomplish the issues. After clarifying that reduction in the minimum operating voltage  $V_{DD}$  (i.e.,  $V_{\min}$ ) is the key to reducing the voltage and timing margin error, adaptive circuits and relevant technologies to reduce  $V_{\min}$  are proposed, and the general features are described. Then, the  $V_{\min}$ s of logic gates, SRAMs, and DRAMs are compared. After that, devices (e.g., fully depleted planar SOI and FinFET structures), circuits (e.g., gate-source reverse biasing schemes accepting low threshold voltage ( $V_t$ ) MOSFETs), and subsystems to widen the margins through reducing  $V_{\min}$  are described.

Chapter 6 briefly describes device/circuit techniques to cope with two kinds of speed-relevant errors, namely, the speed degradation error and the interdie speed variation error. After specifying reduced gate-over-drive voltage of MOSFETs as the source of the speed degradation error, some solutions (e.g., using low- $V_{t0}$  circuits and dynamic  $V_t$  circuits utilizing double-gate FD-SOI structures) are exemplified. Moreover, after specifying the so-called global variation of design parameters in the wafer as the source of the interdie speed variation error, some solutions such as power management for compensating for the variation with static or quasi-static controls of internal supply voltages are presented.



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