

# Preface

This book highlights the research conducted in the area of Multi-Processor System-on-Chip design for more than five years. The work documented within was carried out during my time at the Institute of Integrated Signal Processing Systems (ISS) at the RWTH Aachen University.

More than putting forth a brilliant idea, the conducted work reflects a careful evolution of design methodologies and associated tooling. The original motivation dates back to the GRACE++ methodology. This early attempt of system level modeling with SystemC targeted the efficient and convenient exploration of complex architectures, with particular focus on communication architectures. The tight links to industry partners and the ongoing development turned this technology into a commercialized tool called Architects View Framework.

At the time I joined the ISS as a researcher, plenty of experience had been gained in modeling System-on-Chip platforms. By the investigation of several industrial platforms, we soon discovered that the detailed modeling of processing elements limited the capabilities of design space exploration. Accordingly, we extended the methodology to a more abstract modeling of processing elements and, furthermore, broadened it to capture the challenges of temporal and spatial task mapping. With the help of many partners from different research cooperations, we have evolved the methodology and were lucky to be able to validate our approach with relevant design problems. Finally, this innovative technology was brought to the market and became commercially available in 2009.

All the design issues to be found in the development of MPSoC platforms cannot be mastered by a single person. Therefore, I am grateful for the strong support of researchers with whom I had the pleasure to work.

First of all, I would like to thank my supervisor and Prof. Gerd Ascheid who is the co-author of this book. Apart from his valuable feedback and deep interest in my work, I enjoyed the creative working atmosphere of independent research while being guided by inspiring discussions. In the same way, I would like to thank my co-examiner and co-author Prof. Rainer Leupers for his support and valuable feedback.

As mentioned before, my work is based on the Architects View Framework developed by Tim Kogel. Not only for supervising my master's thesis, but also for the joined research projects, I would like to convey my gratitude to Tim.

In addition, I would like to thank my former colleague and office-mate Andreas Wieferink who recruited me to the ISS when I was an undergraduate student. He was always helpful in solving critical debugging issues.

I am grateful to all my colleagues at ISS, who supported me in my research work. Among them I would like give my special thanks to Filippo Borlenghi, Jeronimo Castrillon, Anupam Chattopadhyay, Meik Dörpinghaus, Felix Engel, Lei Gao, Niels Hadaschik, Manuel Hohenauer, David Kammler, Kingshuk Karuri, Stefan Kraemer, Hanno Scharwächter, Stefan Schürmans, Martin Senst, Martin Witte and Diandian Zhang.

When performing research in the area of EDA tools, I personally consider tight interaction with semiconductor and EDA companies as essential to address the key design issues. Luckily, at ISS I had the unique opportunity to meet many helpful professionals over the years, which gave constant guidance and valuable feedback. My special thanks are due to Xavier Buisson, Andreas Hoffmann, Karl Van Rompaey, Bart Vanthournout from CoWare/Synopsys, and to all the professionals we met during the roadshow of the Virtual Processing Unit (VPU).

Converting my ideas into usable tools would have not been possible without the help of my postgraduate students. I would like to thank all of them for their efforts and hard work. Among them, I would like to give special thanks to Jens Reinecke and Stefan Wallentowitz. Furthermore, I would like to thank Filippo Borlenghi, Jeronimo Castrillon, and James Wood for reviewing this book.

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