

Contents

- 1 Introduction 1**
 - 1.1 The Consumer Electronics Landscape 1
 - 1.2 Design Alternatives for Processing Elements 3
 - 1.3 The ASIP Design Conundrum 7
 - 1.4 Outline of the Book 9

- 2 The ASIP Design Space 11**
 - 2.1 Introduction 11
 - 2.2 Architectural Alternatives for ASIPs 12
 - 2.2.1 Instruction-set Architecture 12
 - 2.2.2 Instruction Pipelining 14
 - 2.2.3 Instruction and Data Parallelism 20
 - 2.2.4 Hardware Acceleration Technologies 24
 - 2.2.5 Register File Architecture 27
 - 2.2.6 Memory Subsystem Design 29
 - 2.2.7 Arithmetic Data Types 31
 - 2.2.8 Partially Reconfigurable ASIPs 32
 - 2.3 Cross Cutting Issue: Designing Optimizing Compilers 33

- 3 Design Automation Tools for ASIP Design 35**
 - 3.1 Introduction 35
 - 3.2 A Generic ASIP Design Flow 35
 - 3.3 The State-of-the-Art in ASIP Design 38
 - 3.3.1 Specification Based Design Flows 38
 - 3.3.2 Configuration Based Design Flows 42
 - 3.4 The Application Analysis Design Gap 45
 - 3.5 Synopsis 49

4	Profiling for ASIP Design	51
4.1	Introduction	51
4.2	Limitations of Traditional Profiling Tools	52
4.3	Profiling for ASIP Architectures: Instruction-set Simulators	53
4.4	μ -Profiler: A Pre-architectural Profiling Tool	55
4.5	Synopsis	57
5	μ-Profiler: Design and Implementation	59
5.1	Introduction	59
5.2	Software Architecture	62
5.3	The LANCE Compiler System	63
5.3.1	Computations in the LANCE IR	65
5.3.2	Control Flow in the LANCE IR	67
5.4	Instrumentation Engine and the Profiler Library	69
5.4.1	A Simple Example of Instrumentation	70
5.4.2	Algorithms and Data Structures of the Profiler Library	73
5.5	Profiling Options and the μ -Profiler GUI	76
5.6	Profiling for Memory Hierarchy Design	81
5.6.1	Memory Accesses in the LANCE IR	82
5.6.2	Memory Profiling Techniques	82
5.7	Profiling Results	86
5.7.1	Profiling Accuracy	86
5.7.2	Speed of μ -Profiling	90
5.8	Synopsis	90
6	A Primer on ISA Customization	93
6.1	Introduction	93
6.2	ISE Generation Under Various Constraints	95
6.2.1	Generic Constraints	96
6.2.2	Architectural Constraints	97
6.3	Related Work on ISA Customization	100
6.3.1	ISE Generation	101
6.3.2	Increasing Data Bandwidth to ISEs	106
6.4	A Seamless Application to Architecture ISA Customization Flow	108
6.5	Synopsis	109
7	ISA Customization Design Flow	111
7.1	Introduction	111
7.2	Components of the ISA Customization Flow	112
7.2.1	The ISA Customization Front-End	113
7.2.2	ISE Generation	115
7.2.3	The ISA Customization Back-End	119
7.3	Generation of Implementation and Utilization Files	123
7.3.1	The LISA Back-End	125
7.4	Synopsis	130

8	ISE Generation Algorithms	131
8.1	Mathematical Formulation of the ISA Customization Problem	131
8.1.1	ISEs and Internal Register Files	134
8.2	ISA Customization Using ILP	137
8.2.1	DFG Partitioning into ISEs	139
8.2.2	Edge Type Assignment	150
8.3	Instruction-set Customization Using High Level Synthesis	152
8.3.1	Basics of Processor Customization Using HLS	154
8.3.2	ISE Generation Through Resource Constrained Scheduling	156
8.3.3	Resource Allocation and Binding	163
8.4	IR Minimization	165
8.5	Computational Complexity of the HLS Based Algorithm	167
8.6	Results	168
8.6.1	ILP Versus HLS Based Algorithms	168
8.6.2	Accuracy of Speed-Up Estimation	170
8.6.3	Effects of I/O Constraints	171
8.6.4	Effects of Resource Sharing and IR Minimization	172
8.7	Synopsis	174
9	Increasing Data Bandwidth to ISEs Through Register Clustering	175
9.1	Introduction	175
9.2	Clustered Register File Architecture	176
9.3	Cluster Allocation in Presence of ISEs	179
9.3.1	Cluster Allocation Problem	180
9.3.2	Cluster Allocation Algorithm	181
9.4	Results	187
9.4.1	Benchmark Speed-Ups	187
9.4.2	Area/Speed-Up Trade-Offs for Clustering	190
9.5	Synopsis	191
10	Case Studies	193
10.1	Introduction	193
10.2	ISA Customization of MIPS 32 with CorExtend	194
10.3	ISA Customization of ARC 600	196
10.4	Development of an MP3 Audio Decoder	197
10.4.1	Operator Usage Analysis	198
10.4.2	Processor ISA Modification	198
10.4.3	Deriving the Final Configuration	199
10.5	Development of a H.264 Video Decoder	200
10.5.1	Operator Usage Analysis	200
10.5.2	Manual ISA Customization	201
10.5.3	Automated ISA Customization	202

10.5.4	Final Optimizations.....	203
10.5.5	Summary of Configurations.....	205
11	Summary: Taking Stock of Application Analysis	207
A	Post ISE Generation DFG Transformation Algorithms	211
A.1	ISE Latency Estimation	211
A.2	ISE Scheduling	213
A.3	IR Allocation	215
	References	219
	Index	229

Application Analysis Tools for ASIP Design
Application Profiling and Instruction-set Customization
Karuri, K.; Leupers, R.
2011, XXII, 232 p., Hardcover
ISBN: 978-1-4419-8254-4