

Chapter 2

The Design Space Exploration: Simplified Case

Abstract In this chapter, the *design space exploration* is exposed and explained as the main tool to get an optimized design of a fully integrated switching power converter. The converter output voltage ripple is used to constraint the design space, while the merit figure to be optimized is defined as the power efficiency versus the occupied silicon area ratio. Additionally, an overall structure of the design space exploration including particular optimizations for each component design is proposed. Then, simplified models for the converter integrated components (i.e. inductor, capacitor, power drivers and power transistors) are presented, as well as an analytical output ripple model that takes into account the output capacitor *Equivalent-Series-Resistance* (ESR). Finally, the design space exploration optimization procedure is exemplified by means of the design of a classical Buck converter, where the simplified components models are used.

2.1 Main Concepts and Design Procedure

In the first steps of a switching power converter design (once the required topology has been determined), there are many questions and decisions to answer regarding input and output voltage ranges, output current, switching frequency, the reactive components values (mainly inductors and capacitors), transformer input–output voltage ratio (if any is required by the design), even some dynamic performance parameters such as bandwidth. If different technological options are considered to implement the power switches and their corresponding drivers, the design options can become overwhelming.

In order to develop an appropriate design procedure, it is interesting to classify the design variables or parameters into different categories to identify their impact upon the design characteristics or performance. In the following, groups proposed herein are presented.

Application parameters. Those parameters that are completely defined by the application needs, like input and output voltage ranges, output current capability and output voltage ripple. Usually, application parameters appear as *hard constraints* in the design space. Additionally, other less conventional

parameters or constraints can be defined: radiated interferences spectrum, maximum input current, etc. . .

Static design variables. Conventional design variables, such as inductance and capacitance value, or the voltage conversion ratio of a transformer. We call them ‘static’ because although they offer degrees of freedom in the design stage, they become fixed once the design is implemented.

Dynamic design variables. The main dynamic design variable that appears in the design of a conventional switching power converter is the switching frequency, since although it can be determined during the design stage, it offers an additional degree of freedom once the converter is implemented, that allows to better fit to application parameter changes.

Performance factor. This category includes those factors that indicate the power converter quality, once application parameters are satisfied or accomplished. Most common performance factors are energy efficiency in power conversion, the bandwidth of the output response versus the control signal, the volume and area occupation, its weight. They can appear as *soft constraints*, since they might not invalidate the design despite it could be interesting to maximize or minimize them. In fact, depending on the application, they could be totally or partially defined as *application parameters* (i.e. in case where a minimum power efficiency is required, or a maximum weight is allowed).

Technological information. This refers to information related to the physical implementation of the converter components, specially in case of the power switches and their corresponding drivers. Although first order approach designs do not require detailed information about the technology used to implement any component, information about non idealities and parasitics is needed to take into account some performance factors (e.g. energy efficiency).

In Table 2.1, the previous classification is summarized. In this case, only those variables that are particularly relevant for the case of integrated switching converters are shown.

Obviously, the categories and what they include could change if non conventional designs are considered, i.e. multiple conversion ratio transformers, variable capacitors, etc. . .

From the previous classification a design procedure is derived, which is described in the following.

1. First of all, taking into account the application parameters, some converter topologies are selected to fit specifications, and the corresponding required ideal analytical expressions for voltages and currents are obtained. In this design step, system-level simulations can be used to confirm that the selected topologies (it could be interesting to consider more than one topology, in order to select the optimum one afterwards, from the performance factors evaluation) suit the application parameters.

Table 2.1 Design variables and parameters classification used in the thesis

Category	Parameters/Variables
Application parameters	Input voltage range Output voltage range Output current range Output voltage ripple
Static design variables	Inductance value Capacitance value
Dynamic design variables	Switching frequency
Performance factors	Energy efficiency Occupied area
Technological information	Equivalent parasitic resistances for each component Parasitic capacitors for each component Capacitive density (capacitance per area) Inductive density (inductance per area)

2. Then, the design variables (static and dynamic) impact on the design are determined by means of ideal expressions or model, and some performance factors can be evaluated (i.e. maximum inductor current). At this point, converter topologies options should be shrunk down to a few ones that suit the application; and some design variables range of values should be partially delimited, by checking some application parameters fulfillment (e.g. maximum output voltage ripple). Power switches are considered ideal and no parasitic components or non idealities are considered.
3. The following design step implies a further increase in the model complexity. It is necessary to decide the technological implementation of the different components of the switching power converter. In case of integrated monolithic converters, this requires to select the microelectronic process used to manufacture the design. The foundry provides information about what is feasible or unfeasible to implant in the selected process, and detailed models for components that lead to parasitic characterization. The addition of all this information generates a notable increase in the converter model complexity, and circuit-level simulations become fundamental (although complex system-level simulation are still interesting). The result of this design stage is the evaluation of performance factors such as energy efficiency and volume (or area) occupation, which should lead to an optimized design.

It should be noted that steps 2 and 3 of such design procedure should be carried out for any different selected topology, to choose the one that provides the best performance factors. Furthermore, it is possible that, in spite of the accomplishment of the application parameters, the evaluation of the performance factors results in so poor quality or performance that another topology or design must be considered from the initial point (Fig. 2.1 summarizes the whole process explained above).

Therefore, once the design variables have been identified and their corresponding range of values have been constrained by the application parameters criteria, any combination of design variables values should be explored to evaluate the selected

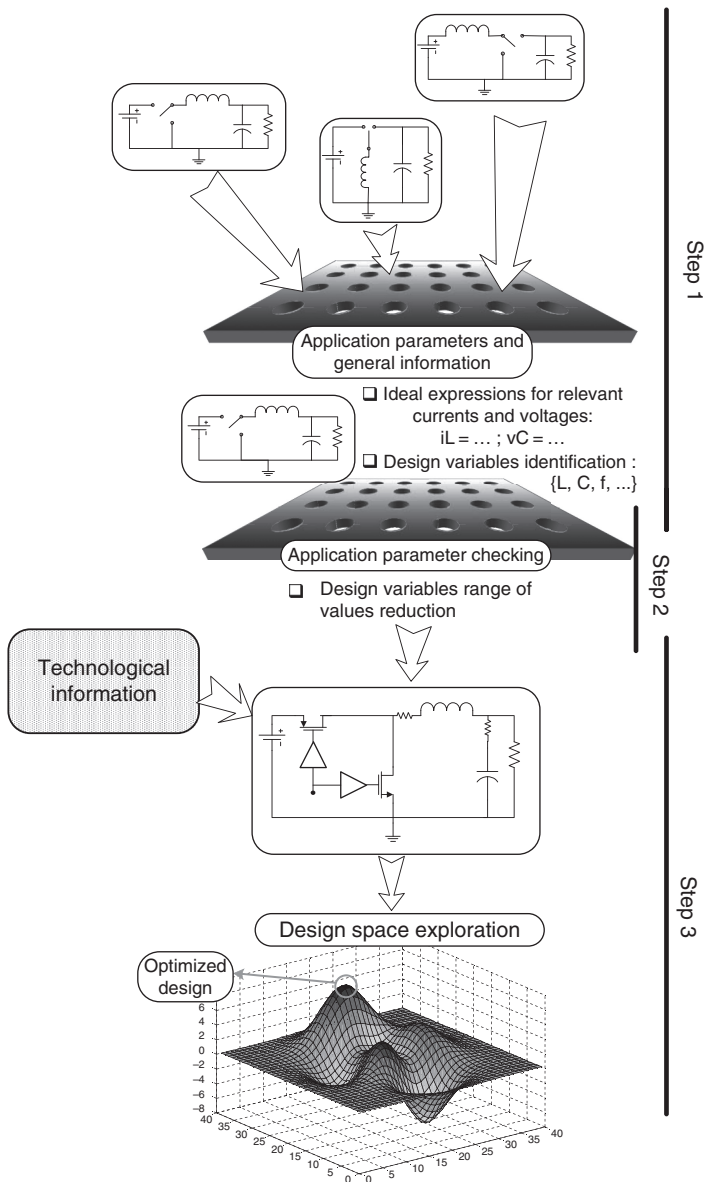


Fig. 2.1 Proposed design procedure. The optimized design is obtained by means of the design space exploration

performance factors. For the sake of simplicity, all the performance factors can be joined in a merit figure definition to obtain a single index that leads to a mathematical maximization, in order to get the desired optimized design. In the following, a representative merit figure definition suitable to mathematical maximization is provided:

$$\Gamma = \frac{A^a B^b}{C^c D^d} \quad (2.1)$$

where A and B are the performance factors to be maximized, whereas C and D should be minimized. The lowercase exponents (a , b , c , and d) are the corresponding weights assigned to each performance factor in the merit figure definition.

The exploration of all the design variables sets of values, searching the optimized design, is what we call the *design space exploration*.

From a mathematical standpoint, the constrained design space exploration (and the corresponding optimization) could be described as follows:

$$\text{minimize} \longrightarrow f_o(\mathbf{x}) \quad (2.2)$$

$$\text{subject to} \longrightarrow f_i(\mathbf{x}) \leq b_i \quad i = 1, \dots, m \quad (2.3)$$

With the following definitions:

$$\mathbf{x} = (x_1, x_2, \dots, x_n) \longrightarrow \text{design variables } (L, f_s, C_o) \quad (2.4)$$

$$f_o : R^n \rightarrow R \longrightarrow \text{objective function} \quad (2.5)$$

$$f_i : R^n \rightarrow R, \quad i = 1, \dots, m \longrightarrow \text{constraint functions} \quad (2.6)$$

In general, main function $f_o(\mathbf{x})$ and constraint functions $f_i(\mathbf{x})$ will be non linear (even non continuous functions), which precludes the obtention of the optimized design by means of analytical procedures.

It should be noted that with the inclusion of technological information, the design of each converter component is related to its non idealities, such as its equivalent series resistance (ESR from now on), parasitic capacitances, area occupation. Therefore, given the variables that may appear in each component design, the particular design of the several components that compose the whole converter should be optimized to improve its energy losses or area. In fact, this is one of the strongest points that the microelectronic integration of switching power converters offers: *any component can be particularly optimized for any converter design, (by the designer itself)*, instead of being already implemented by a third-party manufacturer (Fig. 2.2).

As a result of their monolithic integration, one of the performance factors to be evaluated in the design is the *occupied die area*, since it is directly related to the manufacturing cost of the system (in microelectronics, the cost of a chip is proportional to the used area of silicon). The other most important performance factor to be evaluated is the *energy efficiency* in the power conversion, since it is

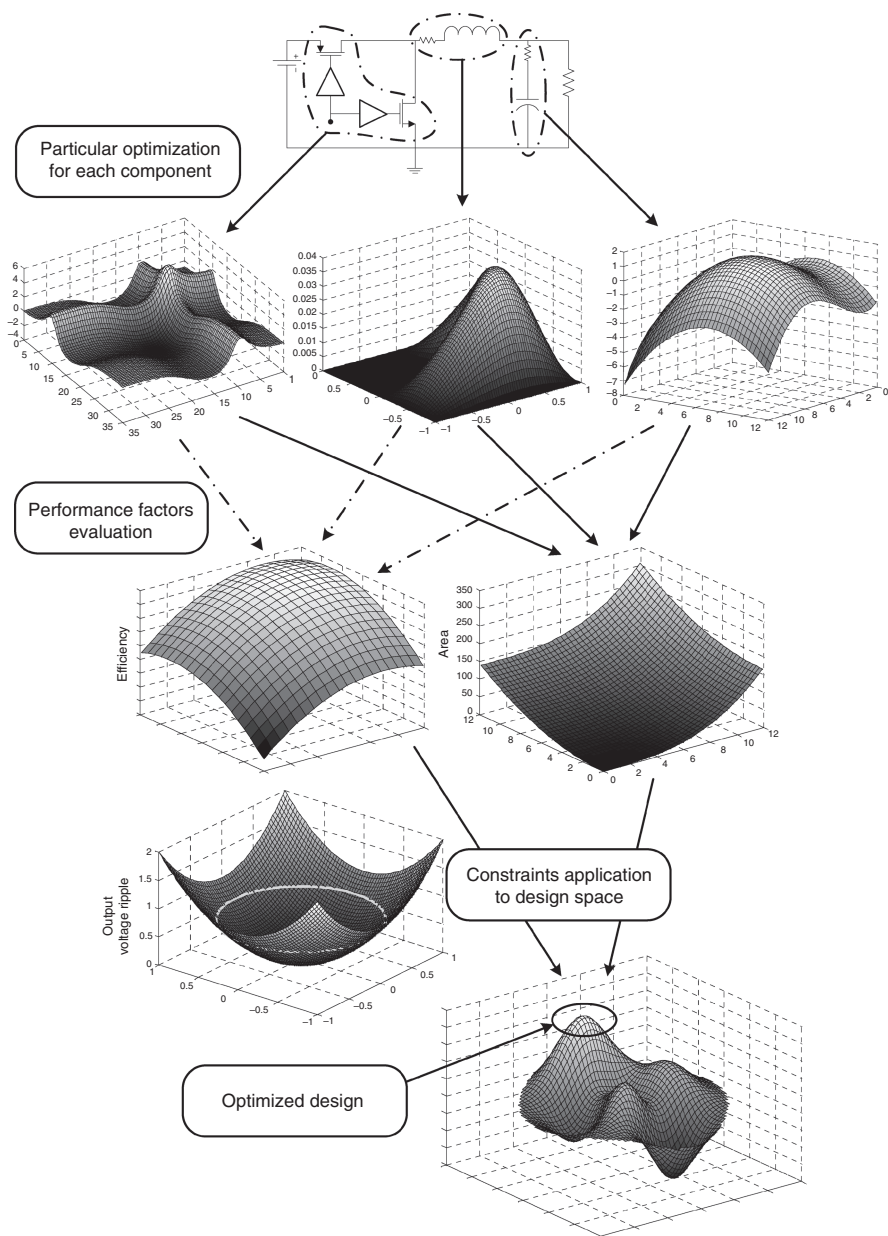


Fig. 2.2 Design space exploration by means of components particular optimizations and the corresponding performance factors evaluation

the main reason in the idea of integrating this kind of power converters and in case of standard CMOS technologies such high efficiency is not assured because those processes have not been conceived for power management applications. A second order performance factor to take into account is the *maximum inductor current*, to reduce the converter components electrical stress. Obviously, whereas energy efficiency should be maximized, occupied silicon area and maximum inductor current are desired to be minimized.

2.2 Simplified Approach for a Buck Converter

The application considered in the development of the design of this work is intended to supply energy to core digital or RF integrated circuits for portable devices, from an external energy source, mainly a Li-Ion battery (that provide a nominal voltage of 3.6 V). In fact, it would become a part of a *Powered-System On-Chip*, *PSOC*, that integrates all the required functions (or, at least, as many as possible) of the portable device, even the power conditioning system. Because of the continuously decreasing voltage supply of such core circuits in the newest technology nodes (trying to reduce power consumption and their dimensions), as an example, the power converter will be designed to supply a 1 V voltage source. Additionally, the considered nominal output current will be set to 100 mA (which is representative for applications such as power supply of portable devices: MP3 players, some parts of more complex Hand-Held devices, etc. . .).

Hence, a *conventional Buck converter* is the first topology considered to develop the design, because of its ability of reducing input to output voltage and its simplicity (which can be a very important factor to take into account when attempting to develop a fully integrated prototype).

2.2.1 Continuous and Discontinuous Conduction Modes

Most of the switching power converters can be considered to operate in two different modes depending on the evolution of the energy stored in their corresponding main inductor.

- A switching power converter is understood to work in *continuous conduction mode* (corresponding to the acronymous CCM, from now on) if its inductor current is different from zero at any time, independently of its switching phase (Fig. 2.3a).
- The *discontinuous conduction mode* (DCM from now on) appears in the converter operation if its inductor current becomes and remains zero for a given amount of time, which can range from being almost instantaneous (operation on the edge between DCM and CCM) to last for most of the switching period (Fig. 2.3b).

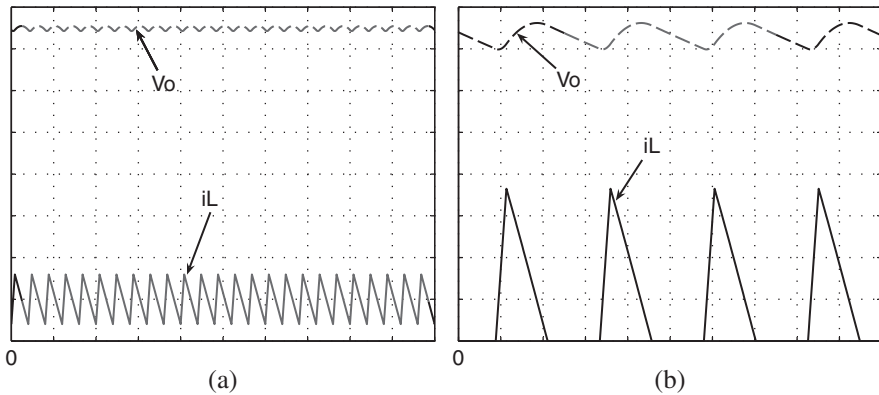


Fig. 2.3 Output voltage and inductor current ideal waveforms for a Buck converter in both operating modes: **a** CCM; **b** DCM

The previous classification becomes of capital importance when analyzing the converter behavior and its corresponding expressions, and, as it will be seen afterwards, the energy losses in each different converter component.

2.2.2 Converter Components Simplified Models

In this section models for all of the converter components are provided. Even though considered as simplified models, these are complex enough to allow the corresponding energy losses calculation as well as its area occupation. Hence, the two first steps of the design procedure proposed in Sect. 2.1 are skipped (since they are covered in detail in the literature), and some technological information is included to allow the performance factors evaluation.

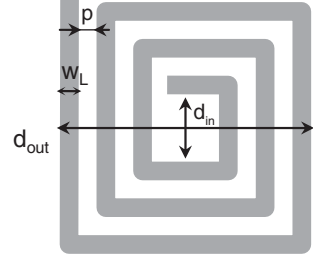
2.2.2.1 Inductor Model

The main inductor of the buck switching power converter is the most difficult component to be integrated on silicon, since in standard CMOS technologies no special materials, such as ferromagnetic cores, are available to increase the self-inductance coefficient.

In power management applications, the main requirements for the inductor design are to provide high inductive density (in order to reduce the occupied silicon area) and very low series resistance (to reduce conduction losses).

However, from the absence of a ferromagnetic core, a benefit is derived because no core magnetization hysteresis cycle appears and thereby no switching losses are present in the inductor. Additionally, no saturation in the magnetic field appears as the inductor current increases (that results in an abrupt equivalent inductance reduction).

Fig. 2.4 Square spiral inductor



The on-chip implementation by means of standard CMOS technology adds an additional constraint to the inductor design since only planar structures are possible. Therefore, a square-shaped spiral inductor is considered as a first approach design possibility (Fig. 2.4).

In [37] and [38] expressions for inductance value L and total path length l_L (related to its equivalent series resistance, R_L) of a square-shaped inductor are provided as a function of its physical dimensions: number of turns n_L , internal and external diameters (d_{in} and d_{out}), path width w_L and separation between turns p .

$$L = \frac{K_1 \mu n_L^2 d_{avg}}{1 + K_2 \rho} \quad (2.7)$$

where μ is the magnetic permeability of the material ($\mu = 4\pi \cdot 10^{-7} \text{ H/m}$, in absence of ferromagnetic materials) and K_1 and K_2 are constants derived from the data fitting procedure used to find expression (2.7) from a batch of measurements ($K_1 = 2.34$ and $K_2 = 2.75$ for a square inductor). d_{avg} is the average diameter of the spiral and ρ is defined as the *fill ratio*:

$$d_{avg} = 0.5(d_{out} + d_{in}) \quad (2.8)$$

$$d_{in} = d_{out} - 2(n_L w_L + (n_L - 1)p) \quad (2.9)$$

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \quad (2.10)$$

While the total length of the path is expressed as:

$$l_L = 4n_L d_{avg} \quad (2.11)$$

Expressions for both inductance and total path length can be obtained as a function of the outer diameter and the number of turns.

$$L = K_1 \mu n_L^2 \frac{[d_{out} - (n_L w_L + (n_L - 1)p)]^2}{d_{out} + (K_2 - 1)(n_L w_L + (n_L - 1)p)} \quad (2.12)$$

$$l_L = 4n_L d_{avg} = 4n_L [d_{dout} - (n_L w_L + (n_L - 1)p)] \quad (2.13)$$

Assuming that K_1 , K_2 , μ , w_L and p are technology-dependent constants (this assumption will be further explained afterwards, in another chapter), outer diameter and the number of turns are considered as the inductor design variables.

Because there are many (d_{out}, n_L) pairs that may result in the same value of inductance, total length becomes a function to be minimized (in order to reduce the inductor series resistance), being (d_{out}, n_L) pairs constrained to values that provide the desired L value.

n_L is selected as the independent variable because its values (number of turns of the spiral) are constrained to natural values, being the d_{out} value computed to provide the required inductance. Then, the resulting pairs (d_{out}, n_L) are used to compute the total spiral length. The resulting series resistance will depend on total path length l_L , its width w_L and thickness t_m and the conductivity of the material used to implement the inductor σ .

$$R_L = \frac{l_L}{w_L t_m \sigma} = \frac{l_L R_{\square}}{w_L} = \frac{4n_L [d_{dout} - (n_L w_L + (n_L - 1)p)]}{w_L t_m \sigma} \quad (2.14)$$

In (2.14), the symbol R_{\square} is the square-resistance of the conductor metal, which is a very common parameter provided by the foundry, in case of planar technologies. It models the resistance provided by an square of conductor, given the conductor thickness (t_m) and conductivity (σ), which are expected to be constant ($R_{\square} = \frac{1}{t_m \sigma}$).

At first sight, it appears that having assured the desired inductance value, the overall series resistance should be minimized, but an additional constraint should be considered: the total occupied silicon area (A_L), that is a square function of the outer diameter (d_{out}). Therefore, the overall area is computed and a merit figure to be maximized is defined Γ_L , particular for the inductor design itself.

$$A_L = d_{out}^2 = f(L) \quad (2.15)$$

$$\Gamma_L = \frac{1}{A_L R_L} = \frac{w_L t_m \sigma}{d_{out}^2 4n_L [d_{dout} - (n_L w_L + (n_L - 1)p)]} \quad (2.16)$$

At this point, it is reminded the dependence $d_{out} = f(L, n_L)$, that leads to the maximization of Γ_L , only as a function of the number of turns. Figure 2.5a shows the evolution of Γ_L . The resulting series resistance and the occupied silicon area for the selected design, are shown as well (Fig. 2.5b).

Having obtained the value of the inductor parasitic series resistance (2.14), the corresponding conduction losses can be determined by means of the inductor *rms* current value.

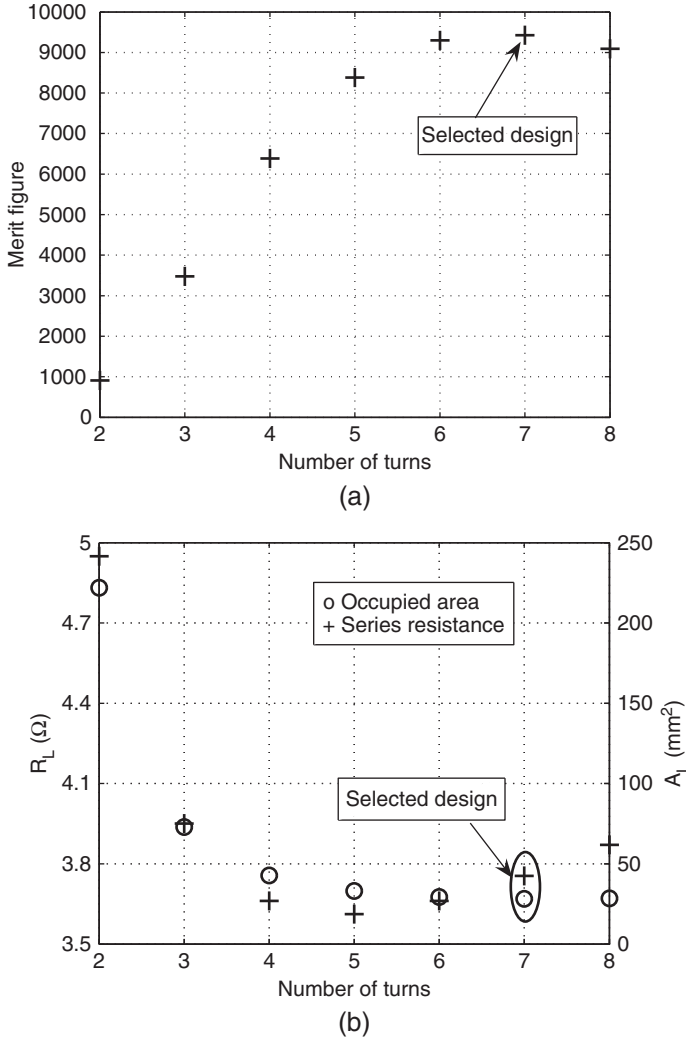


Fig. 2.5 Optimization of an square spiral inductor ($L = 150 \text{ nH}$, $p = 20 \mu\text{m}$, $w_L = 300 \mu\text{m}$): **a** merit figure; **b** series resistance and occupied area

$$I_L^2 = \sqrt{\frac{8I_o^3 V_o (V_{bat} - V_o)}{9V_{bat} L f_s}} \rightarrow DCM \quad (2.17)$$

$$I_L^2 = \frac{V_o^2 (V_{bat} - V_o)^2 V_{bat}}{12L^2 f_s^2 V_{bat}^3} + I_o^2 \rightarrow CCM \quad (2.18)$$

$$P_{L_cond} = I_L^2 R_L = f(f_s, L) \quad (2.19)$$

Therefore, as stated in (2.15) and (2.19), it is observed that the occupied area by the inductor and its corresponding power losses are a function of its self-inductance value. Additionally, power losses also depend on the converter switching frequency, being both of them design variables considered in the design space exploration.

2.2.2.2 Capacitor Model

The main requirement for the output capacitor implementation is to offer a high capacitive density, that results in a high capacitance value (to reduce to amount of output voltage ripple) while keeping reduced silicon area occupation. Moreover, to prevent reducing power efficiency and increasing output ripple it is important to get a low equivalent series resistance (ESR) design.

In order to get the highest capacitive density in planar environment, the parasitic gate capacitor of MOS transistors is used to implement the output capacitor (MOS capacitor). The main reason for this choice is that in standard CMOS technologies the gate silicon oxide is the thinnest dielectric material that can be used between both plates of the planar capacitor.

A common given parameter from a CMOS technology is the transistor gate capacitive density (C_{ox}). This is an average parameter since the MOS gate capacitor is a non-linear function of the gate voltage, but it is a good approach if the gate voltage is above the threshold voltage. Therefore, the expression of the area occupied by the MOS capacitor (A_{C_o}) is immediate, from the desired capacitor value:

$$A_{C_o} = \frac{C_o}{C_{ox}} = f(C_o) \quad (2.20)$$

In regard to the capacitor ESR (R_{C_o}), it is a function of the plates and contacts dimensions and materials resistivity. In standard CMOS technologies, the top plate of a MOS capacitor is build up by polysilicon which is quite resistive, and the bottom plate is implemented by the transistor channel, whose conductivity depends on the applied gate voltage. Additionally, it is observed that resistance of both plates is, in fact, a function of the aspect ratio rather than the area. However, in this first approach a constant value could be considered, since the total ESR can be reduced by the parallel connection of several capacitors (keeping the total capacitance value), which is a common technique in case of non-integrated designs.

Finally, from the capacitor current *rms* value (for both operating modes, continuous and discontinuous) the conduction losses associated to the capacitor are directly found:

$$I_{C_o}^2 = (I_L - I_o)^2 = \left(\sqrt[4]{\frac{8I_o^3 V_o (V_{bat} - V_o)}{9V_{bat} L f_s}} - I_o \right)^2 \longrightarrow DCM \quad (2.21)$$

$$I_{C_o}^2 = (I_L - I_o)^2 = \left(\sqrt{\frac{V_o^2 (V_{bat} - V_o)^2 V_{bat}}{12L^2 f_s^2 V_{bat}^3}} + I_o^2 - I_o \right)^2 \rightarrow CCM \quad (2.22)$$

$$P_{C_o} = I_{C_o}^2 R_{C_o} = f(L, f_s) \quad (2.23)$$

In contrast to the inductor design, the direct relation between the capacitor value and its area, as well as the relatively arbitrary and constant ESR value (in this first approach), avoid the need for an optimization procedure of the capacitor design.

Regarding the performance factors dependencies on the design variables, it is observed that the occupied area depends on the capacitance value (2.20), whereas the power losses depend on inductance and switching frequency but not on the capacitance value (provided that the capacitor ESR is independent of this design variable), as stated by (2.23).

2.2.2.3 Power Transistor Model

Power switches suffer from two different power loss mechanisms: *conduction losses* (due to the joule-effect when current flows through its parasitic non-zero channel resistance) and *switching losses* (due to the coexistence of voltage and current excursions during switching instants).

Conduction Losses

In order to derive the conduction losses for each power switch (that in case of CMOS standard technology implementation are MOSFET transistors), the parasitic on-resistance (R_{on}) expression as well as the *rms* value of the current flowing through its channel are required.

$$P_{cond} = R_{on} I_{MOS}^2 \quad (2.24)$$

Current flowing through each transistor is obtained by the corresponding expressions for the case of considering an ideal switching power converter, for the DCM operation case:

$$I_{PMOS_DCM}^2 = \sqrt{\frac{8I_o^3 V_o^3 (V_{bat} - V_o)}{9L V_{bat}^3 f_s}} \quad (2.25)$$

$$I_{NMOS_DCM}^2 = \sqrt{\frac{8I_o^3 V_o (V_{bat} - V_o)^3}{9L V_{bat}^3 f_s}} \quad (2.26)$$

And for the CCM:

$$I_{PMOS_CCM}^2 = \frac{V_o^3 (V_{bat} - V_o)^2}{12L^2 V_{bat}^3 f_s^2} + I_o^2 \frac{V_o}{V_{bat}} \quad (2.27)$$

$$I_{NMOS_CCM}^2 = \frac{V_o^2 (V_{bat} - V_o)^3}{12L^2 V_{bat}^3 f_s^2} + I_o^2 \frac{V_{bat} - V_o}{V_{bat}} \quad (2.28)$$

As stated in (2.29), in a first order approach, the on-resistance of a MOS switch depends on the corresponding channel size (L_{ch} , W_{power_MOS} for length and width, respectively), the voltage-to-source voltage (V_{gs}) and technology dependent constants: threshold voltage ($V_{TN/P}$), gate capacitance-per-area (C_{ox}) and carriers mobility ($\mu_{N/P}$). Typically, threshold voltage and carriers mobility will take different values for PMOS and NMOS transistors.

$$R_{on} = \frac{L_{ch}}{\mu_{N/P} C_{ox} W_{power_MOS} (V_{gs} - V_{TN/P})} \quad (2.29)$$

Since in the case of a buck converter implementation maximum available voltage-to-source corresponds to the input battery voltage (V_{bat} , for a battery operated system) when sources are properly connected to supply voltages, this should be used to drive the MOS switches gate (to minimize the corresponding on-resistance), resulting in the following expression:

$$R_{on} = \frac{L_{min}}{\mu_{N/P} C_{ox} W_{power_MOS} (V_{bat} - V_{TN/P})} \quad (2.30)$$

being L_{min} the minimum channel length available in a certain technological micro-electronic process, to reduce the on-resistance, and the parasitic capacitances as well.

From (2.29) and (2.30) it is derived that conduction losses in a power MOSFET become an inverse function of its channel width.

Switching Losses

Switching losses computation is addressed by means of the product of the voltage across the channel (between transistor drain and source) and the current flowing through it. In order to simplify the model, linear evolutions for both voltage and current are assumed during switching actions, as it can be seen in Fig. 2.6, as well as the corresponding instantaneous power evolution.

In order to obtain the total energy spent in each commutation, instantaneous power has to be integrated along the commutation interval (shaded area in Fig. 2.6).

$$E_{sw} = \frac{I_{on} V_{on} t_{sw_on}}{6} + \frac{I_{off} V_{off} t_{sw_off}}{6} \quad (2.31)$$

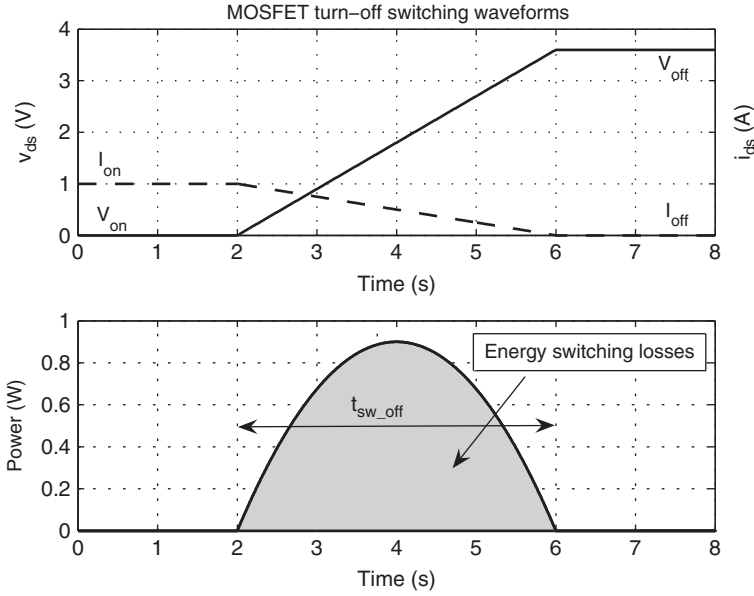


Fig. 2.6 First order approach of channel voltage and current, and instantaneous power evolution along the commutation of a power transistor

Consequently, power switching losses are obtained from energy losses and the switching frequency.

$$P_{sw} = f_s \left(\frac{I_{on} V_{on} t_{sw_on}}{6} + \frac{I_{off} V_{off} t_{sw_off}}{6} \right) \quad (2.32)$$

In (2.31) and (2.32), variables I_{on} , V_{on} and t_{sw_on} are the current and voltage swings applied to the MOS transistor when turning it on, and the corresponding duration; whereas the second terms of those expressions are referred to the turning off action.

Table 2.2 collects the expressions corresponding to the voltage and current conditions applied to both power transistors, for DCM and CCM.

While V_{on} and I_{on} depend on the converter design and operation, the $t_{sw_on/off}$ values depend on the transistor and driver design. As a first order approach, state transition duration of a MOS power switch can be estimated assuming that its gate voltage evolution corresponds to the gate capacitance charge/discharge process through the equivalent resistance of the driver last stage. In this case, a 3-time-constants criterion can be used to determine the duration of the total change in the gate voltage.

$$t_{sw} = 3R_{driver}C_{gate} = 3R_{driver}C_{ox}W_{power_MOS}L_{min} \quad (2.33)$$

Table 2.2 Transistor switching conditions for DCM and CCM operation

DCM	PMOS	NMOS
V_{on}	$V_{bat} - V_o$	V_{bat}
I_{on}	0	$I_{Lmax} = \sqrt{\frac{2I_o V_o (V_{bat} - V_o)}{L f_s V_{bat}}}$
V_{off}	V_{bat}	V_o
I_{off}	$I_{Lmax} = \sqrt{\frac{2I_o V_o (V_{bat} - V_o)}{L f_s V_{bat}}}$	0
CCM	PMOS	NMOS
V_{on}	V_{bat}	V_{bat}
I_{on}	$I_{Lmin} = I_o - \frac{V_o (V_{bat} - V_o)}{2L V_{bat} f_s}$	$I_{Lmax} = I_o + \frac{V_o (V_{bat} - V_o)}{2L V_{bat} f_s}$
V_{off}	V_{bat}	V_{bat}
I_{off}	$I_{Lmax} = I_o + \frac{V_o (V_{bat} - V_o)}{2L V_{bat} f_s}$	$I_{Lmin} = I_o - \frac{V_o (V_{bat} - V_o)}{2L V_{bat} f_s}$

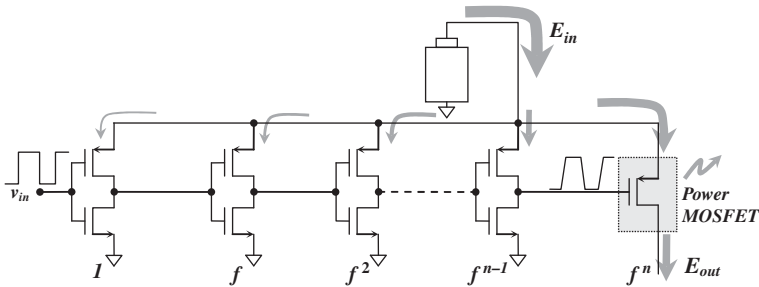
Hence, at this point of the analysis, it is observed from (2.32) and (2.33) that switching losses become a direct function of the MOS transistor channel width. The value of equivalent driver output resistance will be derived in the following Sect. 2.2.2.4, which deals with the driver design issues.

To finish the power switch model, their corresponding occupied silicon area is computed as a function of their gate dimensions.

$$A_{MOS} = W_{power_MOS} L_{min} \quad (2.34)$$

2.2.2.4 Power Driver Design and Loss Model

A power driver is required to amplify the power of the switching signal when it has to drive the power MOSFET gate input capacitance (which usually is rather large), if a fast gate state transition is desired. In standard CMOS technology implementations the most usual way to implement a bi-state power driver is by means of a tapered buffer (Fig. 2.7), which consists of a chain of digital inverters; being the transistors of each stage larger than those from the previous by a tapering factor f .

**Fig. 2.7** Power driver implementation by means of tapered buffers

Given the size of the transistor of a minimum digital inverter (or its equivalent input capacitance), that should be the first of the tapered buffer, and the size of the power MOSFET to be driven (or its equivalent input capacitance), two different variables are available to design the tapered buffer: the number of inverters n and the tapering factor. Usually, tapered buffer designs with a constant tapering factor are implemented, and then the relationship between the tapering factor and the number of stages is as follows:

$$f = \sqrt[n]{\frac{C_{out}}{C_{in}}} \quad (2.35)$$

where C_{out} is the power MOSFET gate capacitance and C_{in} is the minimum inverter capacitance.

Typically, in digital microelectronics research fields, the tapering factor has been determined targeting the overall propagation delay minimization, and it has been found the number e to be the optimum one. Having determined the optimum tapering factor, the number of stages is directly derived from the input-to-output capacitance ratio.

$$n = \ln \left(\frac{W_{power_MOS}}{(1 + w_{pn})W_{min}} \right) \quad (2.36)$$

being W_{min} the channel width of the NMOS transistor of the first inverter, and w_{pn} the relationship between the channel width of PMOS and NMOS transistor of each inverter. In (2.36) it is supposed that transistors from inverters, as well as the power MOS, have minimum channel length, to increase switching speed and reduce parasitic resistance.

Having determined the tapering factor and the number of stages of the whole tapered buffer, the equivalent output resistance that charges and discharges the power MOS gate capacitance can be obtained (R_{driver}), through the channel width of the NMOS transistor of the last driver stage (W_{n_driver}).

$$W_{n_driver} = W_{min}e^{n-1} = \frac{W_{power_MOS}}{(1 + w_{pn})e} \quad (2.37)$$

$$\begin{aligned} R_{driver} &= \frac{L_{min}}{\mu_N C_{ox} W_{n_driver} (V_{bat} - V_{TN})} = \\ &= \frac{(1 + w_{pn})e L_{min}}{\mu_N C_{ox} W_{power_MOS} (V_{bat} - V_{TN})} \end{aligned} \quad (2.38)$$

In Addition to the driver output resistance, its own losses must be modeled in order to include them into the design space exploration, as a part of the overall efficiency.

In case of a tapered buffer, power losses are mainly due to its state change at every switching period. As a first order approach, power losses are computed by means of the charge spent from the power supply to change the value of the respective input gate capacitances of all inverters of the chain.

As a consequence, the total gate capacitance (C_T) should be computed as a function of the number of stages and the tapering factor:

$$C_T = \sum_{i=0}^n C_i = (1 + w_{pn})C_{ox}W_{min}L_{min} \sum_{i=0}^n f^i \quad (2.39)$$

$$\sum_{i=0}^n f^i = \frac{f^{n+1} - 1}{f - 1} \quad (2.40)$$

being e the optimum tapering factor:

$$C_T = (1 + w_{pn})C_{ox}W_{min}L_{min} \frac{e^{n+1} - 1}{e - 1} \quad (2.41)$$

And the corresponding power losses are related to the power supply voltage and the switching frequency by:

$$P_{driver} = V_{bat}^2 f_s (1 + w_{pn})C_{ox}W_{min}L_{min} \frac{e^{n+1} - 1}{e - 1} \quad (2.42)$$

From (2.42) it is observed the driver switching losses increase with the number of inverters that, in turn, is an increasing function of the power transistor channel width. Thus, it is concluded that power driver losses are a linear function of the power MOSFET channel width.

$$P_{driver} = V_{bat}^2 f_s (1 + w_{pn})C_{ox}W_{min}L_{min} \frac{e^{\frac{W_{power_MOS}}{(1+w_{pn})W_{min}}} - 1}{e - 1} \quad (2.43)$$

$$P_{driver} = V_{bat}^2 f_s C_{ox}L_{min} \frac{e^{W_{power_MOS} - (1 + w_{pn})W_{min}}}{e - 1} \quad (2.44)$$

On the other hand, the overall occupied silicon area can be computed directly from the total gate capacitance of the tapered buffer if only channel dimensions are considered.

$$A_{driver} = L_{min} \frac{e^{W_{power_MOS} - (1 + w_{pn})W_{min}}}{e - 1} \quad (2.45)$$

2.2.2.5 Power MOSFET and Driver Joint Design

In previous Sects. 2.2.2.3 and 2.2.2.4 power losses were derived as a function of the power MOSFET channel width. Conduction losses of MOS switch were found to be a decreasing of the channel width, whereas switching losses depend not only on the power switch channel width but on the driver output resistance.

Since output driver resistance was determined in expression (2.38), a closed analytical expression can be found for power MOSFET switching losses, by means of the switching action duration definition.

In the case in which the equivalent driver output resistance for both charge and discharge output capacitance were the same (that can be achieved if a proper relationship between PMOS and NMOS transistor channel width is selected, for the tapered buffer inverters), the duration on the two complementary actions on the power switch would be the same.

$$t_{sw_on/off} = \frac{3(1 + w_{pn})eL_{min}^2}{\mu_N(V_{bat} - V_{TN})} \quad (2.46)$$

Which results in the following switching power losses expression:

$$P_{sw} = \frac{(1 + w_{pn})eL_{min}^2}{2\mu_N(V_{bat} - V_{TN})} (V_{on}I_{on} + V_{off}I_{off}) f_s \quad (2.47)$$

From (2.47) it is observed that *switching power losses from the power MOSFET become independent of its channel width*, as long as the corresponding driver design becomes adapted to it.

And finally, from (2.44) it is observed that driver power losses are a direct linear function of the power MOSFET channel width.

In Table 2.3, the expressions of the three different power loss mechanisms related to the power switches and their corresponding trends as W_{power_MOS} increase are summarized.

Since there are two opposed trends, an optimum design that provides minimum power losses is expected as a function of the power transistor channel width, as shown in the following figure (corresponding to a PMOS design and its associated driver) (Fig. 2.8).

In the following, expressions for the optimum channel width value, and the resulting minimum power losses are provided:

Table 2.3 Power loss expressions and trends for the MOSFET and driver designs

Loss source	Expression	Trend (as W_{power_MOS} increases)
Power MOS conduction losses	$P_{cond} = \frac{L_{min}}{\mu_{N/P} C_{ox} W_{power_MOS} (V_{bat} - V_{TN/P})} I_{MOS}^2$	$\downarrow\downarrow$
Power MOS switching losses	$P_{sw} = \frac{(1 + w_{pn})eL_{min}^2}{2\mu_N(V_{bat} - V_{TN})} (V_{on}I_{on} + V_{off}I_{off}) f_s$	Constant
Driver losses	$P_{driver} = V_{bat}^2 f_s C_{ox} L_{min} \frac{eW_{power_MOS} - (1 + w_{pn})W_{min}}{e - 1}$	$\uparrow\uparrow$

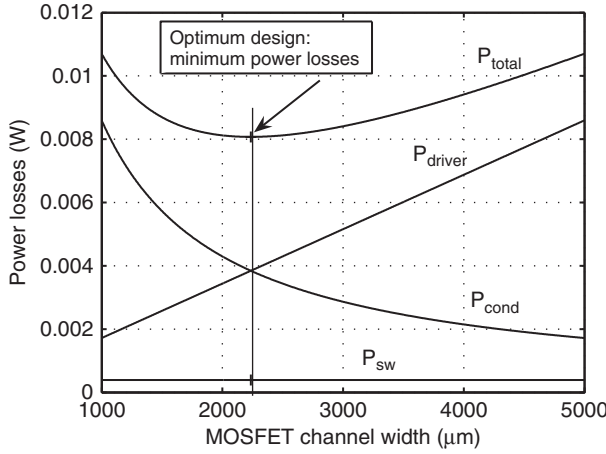


Fig. 2.8 Power MOSFET and driver power losses as a function of the power MOSFET channel width

$$W_{opt} = \frac{I_{MOS}}{V_{bat} C_{ox}} \sqrt{\frac{e - 1}{\mu_{N/P} f_s e (V_{bat} - V_{TN/P})}} \quad (2.48)$$

$$\begin{aligned} P_{MOS+driver} = & f_s (1 + w_{pn}) L_{min} \\ & \left(\frac{e L_{min}}{2 \mu_{N/P} (V_{bat} - V_{TN})} (V_{on} I_{on} + V_{off} I_{off}) - C_{ox} V_{bat}^2 \frac{W_{min}}{e - 1} \right) + \\ & + 2 I_{MOS} V_{bat} L_{min} \sqrt{\frac{f_s e}{\mu_{N/P} (e - 1) (V_{bat} - V_{TN/P})}} \end{aligned} \quad (2.49)$$

2.2.3 Output Voltage Ripple

Once the converter topology has been selected to fulfill some of the application parameters herein considered (mainly, input voltage to output voltage conversion ratio), there is still an application parameter to take into account to yield the desired design. This is the *output voltage ripple*, that becomes a hard constraint of the design space, since any design variables set of values (L , f_s , C_o) that results in an output voltage ripple greater than the one tolerated by the load circuitry to be supplied, will be neglected.

Typically, the output voltage ripple Δv_o is defined as the difference between the maximum and minimum values that the output voltage takes throughout a whole switching period.

$$\Delta v_o = V_{o_max} - V_{o_min} \quad (2.50)$$

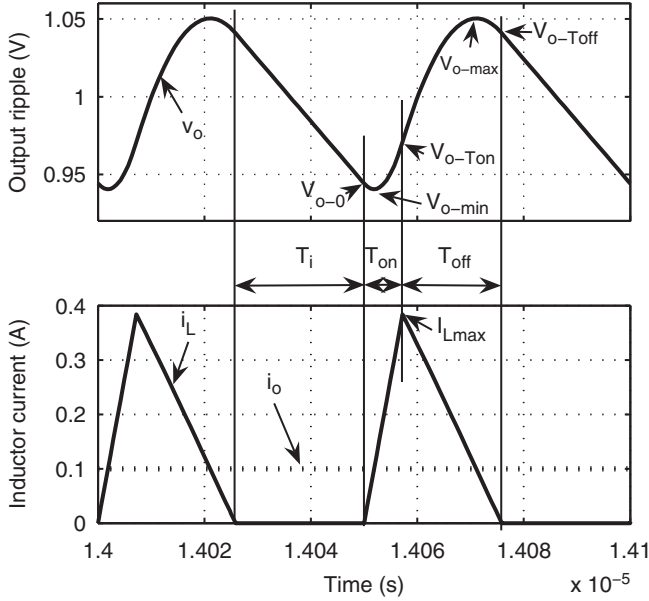


Fig. 2.9 Output voltage and inductor current in a DCM operated Buck converter. Different phases of a switching period are detailed

Figures 2.9 and 2.10 explicitly show these values for DCM and CCM operation. Additionally, other significant and useful characteristics of the output voltage and inductor current waveforms for both operating modes are also noted.

The corresponding expressions for V_{o-max} and V_{o-min} are obtained from the low output ripple assumption, which implies that inductor current correspond to a piecewise linear function. According to the scheme from Fig. 2.11, the output voltage generic expression for both operating modes and different phases that compose a whole switching cycle, is the following.

$$v_o = i_{C_o} R_{C_o} + \frac{1}{C_o} \int i_{C_o} dt = (i_L - I_o) R_{C_o} + \frac{1}{C_o} \int i_L dt - \frac{I_o}{C_o} + V_{C_o,0} \quad (2.51)$$

where $V_{C_o,0}$ is the output capacitor voltage (without ESR) at the beginning of the T_{on} phase.

Taking into account different i_L expressions for any operating mode and switching phase, (2.2.3) is minimized or maximized accordingly to minimum or maximum research.

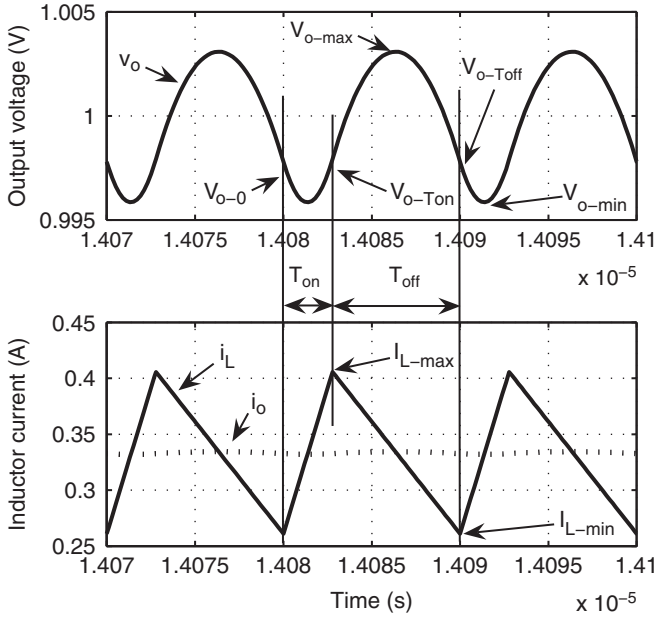
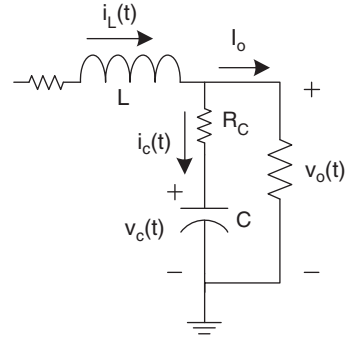


Fig. 2.10 Output voltage and inductor current in a CCM operated Buck converter. Different phases of a switching period are detailed

Fig. 2.11 Buck converter output circuit



In case of DCM, the expressions for V_{o_max} and V_{o_min} are:

$$V_{o_max} = \frac{[(I_{L_max} - I_o)L - R_{C_o}C_oV_o]^2}{2LC_oV_o} + \frac{V_{bat} - V_o}{2LC_o}T_{on}^2 + \frac{(V_{bat} - V_o)R_{C_o}C_o - I_oL}{LC_o}T_{on} - I_oR_{C_o} + V_{C_o_0} \quad (2.52)$$

$$V_{o_min} = V_{C_o_0} - I_oR_{C_o} - \frac{[I_oL - R_{C_o}C_o(V_{bat} - V_o)]^2}{2LC_o(V_{bat} - V_o)} \quad (2.53)$$

But the following constraints must be considered:

$$R_{C_o} > \frac{(I_{L_max} - I_o)L}{V_o C_o} \longrightarrow V_{o_max} = v_o(T_{on}) = \frac{V_{bat} - V_o}{2LC_o} T_{on}^2 + \frac{(V_{bat} - V_o)R_{C_o}C_o - I_oL}{LC_o} T_{on} - I_oR_{C_o} + V_{C_{o_0}} \quad (2.54)$$

$$R_{C_o} > \frac{I_oL}{(V_{bat} - V_o)C_o} \longrightarrow V_{o_min} = v_o(0) = V_{C_{o_0}} - I_oR_{C_o} \quad (2.55)$$

In expressions from (2.52), (2.53), (2.54) and (2.55) T_{on} and I_{L_max} correspond to the T_{on} phase duration and the maximum inductor current (see Fig. 2.9), respectively (for DCM operation).

$$I_{L_max} = \sqrt{\frac{2I_oV_oL}{V_{bat}f_s(V_{bat} - V_o)}} \quad (2.56)$$

$$T_{on} = \sqrt{\frac{2I_oV_o(V_{bat} - V_o)}{V_{bat}f_sL}} \quad (2.57)$$

When the CCM operation is considered the expressions for the boundary values of output ripple are as follows:

$$V_{o_max} = \frac{V_o[(V_{bat} - V_o)^2 + (2V_{bat}R_{C_o}C_of_s)^2]}{8LC_oV_{bat}^2f_s^2} + V_{C_{o_0}} \quad (2.58)$$

$$V_{o_min} = V_{C_{o_0}} - \frac{V_{bat} - V_o}{2LC_o} \left[R_{C_o}^2 C_o^2 + \left(\frac{V_o}{2V_{bat}f_s} \right)^2 \right] \quad (2.59)$$

And the corresponding constraints to be taken into account are:

$$R_{C_o} > \frac{V_{bat} - V_o}{2V_{bat}C_of_s} \rightarrow V_{o_max} = v_o(T_{on}) = \frac{(V_{bat} - V_o)V_oR_{C_o}}{2Lf_sV_{bat}} + V_{C_{o_0}} \quad (2.60)$$

$$R_{C_o} > \frac{V_o}{2V_{bat}C_of_s} \rightarrow V_{o_min} = v_o(0) = V_{C_{o_0}} - \frac{(V_{bat} - V_o)V_o}{2LV_{bat}f_s}R_{C_o} \quad (2.61)$$

All the V_{o_max} and V_{o_min} previous expressions, contain the initial voltage of output capacitor ($V_{C_{o_0}}$), which is directly related to the average converter output voltage. It is important to note that for ripple calculation purposes, this value is not necessary because just the difference between both values is required.

Moreover, in both cases (DCM and CCM), the obtained expressions are subject to some constraints depending on the R_{C_o} value. This results from the fact that the minimization or maximization of (2.2.3) is limited to T_{on} and T_{off} phases, respectively. Nevertheless, under some circumstances (stated by inequalities related to R_{C_o}), the minimum or maximum of such parabolic sections, could be somewhere

outside those boundaries. In these cases, minimum and maximum output voltage becomes the output voltage at the beginning of the corresponding switching phase.

In summary, this is the reason that precludes the existence of a closed analytical expression for the output voltage ripple.

Figure 2.12 shows good matching between the proposed expressions for output ripple calculation (as a function of the capacitor resistance) and some simulation results, for both operating modes: DCM ($V_o = 1\text{ V}$, $V_{bat} = 3.6\text{ V}$,

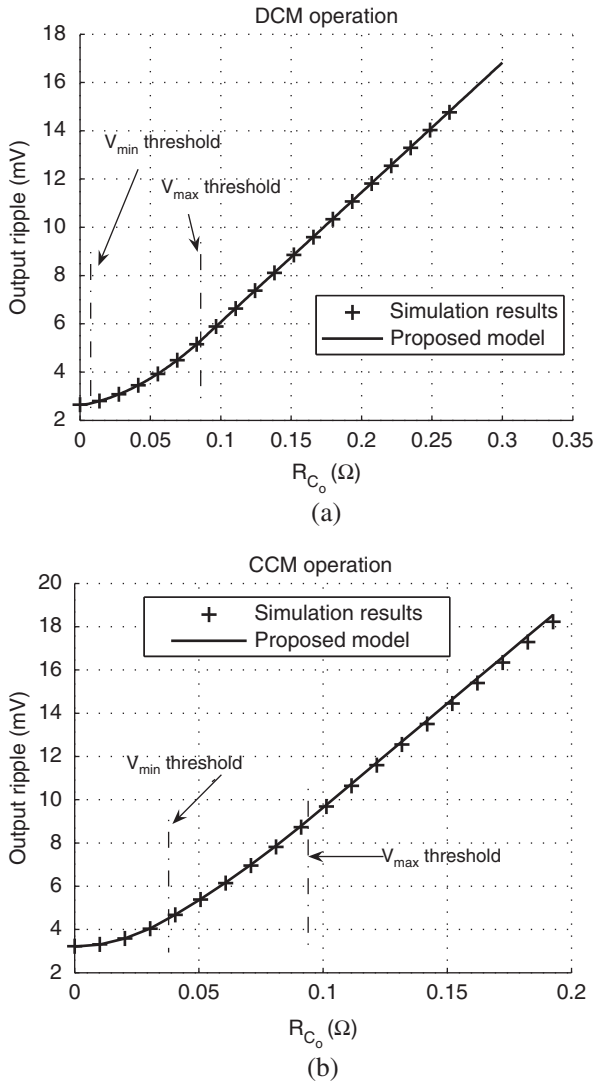


Fig. 2.12 Output ripple prediction as a function of R_{C_o} , contrasted with some simulation results, for DCM **a** and CCM **b**

$L = 50 \text{ nH}$, $C_o = 25 \text{ nF}$, $f_s = 100 \text{ MHz}$, $I_o = 10 \text{ mA}$) and CCM ($V_o = 1 \text{ V}$, $V_{bat} = 3.6 \text{ V}$, $L = 50 \text{ nH}$, $C_o = 25 \text{ nF}$, $f_s = 150 \text{ MHz}$, $I_o = 100 \text{ mA}$). In this figure, threshold values for R_{C_o} exposing the constraints from (2.54), (2.55), (2.60) and (2.61) are marked with vertical lines. It is interesting to note that these constraints (and the corresponding change in calculation expressions) appear for low R_{C_o} values.

However, it should be taken into account that as a the load resistance value becomes lower (and closer to the R_{C_o}), little error occurs on ripple prediction.

2.2.4 Design Space Exploration Results

In the previous sections, all the converter components have been modeled towards the selected performance factors evaluation (power efficiency and occupied area) and application parameters (output voltage ripple). At this point, with the information provided from such models, the design space exploration is carried on by means of the power efficiency evaluation.

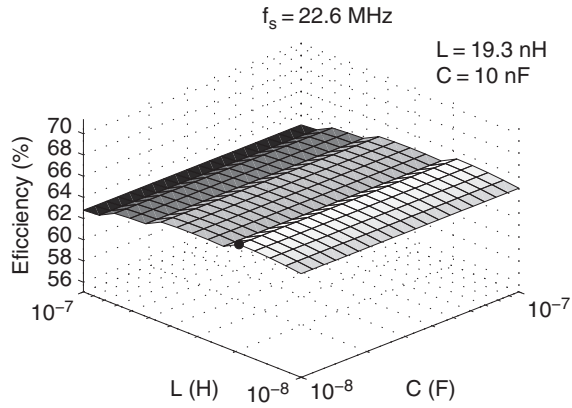
$$\begin{aligned} \eta(\%) &= \frac{P_{out}}{P_{out} + P_{losses}} 100 = \\ &= \frac{V_o I_o}{V_o I_o + P_{NMOS+driv} + P_{PMOS+driv} + P_{C_o} + P_{L_{cond}}} 100 \quad (2.62) \end{aligned}$$

In Table 2.4, all the required technological information to evaluate the design performance factors, can be found (which correspond to a representative standard CMOS $0.25 \mu\text{m}$ process).

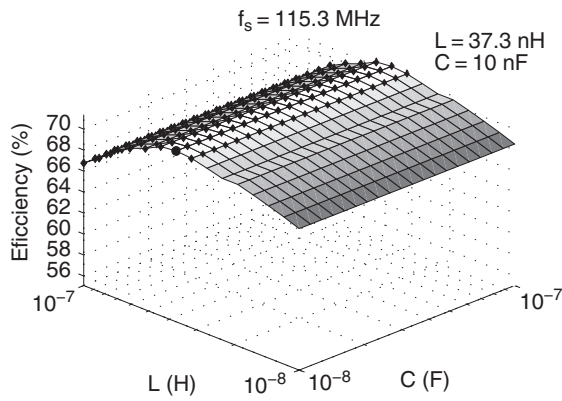
Expression (2.62) generates the results depicted in Fig. 2.13, which expose 3 different 3D surfaces since the function to be represented is a fourth dimensional one (efficiency plus the 3 design variables). Therefore, efficiency as a function of L

Table 2.4 Technological parameters information required to develop the design space exploration

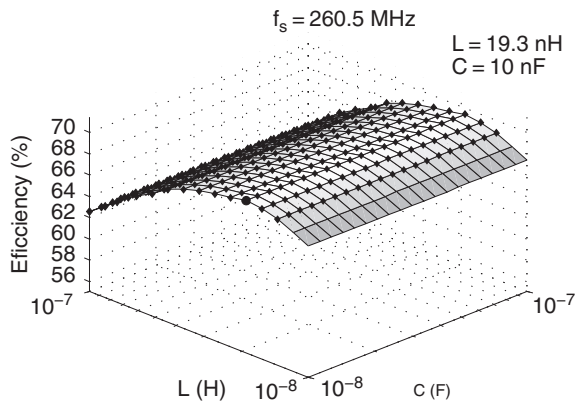
Component	Technological parameter	Value
Inductor	R_{\square}	$13 \text{ m}\Omega/\square$
	μ	$4\pi 10^{-7} \text{ H/m}$
	w_L	$300 \mu\text{m}$
	p	$20 \mu\text{m}$
Capacitor	R_{C_o}	$50 \text{ m}\Omega$
	C_{ox}	$4.933 \text{ fF}/\mu\text{m}^2$
Power MOSFETs	W_{min}	$0.3 \mu\text{m}$
	L_{min}	$0.34 \mu\text{m}$
	μ_n	$393.8 \times 10^8 \mu\text{m}^2/(\text{sV})$
	μ_p	$89 \times 10^8 \mu\text{m}^2/(\text{sV})$
	V_{TP}	0.65 V
	V_{TN}	0.55 V



(a)



(b)



(c)

Fig. 2.13 Buck converter power efficiency: **a** $f_s = 22.6 \text{ MHz}$; **b** $f_s = 115.3 \text{ MHz}$; **c** $f_s = 260.5 \text{ MHz}$

and C_o is depicted, and all figures correspond to a switching frequency single value. In the center figure the maximum power efficiency is achieved.

In Fig. 2.13 a black dot is depicted to mark, in the (L, C_o) plane, the design that provides the maximum efficiency, whereas black diamonds are used to mark all the designs that will result in CCM operation for the considered output current (100 mA).

As expected, it is observed that power efficiency is a function of inductor and switching frequency values, whereas it becomes constant against changes in output capacitor value, since no relationship between C_o and R_{C_o} have been considered in this simplified case (despite just one dot is depicted, any row with C_o constant results in the same power efficiency).

In fact, due to this particularity power efficiency is represented as a function of f_s and L in Fig. 2.14, where the maximum efficiency is better observed.

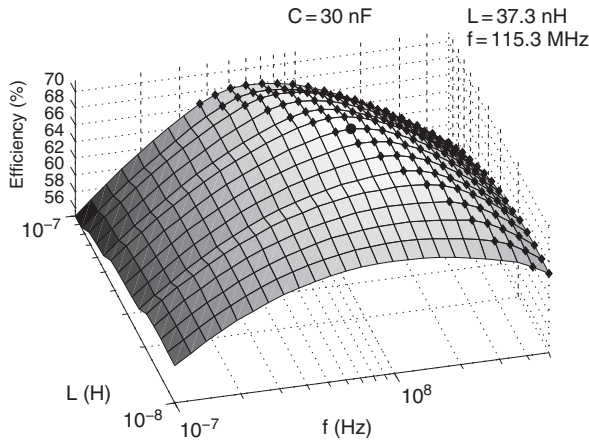


Fig. 2.14 Buck converter power efficiency in the (f_s, L) plane ($C_o = 30$ nF)

Since conduction mode is independent of the output capacitor (if low output ripple is assumed), as the power efficiency, Fig. 2.14 shows all the design solutions that will produce CCM operation (marked with black diamonds).

As far as occupied area (2.64) is concerned, the same kind of figures are presented in Fig. 2.15. It is noted that the area variation with f_s is insignificant. The reason for this is that the total converter area depends most on the inductor and capacitor values (which are independent of switching frequency). Only the power MOSFETs and their corresponding drivers design are frequency dependent, but its impact on the overall area is negligible. Additionally, in the 3 depicted cases, it is clearly observed how, as the switching frequency is increased, more designs become CCM operated.

Following the obtention of both considered performance factors (total area occupied and power efficiency), the merit figure to be maximized can now be defined (equivalent to $f_o(x)$, exposed in (2.2)).

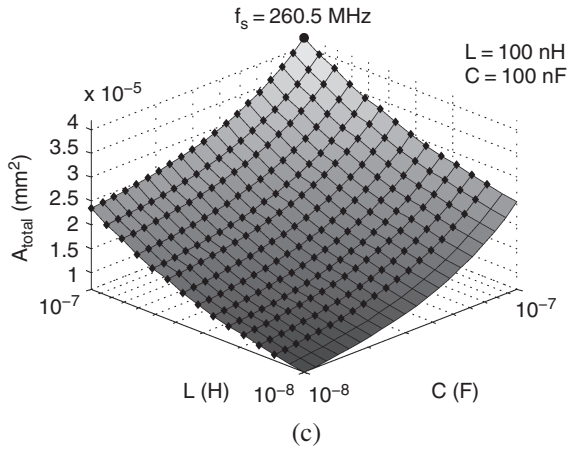
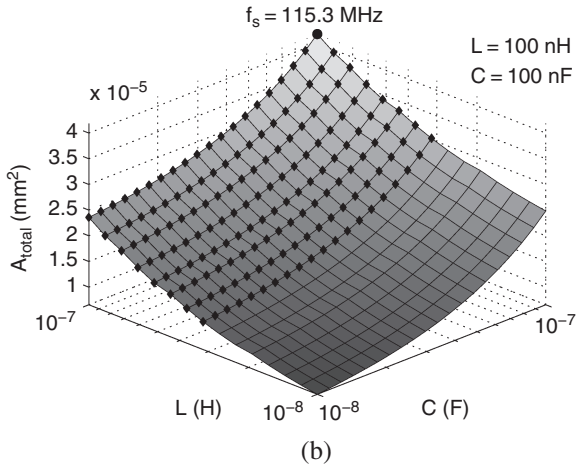
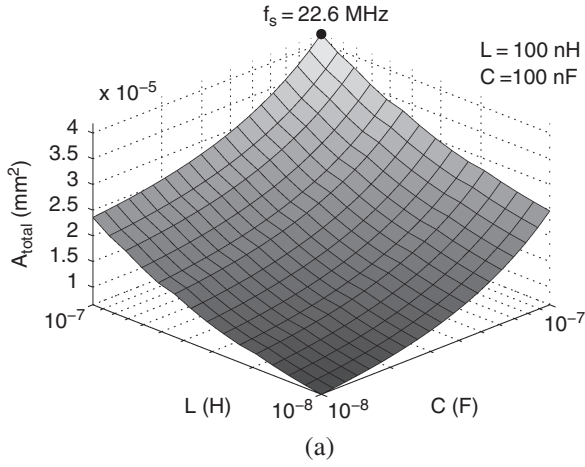


Fig. 2.15 Buck converter occupied area: **a** $f_s = 22.6 \text{ MHz}$; **b** $f_s = 115.3 \text{ MHz}$; **c** $f_s = 260.5 \text{ MHz}$

$$\Gamma = \frac{\eta(\%) - \eta_{min}(\%)}{A_{total}} \quad (2.63)$$

$$A_{total} = A_L + A_{C_o} + A_{PMOS} + A_{NMOS} + A_{driverN} + A_{driverP} \quad (2.64)$$

In (2.63), the minimum obtained power efficiency is subtracted from the rest of the power efficiency values as a way to increase the effect of its span, because of its relatively narrow range (from 54.5 to 71.4%).

Figure 2.16 is a volumetric representation of the (2.63) results, where the darker the painted area is, the higher the merit figure value becomes. It is just intended to be a qualitative representation revealing the existence of a single maximum (corresponding to an optimized design), and, approximately, where it is obtained (in terms of the coordinates (L, C_o, f_s)). Due to difficulties of volumetric representation, several slices are depicted on all axis, as well as a 3-dimensional contour around the maximum value.

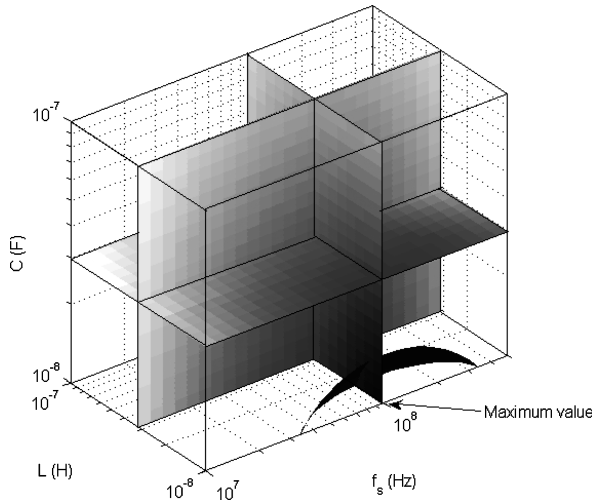


Fig. 2.16 Volumetric representation of the design merit figure as a function of the 3 design variables (L, C_o, f_s) . In the figure, the *darker area* is, the higher the merit figure value becomes

Figure 2.17 shows 3 different surfaces where the merit figure is exposed as a function of inductor and capacitor values for 3 different f_s values, respectively (the picture in the middle corresponds to the optimum switching frequency $f_s = 98$ MHz).

As observed, the maximum merit figure value is obtained when minimum inductor and capacitor are applied, because this greatly reduces the occupied area, whereas the optimum switching frequency is the one that increases power efficiency. Table 2.5 summarizes the main characteristics of this optimized design.

Apparently, an optimized design (in terms of performance factors) has been obtained, but there is still a constraint to be taken into account. It could be possible that the obtained design results in an output ripple higher than the maximum

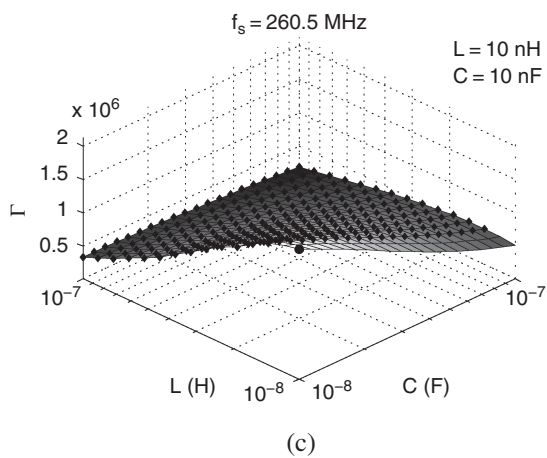
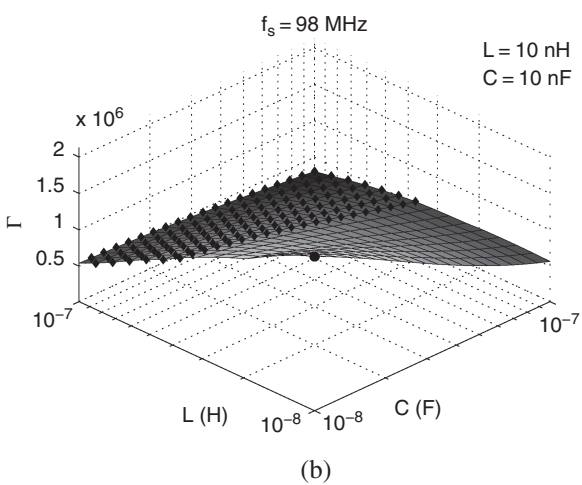
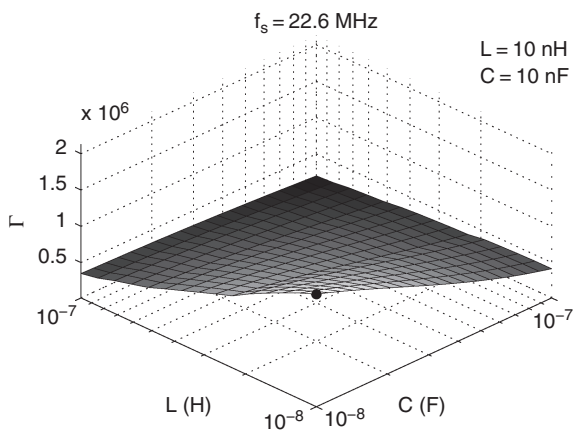


Fig. 2.17 Merit figure representation, from (2.63): **a** $f_s = 22.6 \text{ MHz}$; **b** $f_s = 98 \text{ MHz}$; **c** $f_s = 260.5 \text{ MHz}$

Table 2.5 Main characteristics of the optimized design before the application of the output ripple constraint

Variable	Value
Battery voltage	3.6 V
Output voltage	1 V
Output current	100 mA
Inductor (L)	10 nH
Capacitor (C_o)	10 nF
Switching frequency (f_s)	98 MHz
Total Area	6.59 mm ²
Power efficiency	68.6%
Output voltage ripple	60.2 mV

allowed by the considered application, specially if minimum inductor and capacitor are implemented.

Consequently, the following step is to evaluate the output voltage ripple, and observe how the design space is constrained by those designs that result in an output ripple higher than the maximum allowed by the load circuitry (in this work, the maximum allowed is 50 mV).

Thus, using expressions from Sect. 2.2.3 the output voltage ripple produced by any considered design is calculated and represented in Fig. 2.18. Again, 3 different figures are shown, corresponding to the 3 different switching frequency single values (22.6 MHz, 98 MHz, 260.5 MHz). In this case, it is also marked the maximum allowed ripple by means of a contour line (black solid line). Additionally, a black dot is used to mark the design that results in maximum ripple for each switching frequency value, as well as black diamonds are used to mark the CCM operated designs.

As it would be expected, maximum output ripple is produced when minimum L and C_o values are implemented. It is important to note that in case of $f_s = 98$ MHz output ripple is almost not a constraint of the (L, C_o) plane, and furthermore, for $f_s = 260.5$ MHz (Fig. 2.18c), it is no more a constraint (obviously, the overall design space is already constrained by the high switching frequency values).

In Fig. 2.19, a 2-dimensional view of the design space reduction is shown by means of a family of isolines (corresponding to different f_s values), that shrink down the possible designs area as the switching frequency becomes lower.

Applying the output voltage ripple constraint, power efficiency is depicted again in Fig. 2.20, as well as the total area in Fig. 2.21.

As expected from Fig. 2.19 the (L, C_o) design space is strongly constraint for low switching frequencies (e.g. $f_s = 22.6$ MHz), while it becomes in a minor reduction for $f_s = 98$ MHz or even unchanged at higher switching frequency.

Nevertheless, the output ripple constraint modifies the localization of the optimized design: Fig. 2.22 repeats the merit figure results exposed in Fig. 2.17, but this time the design space have been reduced, and the previous optimized design is not feasible since it produces an unacceptable output ripple. Please note that in Fig. 2.22, axis orientation has been rotated by 180° to increase the constraint effect visibility.

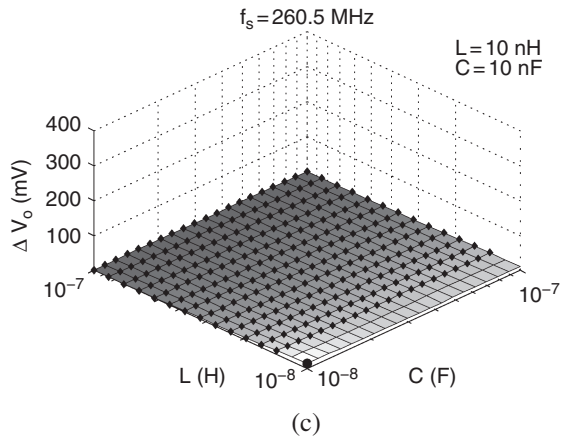
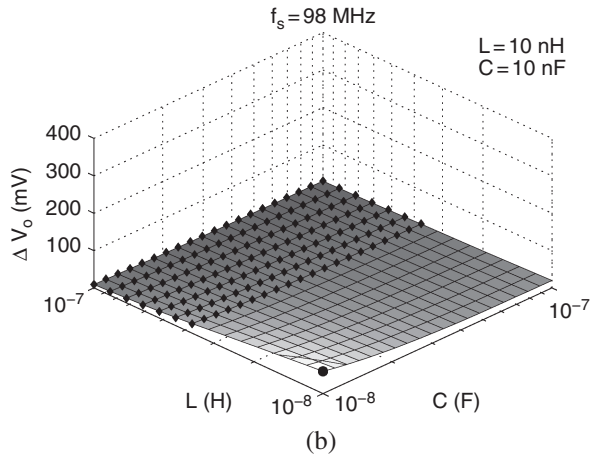
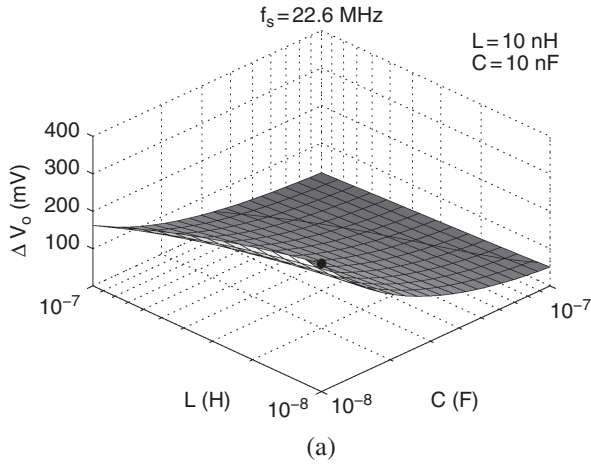


Fig. 2.18 Buck converter output voltage ripple: **a** $f_s = 22.6 \text{ MHz}$; **b** $f_s = 98 \text{ MHz}$; **c** $f_s = 260.5 \text{ MHz}$

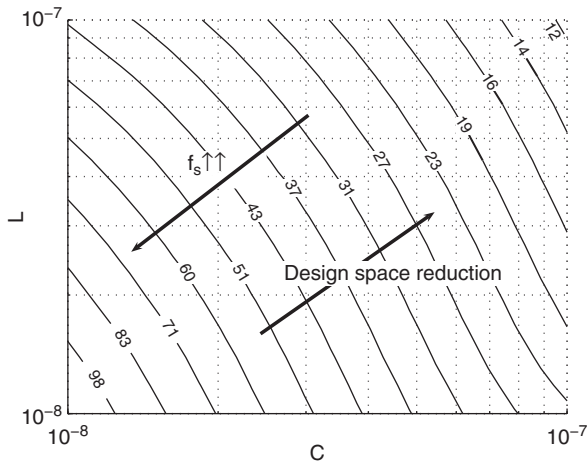


Fig. 2.19 Design space reduction (in plane (L, C_o)) due to the output voltage ripple constraint, as a function of the switching frequency (numbers on isolines represent f_s values in MHz). Possible designs appear on the *right* of any isoline

Hence, the optimized design previously found in (Fig. 2.17b) is replaced by the one that appears in Fig. 2.23. It should be noted that although the inductor and capacitor values remain the same (which results in the minimum area design), switching frequency is increased in order to produce lower output ripple. Obviously, the resulting power efficiency is slightly lower than the one corresponding to (Fig. 2.17b). Table 2.6 summarizes the complete set of characteristics of this design setup. In this case, very small change on efficiency results from the frequency increase (which in turn is due to the output ripple constraint application), although in other cases design space constraint could have a greater effect on the final result.

In Fig. 2.24 power loss distribution as well as occupied area are shown as a function of the power lower loss mechanisms and components, respectively.

As regards energy losses distribution, it is found what would have been expected from results in Sect. 2.2.2.5:

- Transistor switching losses are independent not only from the transistor channel width, but even from the transistor type (NMOS or PMOS), since their corresponding driver will be accordingly designed.
- In both types of transistors, those associated energy losses that depend on channel width (conduction and driver losses) become equalized when losses are minimized. This is caused by the opposed trends that these loss mechanisms present when channel width is changed.
- Inductor conduction losses are the highest, which is reasonable because any current flowing through the Buck converter always passes through the inductor, whereas it is split between both transistors.
- Capacitor conduction losses are the lowest because of the low capacitor ESR considered, and the fact that its current is much lower than the inductor current.

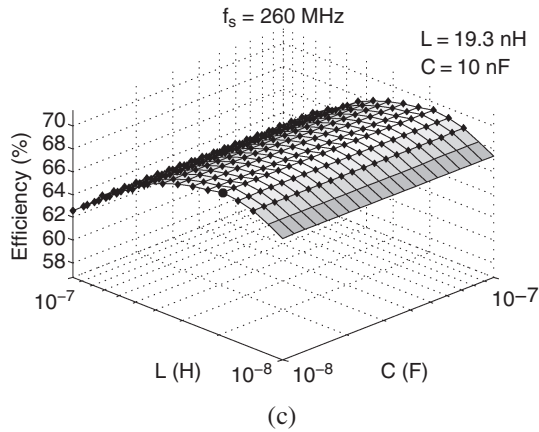
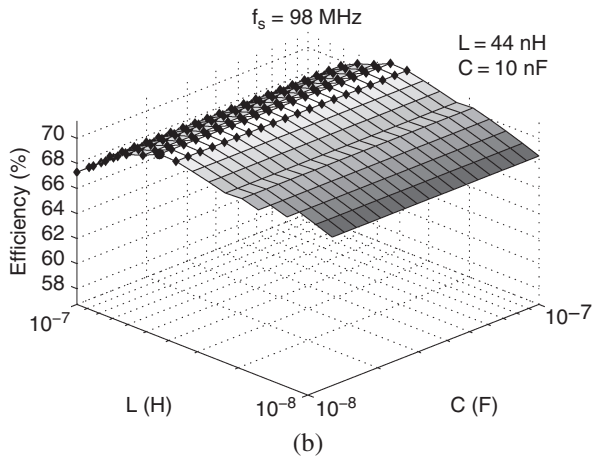
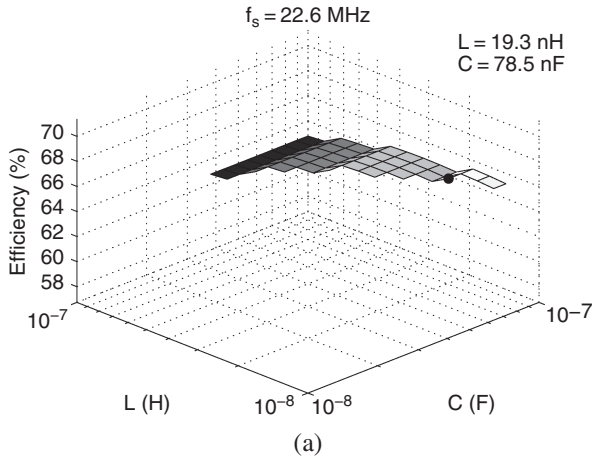


Fig. 2.20 Buck converter power efficiency after applying the output ripple constraint on design space: **a** $f_s = 22.6 \text{ MHz}$; **b** $f_s = 98 \text{ MHz}$; **c** $f_s = 260.5 \text{ MHz}$

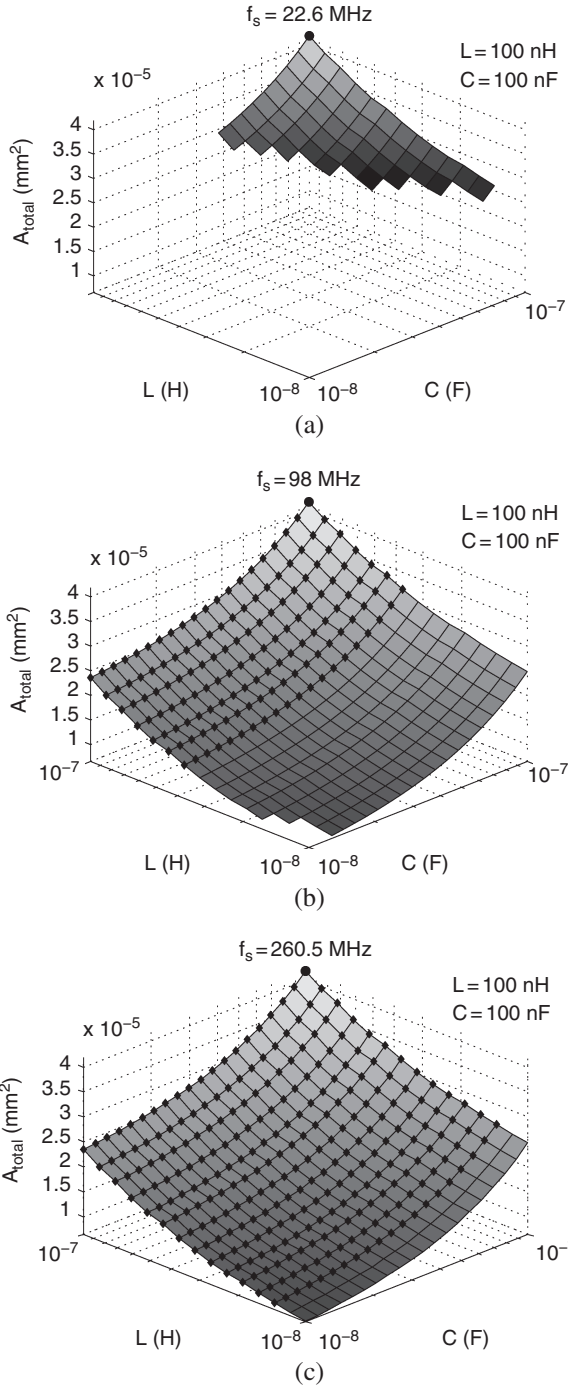


Fig. 2.21 Buck converter total occupied area after applying the output ripple constraint on design space: **a** $f_s = 22.6$ MHz; **b** $f_s = 98$ MHz; **c** $f_s = 260.5$ MHz

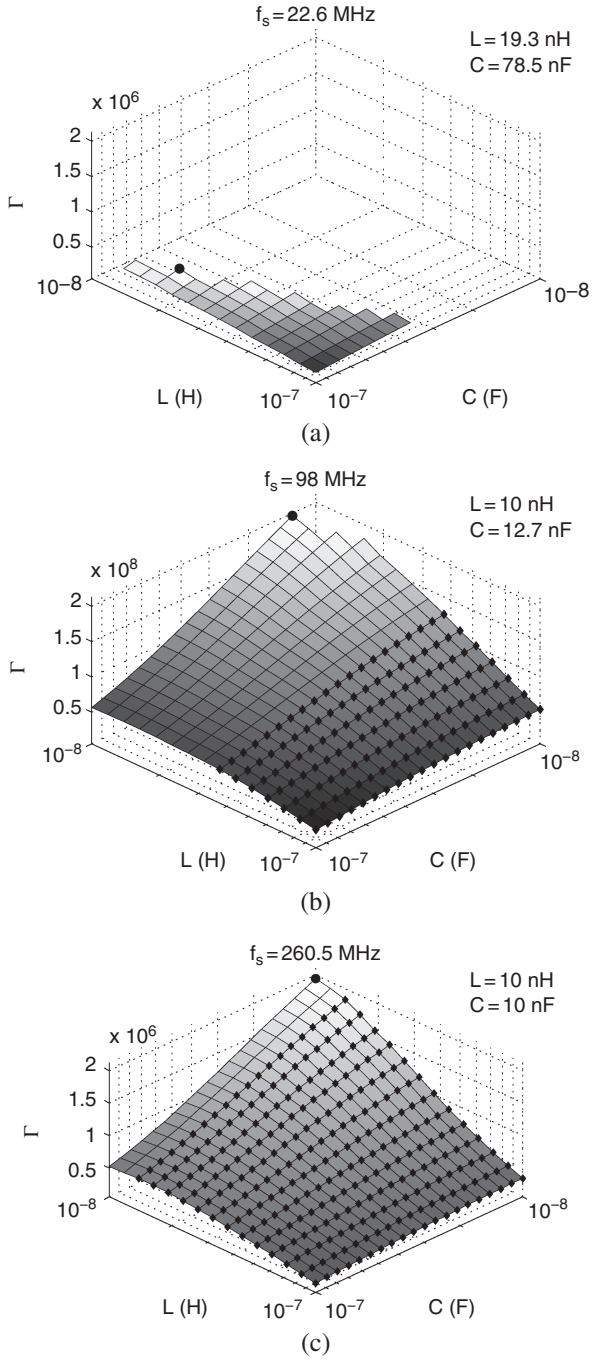


Fig. 2.22 Merit figure representation, applying the output ripple constraint: **a** $f_s = 22.6$ MHz; **b** $f_s = 98$ MHz; **c** $f_s = 260.5$ MHz

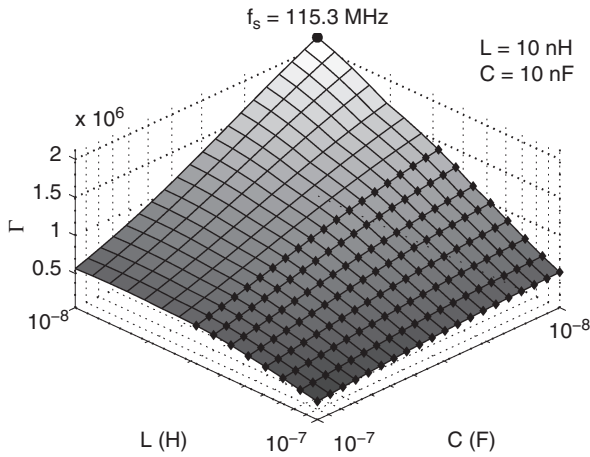


Fig. 2.23 New optimized design after applying the output voltage ripple constraint ($f_s = 115.3$ MHz)

Table 2.6 Complete set of characteristics of the optimized design after the application of the output ripple constraint

Variable	Value
Battery voltage	3.6 V
Output voltage	1 V
Output current	100 mA
Inductor (L)	10 nH
Inductor ESR	621.5 m Ω
Inductor outer diameter	2.1 mm
Inductor number of turns	3
Capacitor (C_o)	10 nF
Capacitor ESR	50 m Ω
Switching frequency (f_s)	115.3 MHz
Total Area	6.59 mm ²
Power efficiency	68.57%
Output voltage ripple	49 mV
Maximum inductor current	354 mA
Operating mode	DCM
N-MOSFET channel width	1,572 μ m
N-MOSFET driver inverters	7
P-MOSFET channel width	2,083 μ m
P-MOSFET driver inverters	7

In addition to this, Fig. 2.24b clarifies that the occupied silicon area is almost absolutely due to the energy storage components.

The main conclusion that arises from the presented design procedure is that the design challenge that any designer faces when trying to develop a switching power converter to fulfill some specifications is solved by means of the design space exploration. This just requires the appropriate modelling of any of the components to be designed, and subsequently the application of the considered constraints of the

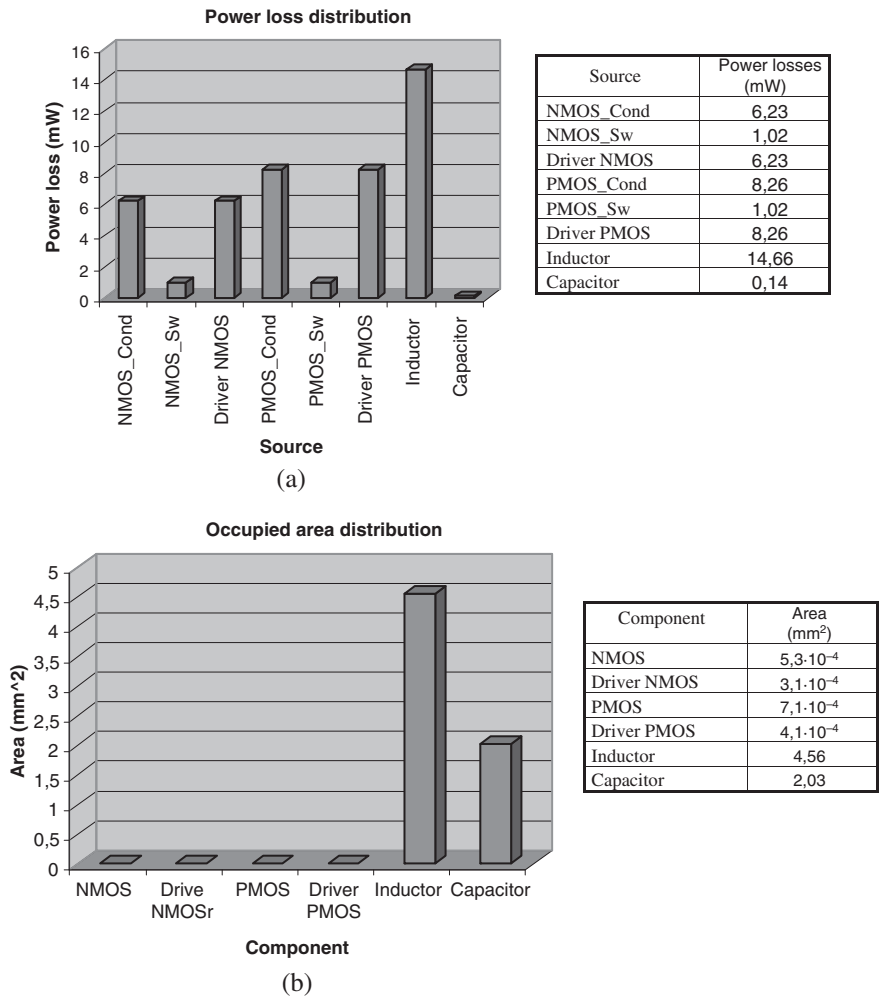


Fig. 2.24 Optimized design power losses **a** and occupied area **b** distributions, for each converter component

design space. Finally, the convenient definition of a merit figure is used to obtain the desired converter configuration.

Therefore, it is observed that the huge number of questions that involve the whole design (reactive components values, switching frequency, power transistors size, power drivers design, ...) are indirectly answered, being the final result a set of design characteristics and values as the exposed in Table 2.6, after considering all the suitable possibilities.

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