

Preface

Device-level modeling and synthesis of high-performance pipeline ADCs

Digital computing and signal processing are present in most current communications systems. The proliferation of these systems, compared with their analog counterparts, is a result of their robustness to supply and processing variations, their low sensitivity to noise and, above all, the improvements in their technological scaling [1–5]. These properties have made the design and test automation of such systems easier, favouring the development of *Computer-Aided Design* (CAD) tools and automatized methodologies.

In spite of the benefits of digital processing, a communications system cannot be fully digital as the actual signals are inherently analog and as a result, there is a need for circuits which can interface with the digital world. Analog-to-Digital Converters (ADCs), which acquire and digitize the signal, fall into the category of circuits required. As Fig. 1 shows, numerous approaches can be found, depending on the field of application of the converter. The design of these analog circuits is a major challenge for designers due to rapidly-evolving digital systems, which require increasingly accurate and fast converters, while the current trend to integrate them into adverse digital technologies is also a contributing factor. Hence the importance of developing design methodologies and CAD tools [6–16] which can assist designers in shortening the time-to-market of final products and reducing the complexity of such a challenge.

In this monograph, a thorough design methodology for ADCs, and more specifically pipeline converters, will be presented. The main motivations for this book are that: (1) on the one hand, pipeline converters cover a wide field of broadband applications such as *Digital Video Broadcasting* (DVB), *Power Line Communications* (PLC) or *Very high bit-rate Digital Subscriber Line* (VDSL) communications and (2) their inner structure is complex, comprising very accurate *Switched-Capacitor* (SC) circuits, other sub-ADC topologies such as flash architectures, digital circuits, numerous auxiliary building blocks and a meticulous timing. These two reasons make a design methodology for pipeline converters even more attractive and necessary. The main contributions of this design methodology are:

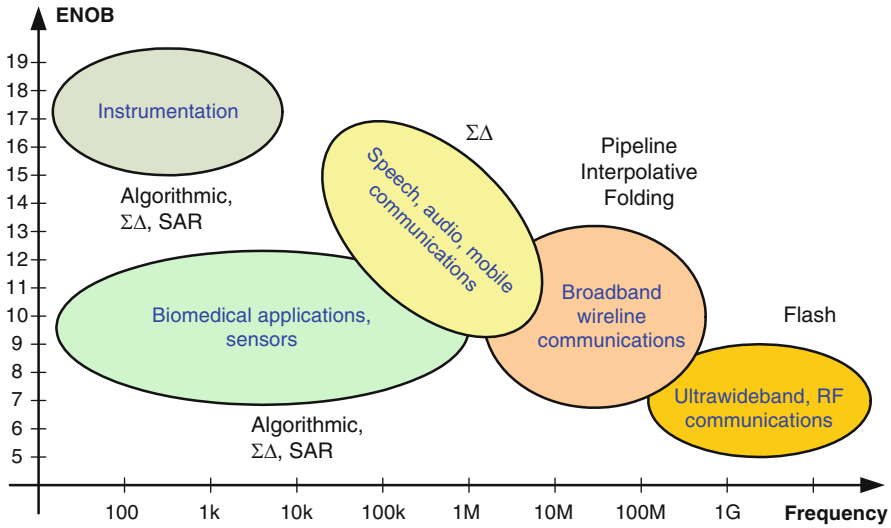


Fig. 1 Field of application of ADCs

- The development of an accurate and fast behavioural simulator for pipeline ADCs. It includes efficient and accurate behavioural models for the basic building blocks of pipeline converters. In addition, it provides high flexibility, low computational cost, and user-friendliness since it has been integrated into the Matlab-Simulink interface. To the best of our knowledge, these behavioural models are the most accurate and thorough models reported to date, taking into account not only small-signal effects but also other important large-signal phenomena. In fact, our behavioural models show a maximum deviation of 0.3 bits of effective resolution with transistor-level simulations.
- The above behavioural simulator has been combined with an optimization algorithm for synthesis purposes. Both genetic and simulated annealing approaches have been used.
- A complex synthesis procedure for the mapping of the high-level converter specifications onto transistor-level specifications has been developed. This procedure is able to reduce the design parameter space to only three design variables, from which the remaining parameters are meticulously determined. This reduction of the design parameter space is combined with a set of processing routines in Matlab which optimize the sizing of remaining parameters and provide accurate estimates of transistor-level parameters. These routines use look-up table techniques for a better characterization and estimation of technology parameters.

As a result, an efficient and accurate transistor-level synthesis tool of pipeline converters will be implemented. It will be able to map the high-level specifications of the pipeline converter directly onto transistor-level parameters. To do so we will combine the proposed behavioural simulator to evaluate the converter performance, and the Matlab routines to reduce the design parameter space and estimate the parasitics and dimensions of the transistors at electrical level; with an optimization algorithm for

the selection of the most suitable pipeline architecture in terms of power consumption and area. Against other design methodologies and CAD tools, it will be shown that several advantages are achieved with our proposed synthesis tool: (1) the proposed behavioural modelling will extend previous approaches, considering both one- and two-stage *Miller Compensated* (MC) OTA macromodels and including small- and novel large-signal effects, (2) the required bottom-up iterations for the fine tuning of the converter performance will be drastically reduced thanks to actual transistor-level parameters (such as parasitic capacitances, transconductances, saturation currents, etc.) and closed-loop operation conditions will be intrinsically considered in the design flow; (3) optimum architecture selection will be guaranteed since all required architectures will be synthesized at transistor level thanks to the efficiency and speed of the proposed tool; (4) the typical oversizing carried out by most designers due to uncertainty of other design methodologies will not be necessary since the accuracy of the behavioural models proposed will allow us to estimate both the resolution and power consumption of the converter with precision.

It is worth mentioning that although this design methodology will be developed specifically for pipeline ADCs, it can easily be extended to other converter approaches such as Sigma-Delta ($\Sigma\Delta$), algorithmic or Successive Approximations Register (SAR) architectures. The book is organized into seven chapters.

Chapter 1: Pipeline ADC Overview

This chapter will present a brief introduction to ADCs, offering a description of the fundamentals of analog-to-digital conversion and the main error mechanisms inherent to the conversion process. The main metrics which characterize the ADC performance will also be summarized. The basic operation principles of pipeline converters will then be described and the practical implementation of its basic building blocks discussed.

Chapter 2: Design Methodologies for Pipeline ADCs

A brief review of the conventional design methodologies for analog-to-digital converters is offered in this chapter. A novel synthesis tool will be proposed for the improvement of these conventional design methodologies. This tool will be composed of a behavioural simulator, a set of Matlab routines, and an optimizer. The main advantages of this synthesis procedure will be highlighted.

Chapter 3: Pipeline ADC Electrical-Level Synthesis Tool

The proposed synthesis tool, which has been integrated into the Matlab-Simulink interface, will be presented in this chapter. Brief descriptions will be offered for the

basic components, that is, the behavioural simulator, the set of Matlab routines and the optimizer.

Chapter 4: Behavioural Modelling of Pipeline ADCs

The key to the proposed synthesis tool is a behavioural simulator which allows us to accurately estimate the performance of the ADC. This behavioural simulator includes a set of behavioural models which describe the effect of the main non-idealities of the practical implementation of the basic building blocks in the pipeline converter. This chapter will be devoted to presenting these behavioural models and illustrating the impact of these non-idealities on the performance of the ADC.

Chapter 5: Case Study: Design of a 10bit@60MS Pipeline ADC

The design methodology will be applied to synthesize a 10bit@60MS/s pipeline ADC in a 0.13 μ m 6-metal technology at 1.2 V voltage supply. The high-level converter specifications will be directly mapped to transistor-level specifications, verifying target fulfilment by means of transistor-level simulations. The design of auxiliary building blocks will also be detailed. The layouts of all basic building blocks will be presented and post-layout verifications will be carried out.

The converter designed will only consume about 23 mW, including internal reference voltage generators and digital circuits, which provide excellent performance when compared with state-of-the-art pipeline converters. In addition, these specifications will be fully satisfied on all required technological corners.

Chapter 6: Experimental Results and State of the Art

The prototype will be tested in the laboratory. The test procedure and the measured performance will be presented and compared with similar state-of-the-art pipeline converters in this chapter.

Chapter 7: Conclusions and Future Lines of Research

The final chapter of this work draws conclusions and suggests future lines of research.

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