

Table of Contents

- 1 Pipeline ADC Overview 1**
 - 1.1 A/D Conversion: Fundamentals 1
 - 1.1.1 Sampling Theory 1
 - 1.1.2 Quantization 2
 - 1.1.3 A/D Conversion Errors 3
 - 1.1.4 A/D Characterization 7
 - 1.2 Pipeline Fundamentals 11
 - 1.2.1 Operation Principle 11
 - 1.2.2 Redundancy 13
 - 1.2.3 Analog Building Blocks Implementation 15
 - 1.3 Current Trends in Pipeline Converters 20
 - 1.3.1 State-of-the-Art Technology in Pipeline Converters 25
- 2 Design Methodologies for Pipeline ADCs 29**
 - 2.1 Top-Down Design Methodology 29
 - 2.2 Key Elements in a Top-Down Design Methodology 32
 - 2.2.1 Simulator and Circuit Modelling 32
 - 2.2.2 Power and Area Estimators 33
 - 2.2.3 Synthesis Procedures 33
 - 2.3 Proposed Synthesis Procedure 34
- 3 Pipeline ADC Electrical-Level Synthesis Tool 39**
 - 3.1 Synthesis Procedure 39
 - 3.2 Snycos: The Behavioural Simulator 41
 - 3.2.1 Accuracy 41
 - 3.2.2 Low Computational Cost 41
 - 3.2.3 Flexibility 43
 - 3.2.4 User-Friendliness 44

3.3	Low-Level Mapping Routines	44
3.3.1	One-Stage OTA Mapping Procedure	46
3.3.2	Two-Stage MC OTA Procedure	54
3.4	Optimization Algorithms	62
4	Behavioural Modelling of Pipeline ADCs	65
4.1	Non-Idealities in SH and MDACS	65
4.1.1	Ideal Performance of the MDAC	67
4.1.2	Capacitors Mismatch	68
4.1.3	Dynamic Limitations: Small-Signal Effects	69
4.1.4	Dynamic Limitations: Large-Signal Effects	75
4.1.5	Switch-on Resistance	83
4.1.6	Thermal Noise in the MDAC	89
4.1.7	Jitter Noise	96
4.1.8	Behavioural Model of the MDAC	96
4.2	Non-Idealities in Sub-ADCS	99
5	Case Study: Design of a 10bit@60MS Pipeline ADC	105
5.1	Design Scenario	105
5.1.1	Converter Specifications	105
5.1.2	Technology	106
5.2	Transistor-Level Synthesis of the ADC	109
5.3	Redesigning for Corners	113
5.4	Electrical-Level Design: Detailed Description	116
5.4.1	SH Circuit	116
5.4.2	MDACs	122
5.4.3	Sub-ADCS	123
5.4.4	Clock-Phase Generator	131
5.4.5	Reference Voltage Generator	134
5.4.6	Common-Mode Voltage Generator	145
5.4.7	Reference Current Generator	148
5.5	Converter Electrical-Level Verification	149
5.6	Layout	151
5.6.1	SH Layout	152
5.6.2	MDAC Layout	153
5.6.3	Sub-ADC Layout	155
5.6.4	Reference Current Generator Layout	156
5.6.5	Reference Voltage Generator Layout	156
5.6.6	Clock-Phase Generator Layout	158
5.6.7	ADC Layout	158
5.7	Post-Layout Verification	160
5.7.1	SH & MDAC Post-Layout Verification	161
5.7.2	Remaining Building Block Post-Layout Verification	163
5.7.3	Converter Post-Layout Verification	165
5.8	Packaging	166

6	Experimental Results and State of the Art	171
6.1	Test Setup	171
6.1.1	PCB	171
6.2	Experimental Results	177
6.2.1	Static Characterization	177
6.2.2	Dynamic Characterization	179
7	Conclusions and Future Lines of Research	185
	Appendix A: Technology Characterization	189
	Appendix B: Thermal Noise in SC Circuits Overview	193
	References	199
	Index	207



<http://www.springer.com/978-1-4419-8845-4>

Device-Level Modeling and Synthesis of
High-Performance Pipeline ADCs

Ruiz-Amaya, J.; Delgado-Restituto, M.;

Rodríguez-Vázquez, Á.

2011, XIII, 209 p., Hardcover

ISBN: 978-1-4419-8845-4