

Chapter 2

VCO-Based Quantizer

In this chapter a detailed analysis on the operation and architecture of the voltage-controlled oscillator (VCO)-based ADC is presented. The VCO-based quantizer is analyzed for two different architectures, one using a frequency-to-digital converter (FDC) the other a time-to-digital converter (TDC). Theoretical equations are derived to determine the resolution of these quantizers and verified through a VerilogA model.

2.1 VCO Operation

An ideal VCO output can be expressed as a sinusoidal signal with amplitude and phase as shown in (2.1) [1]:

$$\text{VCO}_{\text{out}}(t) = A_{\text{vco}} \sin \theta_{\text{vco}}(t), \quad (2.1)$$

$$\theta_{\text{vco}}(t) = 2\pi \int_0^t f_{\text{vco}}(\tau) d\tau = 2\pi \int_0^t f_c + K_v x(\tau) d\tau. \quad (2.2)$$

The phase of the VCO (2.2) is the integral of the VCO frequency which depends on VCO characteristics such as the free running center frequency, f_c , VCO gain, K_v , and input signal to the VCO, i.e., the control voltage $x(t)$. The block diagram of the VCO is shown in Fig. 2.1.

The voltage dynamic range of $x(t)$ is converted to a frequency dynamic range via the VCO, which depends on the control voltage, $x(t)$, along with the VCO gain, K_v . This is shown graphically in Fig. 2.2, where the VCO output frequency range is $f_c \pm \Delta f$, with $\Delta f = K_v x(t)$.

Next the methods of quantizing the VCO output signal are discussed. The FDC measures the phase difference between samples to arrive at the VCO frequency,

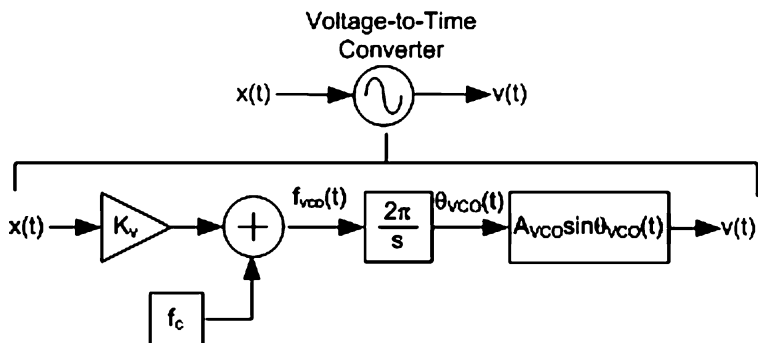


Fig. 2.1 VCO block diagram

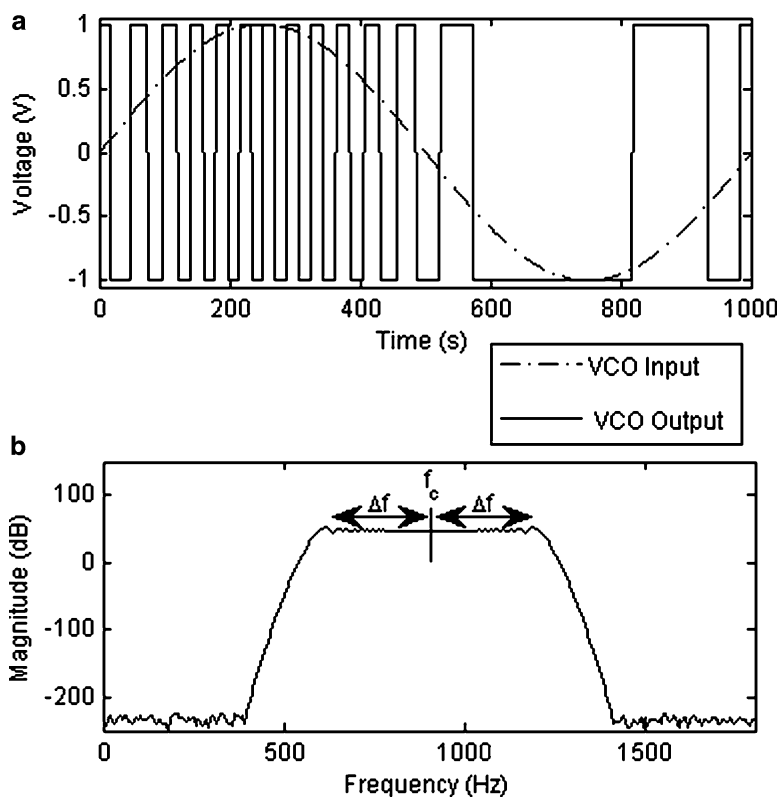
Fig. 2.2 (a) Buffered VCO output vs. sinusoidal VCO input signal (time domain). (b) VCO output with frequency range: $f_c \pm \Delta f$ (frequency domain)

Fig. 2.3 VCO-based quantizer. (a) FDC: measures phase difference. (b) TDC: measures period and inverts

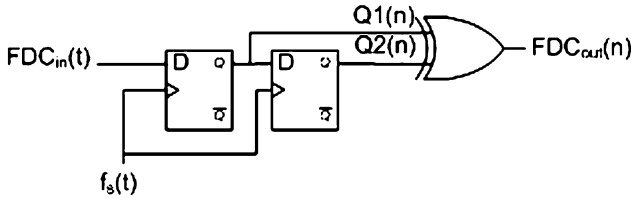
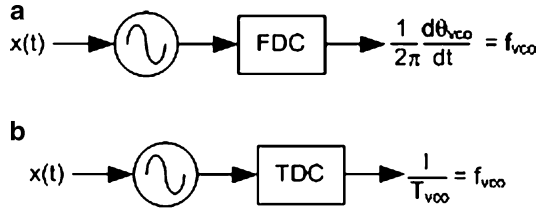


Fig. 2.4 FDC block diagram

while the TDC measures the period of the VCO which is inverted to get the VCO frequency, Fig. 2.3.

2.2 FDC VCO-Based Quantizer

The architecture of the FDC consists of two D flip-flops (DFFs) and one XOR gate as shown in Fig. 2.4 [2].

Consider the waveforms shown in Fig. 2.5. The FDC operation is as follows: At the rising clock edge the first DFF output, Q1, samples the input signal. The value of the second DFF output, Q2, takes on the value of Q1 before that rising clock edge. The output of the FDC, the XOR gate, determines if there is a difference between two consecutive samples. Consider the first occurrence when the FDC input changes from 1 to 0. At the rising clock edge after this transition, the first DFF output, Q1, changes from 1 to 0. The value of the second DFF output, Q2, takes on the value of Q1 before that rising clock edge – 1. The XOR gate sees $Q1 = 0$ and $Q2 = 1$ and it outputs a value of 1. Thus, the FDC operates as an edge detector, with some delay or error when the transition is detected, this can be up to one clock period.

The architecture of the FDC VCO-based quantizer is shown in Fig. 2.6 [3]. This architecture consists of a ring VCO to provide a multiphase output, and several FDC's operating in parallel which are summed together to form a multibit

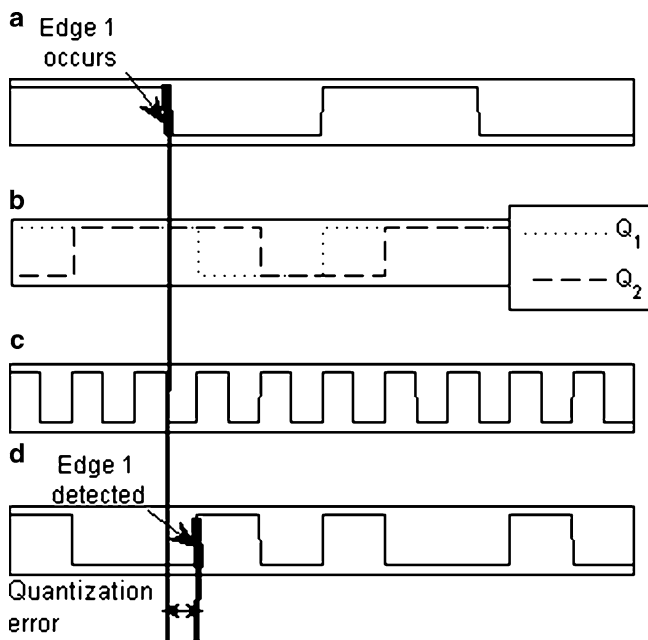


Fig. 2.5 FDC example waveforms. (a) FDC input; (b) output of sampled DFF 1 and 2; (c) sampling clock $f_s(t)$; (d) FDC output

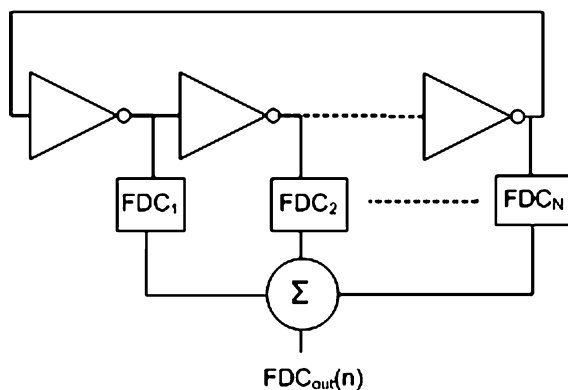


Fig. 2.6 Multibit FDC VCO-based quantizer

quantizer. The VCO phase taps are delayed from one another by $2\pi/N$, N being the number of stages. Thus, there are multiple reads of the signal within a single cycle to improve the resolution. The single-bit and multibit operations are shown in Fig. 2.7.

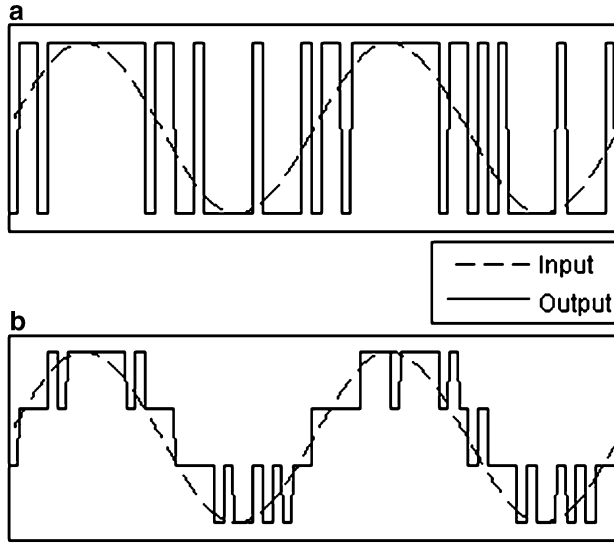


Fig. 2.7 FDC VCO-based quantizer input vs. output (time domain): (a) single bit (b) multibit

2.2.1 Linear Modeling and Analysis

The FDC VCO-based quantizer is modeled and analyzed using linear modeling to determine the resolution. As stated before, the FDC differentiates the VCO phase to get the VCO frequency. Figure 2.8 shows the VCO phase which is sampled at two consecutive samples denoted as $(n - 1)$ and (n) . θ_{vco} is the actual VCO phase and ϕ_{vco} is the phase error which is the difference between what the actual VCO phase is and when it last accumulated multiple of π . When the VCO phase accumulates π , the VCO output will undergo transition which is detected by the FDC at the next sampling instance.

The output of the FDC can be written as the phase difference between samples (2.3) using the relationships shown in Fig. 2.8. The equation includes the multibit operation of using “ N ” FDCs, similar analysis is given in ref. [4].

$$\text{FDC}_{\text{out}}(n) = \frac{N}{\pi} [\theta_{\text{vco}}(n) - \theta_{\text{vco}}(n - 1) + \phi_{\text{vco}}(n - 1) - \phi_{\text{vco}}(n)]. \quad (2.3)$$

The VCO phase given in (2.2) is sampled and can be written as (2.4):

$$\theta_{\text{vco}}(n) = 2\pi \int_{(n-1)T_s}^{nT_s} f_c + K_v x(\tau) d\tau = 2\pi \sum_{i=1}^n T_s [f_c + K_v x(i)]. \quad (2.4)$$

The FDC output equation is simplified in terms of the phase difference as shown in (2.5) and (2.6) to arrive at the output equation of the FDC (2.7).

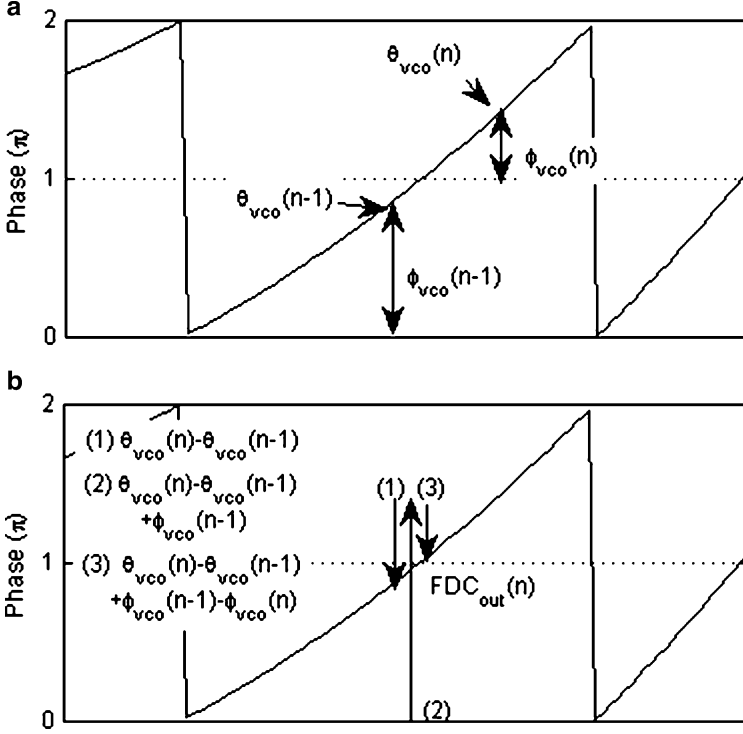


Fig. 2.8 Quantization of VCO phase by the use of FDC: (a) phase and phase error for two consecutive samples; (b) FDC output based on phase differences

$$\theta_{vco}(n) - \theta_{vco}(n-1) = 2\pi \sum_{i=1}^n T_s [f_c + K_v x(i)] - 2\pi \sum_{i=1}^{n-1} T_s [f_c + K_v x(i)], \quad (2.5)$$

$$\theta_{vco}(n) - \theta_{vco}(n-1) = 2\pi T_s [f_c + K_v x(n)], \quad (2.6)$$

$$FDC_{out}(n) = 2NT_s [f_c + K_v x(n)] + \frac{N}{\pi} [\phi_{vco}(n-1) - \phi_{vco}(n)]. \quad (2.7)$$

Using Z-transformations, the output of the FDC in terms of the frequency domain is written as (2.8):

$$FDC_{out}(z) = 2NT_s f_c + 2NT_s K_v X(z) + \frac{N}{\pi} \phi_{vco}(z) \left(\frac{1-z}{z} \right). \quad (2.8)$$

Based on (2.8), the signal transfer function (STF) and noise transfer function (NTF) for the FDC VCO-based quantizer is derived in (2.9) and (2.10).

$$\text{STF} = \frac{\text{FDC}_{\text{out}}(z)}{X(z)} = 2NT_s K_v, \quad (2.9)$$

$$\text{NTF} = \frac{\text{FDC}_{\text{out}}(z)}{\phi_{\text{vco}}(z)} = \left(\frac{1-z}{z} \right) \frac{N}{\pi}. \quad (2.10)$$

From the derivations, the input signal is scaled while the quantization noise is first-order shaped. To derive the SNR, the power of the signal and the power of the noise at the output of the FDC are calculated. Consider the input to the VCO as a sine wave (2.11), then the power of the output signal is given as follows (2.12):

$$x(t) = A_m \sin(2\pi f_m t), \quad (2.11)$$

$$P_s = \left(\frac{2NT_s K_v A_m}{\sqrt{2}} \right)^2. \quad (2.12)$$

The power of the quantization noise is derived next. The quantization noise is assumed to be white and thus the level of noise is constant across all frequencies and equal to (2.13) using the two-sided definition of power [5, pp. 532–533].

$$\phi_{\text{vco}}(n) = \frac{\Delta}{\sqrt{12f_s}} = \frac{\pi}{N\sqrt{12f_s}}, \quad (2.13)$$

where Δ is the difference between quantization levels, in the FDC case this is equal to π and reduced by N when using a multibit architecture [6]. The noise is filtered through the NTF. For this analysis, the NTF is given in the frequency domain (2.14):

$$\begin{aligned} \text{NTF} &= \left(\frac{1-z}{z} \right) \frac{N}{\pi} \bigg|_{z=e^{j2\pi\ell/f_s}} = N \frac{e^{-j2\pi\ell/f_s} - 1}{\pi} \\ &= -N \frac{2j}{\pi} e^{-j\pi(f/f_s)} \frac{e^{j\pi\ell/f_s} - e^{-j\pi\ell/f_s}}{2j}. \end{aligned} \quad (2.14)$$

Using Euler's formula, the magnitude of the NTF assuming that the sampling frequency is much greater than the bandwidth is given as follows (2.15):

$$|\text{NTF}| = N \frac{2}{\pi} \sin\left(\pi \frac{f}{f_s}\right) \approx N \frac{2}{\pi} \frac{\pi f}{f_s} = N \frac{2f}{f_s}. \quad (2.15)$$

The in-band power given a bandwidth equal to f_b is given in (2.16) using (2.13) and (2.15):

$$P_N = 2 \int_0^{f_b} \left(\frac{2f}{f_s} \frac{\pi}{\sqrt{12f_s}} \right)^2 df = 8 \frac{\pi^2 f_b^3}{36 f_s^3} = \frac{\pi^2}{36 \text{OSR}}. \quad (2.16)$$

The power of the noise matches the general equation used for first-order noise shaping [5, p. 552]. The SNR is the power of the signal divided by the power of the noise, (2.12) divided by (2.16), given as follows (2.17):

$$\text{SNR} = 10 \log_{10} \left(\frac{(2NT_s K_v A_m / \sqrt{2})^2}{8(\pi^2 f_b^3 / 36 f_s^3)} \right) = 10 \log_{10} \left(\frac{9 f_s^3 (2NT_s K_v A_m)^2}{4 \pi^2 f_b^3} \right). \quad (2.17)$$

The maximum SNR of the FDC VCO-based quantizer depends on the number of FDCs, the ratio of the sampling frequency to the system bandwidth, and the VCO gain factor. This SNR value is consisted with what has previously been derived [4].

2.2.2 Model Verification Using VerilogA

To verify the above analysis and make further assessment, the FDC VCO-based quantizer is modeled in VerilogA and shown below.

```
//Begin VerilogA code: FDC VCO-based quantizer
`include "constants.vams"
`include "disciplines.vams"
`define PI 3.14159265

module fdc(in,clk,out);
input in, clk;
output out;
voltage in,clk,out;

parameter real      vdd=0.6,          // Positive Supply
                   vss=-0.6,          // Negative Supply
                   fc=500e6,           // VCO center frequency
                   Kv=250e6;           // VCO gain Hz/V
parameter           N=5;               // number of phase taps

// Define variables
real vout,fvco,phase, Ac, vmid;
real vcout[0:N-1];
integer q1[0:N-1],q2[0:N-1];
integer i,count;
```



```

analog begin
// Initialized Parameters
    @(initial_step) begin
        Ac=(vdd-vss)/2.0;    // VCO Amplitude
        vmid=(vdd+vss)/2.0; // Midrail Voltage
    end
// Ideal VCO frequency and phase equations
    fvco=Kv*V(in)+fc;    // VCO Frequency
    phase=2.0*PI*idtmmod(fvco,0,1,-0.5);    // VCO Phase
    for(i=0;i<N;i=i+1) begin
// Multiphase VCO output "N" phase taps
        vcout[i]=vmid+Ac*sin(phase+i*2.0*PI/N);
// Buffer multiphase VCO outputs
        if (vcout[i]>=vmid) vcout[i]=vdd;
        if (vcout[i]<vmid) vcout[i]=vss;
    end
// "N" FDCs samples at the rising clock edge
    @ (cross(V(clk)-vmid,1)) begin
        count=0;
        for(i=0;i<N;i=i+1) begin
            q2[i]=q1[i]; // DFF2=DFF1
            q1[i]=vcout[i]>=vmid; // DFF1=buffered VCO output
// XOR Q1 and Q2 - add for multibit output
            if (q1[i] != q2[i]) count=count+1;
        end
    end
    vout= count    // Output
    V(out) <+ vout;
end
endmodule
//End VerilogA code: FDC VCO-based quantizer

```

The input to the VerilogA model is the clock signal and the input control voltage to the VCO. The VCO is modeled using the ideal relationships and buffered. At the rising clock edge, each FDC operates on its own buffered VCO phase tap. The output of the model is the sum of the FDCs.

To verify the theoretical analysis, multiple simulations of the VerilogA code are run varying different circuit parameters, Fig. 2.9. The theoretical analysis shows good correlation with the VerilogA model.

2.3 TDC VCO-Based Quantizer

The architecture of the TDC consists of a delay chain, several DFFs, and a digital pulse detector as shown in Fig. 2.10 [7].

Consider the waveforms shown in Fig. 2.11. The TDC operation is as follows: the input to the TDC is a pulse which will propagate through the delay chain and be sampled through the DFF's providing a snapshot of that pulse. Then using digital logic, the width of that pulse may be detected with some error which depends on the delay of the buffer (τ_{buff}) in the delay chain. The output of the pulse detector gives a

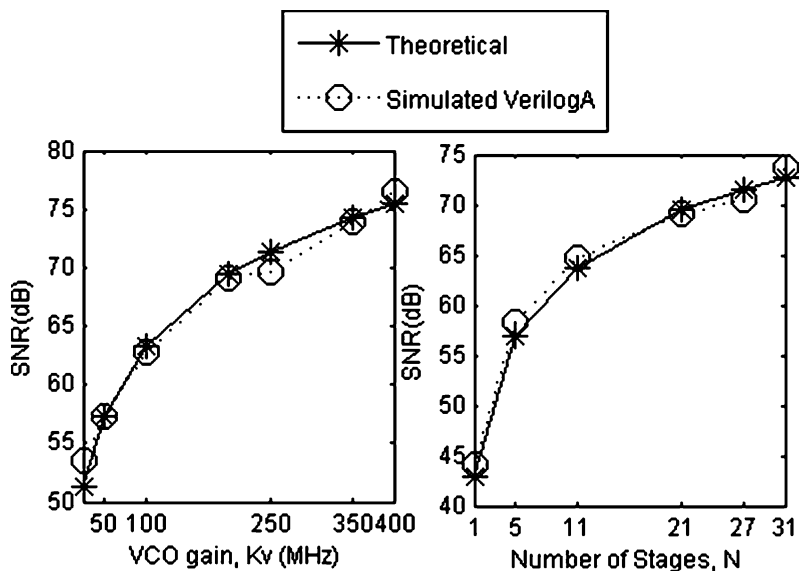


Fig. 2.9 FDC VCO-based quantizer SNR curves while varying design parameters: theoretical vs. simulated VerilogA model

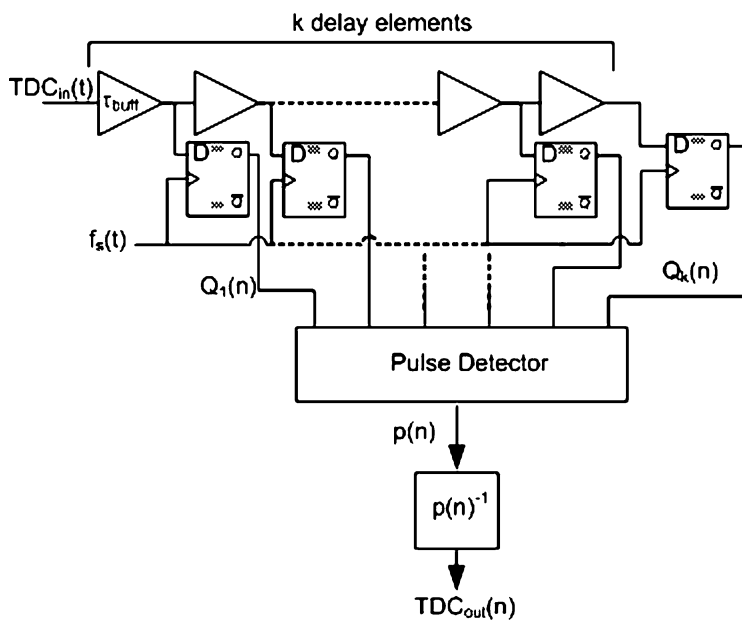


Fig. 2.10 TDC block diagram

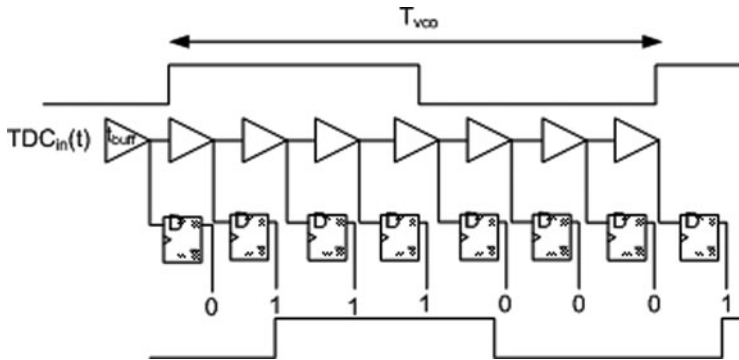


Fig. 2.11 Quantization of VCO period by the use of a TDC

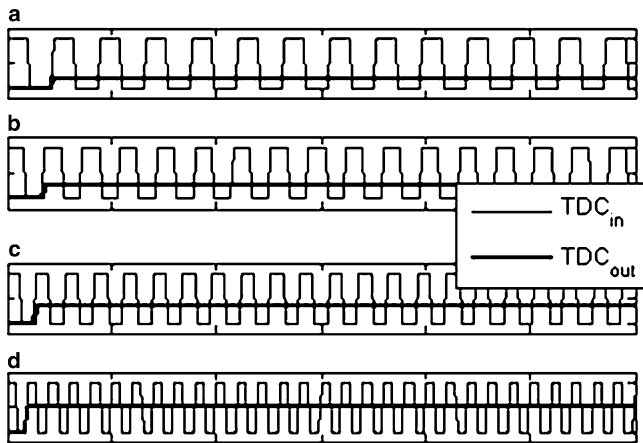


Fig. 2.12 TDC example waveform

representation of the period of that pulse and can be inverted to get the frequency; some results are shown in Fig. 2.12.

Like the FDC, the TDC can have “ N ” stages cascaded together, Fig. 2.13. The same delay chain can be used for each TDC; however, different sampling DFFs and pulse width detectors are needed. The clock signal is delayed to each TDC to cover a complete sampling cycle and the output of each TDC will be added to improve the resolution. This is the equivalent of increasing the sampling clock by “ N ”. This is a slightly different approach to improve the dynamic range of the TDC than taken in ref. [7].

The architecture of the TDC VCO-based quantizer consists of any type of VCO and the TDC shown in Fig. 2.10. The resolution of the quantizer is improved by using multiple TDCs but only requires one-phase output of the VCO. The single TDC and multi-TDC VCO-based quantizer operations are shown in Fig. 2.14.

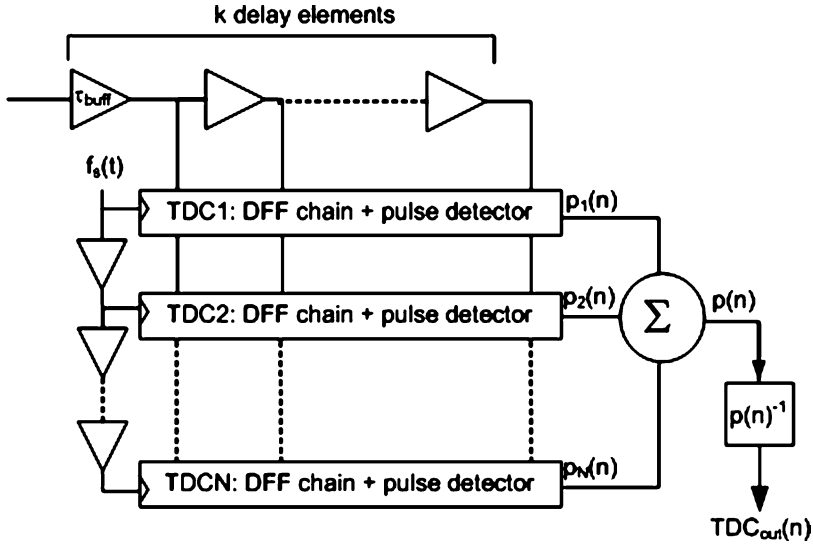


Fig. 2.13 Cascaded TDC block diagram

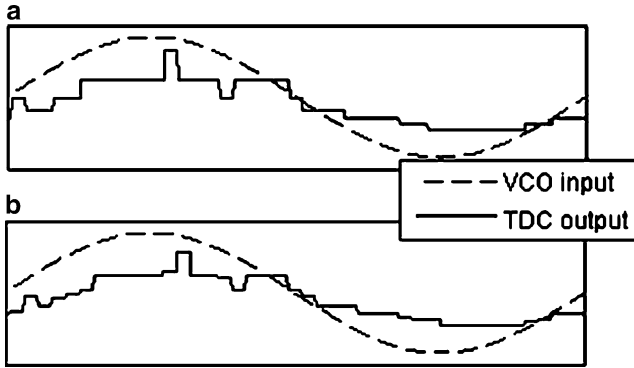


Fig. 2.14 TDC VCO-based quantizer input vs. output (time domain): (a) single TDC (b) multi-TDC

2.3.1 Linear Modeling and Analysis

The TDC VCO-based quantizer is modeled and analyzed using linear modeling to determine the resolution. As stated before, the TDC measures the period of the VCO and is inverted to get the VCO frequency. The detected pulse using the relationship shown in Fig. 2.11 is given in (2.18), including multiple TDCs.

$$p(n) = \frac{NT_{\text{vco}}(n)/2 + \sqrt{N}q(n)}{\tau_{\text{buff}}}. \quad (2.18)$$

The period of the VCO is divided by two since only the positive going pulse is detected, and it is quantized in terms of the buffer delay, τ_{buff} , with quantization noise, $q(n)$. The noise is assumed to be uncorrelated and adds as the square root of N , while the signal adds constructively. Since the frequency of the VCO is of interest, the pulse width is inverted to give the TDC output (2.19).

$$\text{TDC}_{\text{out}}(n) = \frac{1}{p(n)} = \frac{1}{(N/f_{\text{vco}}(n)2\tau_{\text{buff}}) + (\sqrt{N}q(n)/\tau_{\text{buff}})}. \quad (2.19)$$

The TDC output is simplified for analysis

$$\begin{aligned} \text{TDC}_{\text{out}}(n) &= \frac{1}{(N/f_{\text{vco}}(n)2\tau_{\text{buff}}) + (\sqrt{N}q(n)/\tau_{\text{buff}})} \\ &\cdot \frac{(N/f_{\text{vco}}(n)2\tau_{\text{buff}}) - (\sqrt{N}q(n)/\tau_{\text{buff}})}{(N/f_{\text{vco}}(n)2\tau_{\text{buff}}) - (\sqrt{N}q(n)/\tau_{\text{buff}})}, \end{aligned} \quad (2.20)$$

$$\text{TDC}_{\text{out}}(n) = \frac{(N/f_{\text{vco}}(n)2\tau_{\text{buff}}) - (\sqrt{N}q(n)/\tau_{\text{buff}})}{(N/f_{\text{vco}}(n)2\tau_{\text{buff}})^2 + (\sqrt{N}q(n)/\tau_{\text{buff}})^2}. \quad (2.21)$$

Assuming the second term in the denominator of (2.21) is much smaller than the first, the TDC output can further be simplified (2.22):

$$\text{TDC}_{\text{out}}(n) \approx \frac{2\tau_{\text{buff}}f_{\text{vco}}(n)}{N} - \frac{4\sqrt{N}\tau_{\text{buff}}f_{\text{vco}}^2(n)q(n)}{N^2}. \quad (2.22)$$

Plugging in (2.2), the TDC output is approximately (2.23):

$$\text{TDC}_{\text{out}}(n) \approx \frac{2\tau_{\text{buff}}[f_c + K_v x(n)]}{N} - \frac{4\sqrt{N}\tau_{\text{buff}}[f_c + K_v x(n)]^2 q(n)}{N^2}. \quad (2.23)$$

One thing to note is that the quantization noise changes when the input signal changes. There is some correlation between the noise and input signal which is

nonlinear. For simplification, this correlation is ignored and the final TDC output is given as follows (2.24):

$$\text{TDC}_{\text{out}}(n) \approx \frac{2\tau_{\text{buff}}[f_c + K_v x(n)]}{N} - \frac{4\sqrt{N}\tau_{\text{buff}}f_c^2 q(n)}{N^2}. \quad (2.24)$$

Based on (2.24), the STF and NTF for the TDC VCO-based quantizer are derived in (2.25) and (2.26).

$$\text{STF} = \frac{\text{TDC}_{\text{out}}(n)}{x(n)} = \frac{2\tau_{\text{buff}}K_v}{N}. \quad (2.25)$$

$$\text{NTF} = \frac{\text{TDC}_{\text{out}}(n)}{q(n)} = \frac{4\sqrt{N}\tau_{\text{buff}}f_c^2}{N^2}. \quad (2.26)$$

From the derivations, the input signal and noise are both scaled and dependant on some of the same factors. To derive the SNR, the power of the signal and the power of the noise at the output of the TDC are calculated. Consider the input to the VCO as a sine wave (2.11), then the power of the output signal is given in (2.27).

$$P_s = \left(\frac{2\tau_{\text{buff}}K_v A_m}{N\sqrt{2}} \right)^2. \quad (2.27)$$

The power of the quantization noise is derived next. The quantization noise is assumed to be white and thus the level of noise is constant across all frequencies and equal to (2.28) using the two-sided definition of power [5, pp. 532–533].

$$q(n) = \frac{\Delta}{\sqrt{12}f_s} = \frac{\tau_{\text{buff}}}{\sqrt{12N}f_s}, \quad (2.28)$$

where Δ is the difference between quantization levels, in the TDC case this is equal to τ_{buff} . The effective sampling frequency is increased by N when using N TDCs to reduce the quantization noise. The noise is filtered through the NTF and the in-band power given a bandwidth equal to f_b is given in (2.29) and (2.30) using (2.26) and (2.28).

$$P_N = 2 \int_0^{f_b} \left(\frac{4\sqrt{N}\tau_{\text{buff}}f_c^2}{N^2} \frac{\tau_{\text{buff}}}{\sqrt{12N}f_s} \right)^2 df = 2 \int_0^{f_b} \left(\frac{4\tau_{\text{buff}}^2 f_c^2}{N^2 \sqrt{12}f_s} \right)^2 df, \quad (2.29)$$

$$P_N = \frac{32f_b \tau_{\text{buff}}^4 f_c^4}{N^4 12f_s}. \quad (2.30)$$

The SNR (2.31) is the power of the signal divided by the power of the noise, (2.27) divided by (2.30).

$$\text{SNR} = 10\log_{10} \left(\frac{((2\tau_{\text{buff}}K_v A_m)/(N\sqrt{2}))^2}{(32f_b\tau_{\text{buff}}^4 f_c^4)/(N^4 12f)} \right) = 10\log_{10} \left(\frac{3f_s(NK_v A_m)^2}{4\tau_{\text{buff}}^2 f_c^4 f_b} \right). \quad (2.31)$$

The maximum SNR of the TDC VCO-based quantizer depends on the number of TDCs, the ratio of the OSR, the VCO gain factor, and also depends on the VCO center frequency and buffer delay. To the author's knowledge, this is the first time these equations have been derived. TDCs are traditionally used to detect the time or phase difference of two signals, but have not been used to detect the frequency of a signal.

2.3.2 Model Verification Using VerilogA

To verify the above analysis and make further assessment, the TDC VCO-based quantizer is modeled in VerilogA and shown below.

```
//Begin VerilogA code: TDC VCO-based quantizer
`include "constants.vams"
`include "disciplines.vams"
`define PI 3.14159265

module tdc(in, clk1,clk2,clk3,clk4,clk5 ,out);
input in,clk1,clk2,clk3,clk4,clk5,;
output out;
electrical in,clk1,clk2,clk3,clk4,clk5,out;

parameter real      tbuff= 33p,    // Buffer Delay
                   vdd = 0.6,      // Positive power supply
                   vss = -0.6,     // Negative power supply
                   fc=500M,        // VCO center frequency
                   Kv=250M;         // VCO gain factor Hz/V
parameter           N=5,           // Number of TDCs
                   n = 150;        // Length of delay chain

// Define variables
integer q1[0:n-1],q2[0:n-1],q3[0:n-1],q4[0:n-1],q5[0:n-1]
integer i,vs11,vs12,vs21,vs22,vs31,vs32,vs41,vs42,vs51,vs52;
real Ac,vmid,phase,fvco,vcout,vp1,vp2,vp3,vp4,vp5,vp, d[0:n-1];
```

```

analog begin
//Initialize parameters
  @(initial_step) begin
    Ac=(vdd-vss)/2.0;    // VCO amplitude
    vmid=(vdd+vss)/2.0;  // Midrail Voltage
  end
// Ideal VCO equations
  fvco=Kv*V(in)+fc;      // VCO frequency
  phase=2.0*PI*idtmmod(fvco,0,1,-0.5); // VCO phase
  vcout=vmid+Ac*sin(phase); // VCO output
// Delay the VCO pulse along the delay chain
  @(timer(0,tbuff)) begin
    for(i=1;i<n;i=i+1) begin
      d[n-i]=d[n-i-1];
    end
    d[0]=vcout;
  end
// Calculate the detected pulse width using TDC
// TDC1
  @(cross(V(clk1)-vmid,1)) begin
    for(i=0;i<n;i=i+1) begin // Buffer VCO output
      q1[i]=(d[i]>=vmid);
    end
    for(i=1;i<n;i=i+1) begin // Determine pulse width
      if (q1[i]==1 && q1[i-1]==0) vs11=i;
      if (q1[i]==0 && q1[i-1]==1) vs12=i;
    end
    vp1=abs(vs11-vs12); // Pulse width
  end
// TDC2
  @(cross(V(clk2)-vmid,1)) begin
    for(i=0;i<n;i=i+1) begin
      q2[i]=(d[i]>=vmid);
    end
    for(i=1;i<n;i=i+1) begin
      if (q2[i]==1 && q2[i-1]==0) vs21=i;
      if (q2[i]==0 && q2[i-1]==1) vs22=i;
    end
    vp2=abs(vs21-vs22);
  end
// TDC3
  @(cross(V(clk3)-vmid,1)) begin
    for(i=0;i<n;i=i+1) begin
      q3[i]=(d[i]>=vmid);
    end
    for(i=1;i<n;i=i+1) begin
      if (q3[i]==1 && q3[i-1]==0) vs31=i;
      if (q3[i]==0 && q3[i-1]==1) vs32=i;
    end
    vp3=abs(vs31-vs32);
  end
end

```



```

// TDC4
    @(cross(V(clk4)-vmid,1)) begin
        for(i=0;i<n;i=i+1) begin
            q4[i]=(d[i]>=vmid);
        end
        for(i=1;i<n;i=i+1) begin
            if (q4[i]==1 && q4[i-1]==0) vs41=i;
            if (q4[i]==0 && q4[i-1]==1) vs42=i;
        end
        vp4=abs(vs41-vs42);
    end
// TDC5
    @(cross(V(clk5)-vmid,1)) begin
        for(i=0;i<n;i=i+1) begin
            q5[i]=(d[i]>=vmid);
        end
        for(i=1;i<n;i=i+1) begin
            if (q5[i]==1 && q5[i-1]==0) vs51=i;
            if (q5[i]==0 && q5[i-1]==1) vs52=i;
        end
        vp5=abs(vs51-vs52);
    end
    @(cross(V(clk1)-vmid,1)) begin
// Add TDC outputs
        vp=vp1+vp2+vp3+vp4+vp5;
    end
// Convert to frequency
V(out)<+1.0/vp;
end
endmodule
//End VerilogA code: TDC VCO-based quantizer

```

The input to the VerilogA model is the clock signals and the input to the VCO. The VCO is modeled using the ideal relationships, delayed along the chain, buffered, and then fed to each TDC (five TDCs in this case). At the rising clock edge of each TDC, the pulse width is determined. The output of the model is the inverted sum of the TDCs.

To verify the theoretical analysis, multiple simulations of the VerilogA code are run varying different circuit parameters, Fig. 2.15. The theoretical analysis shows good correlation with the VerilogA model with some slight variations due to approximation.

2.4 FDC vs. TDC Architecture

So far, theoretical modeling and analysis has been developed for both the FDC and TDC VCO-based quantizers. The theoretical analysis is verified through a VerilogA model. The VerilogA model will be used to make further comparisons between the two quantization methods. The VCO-based quantizers are designed to achieve an SNR = 60 dB. The design parameters are chosen to produce the desired SNR and outlined in Table 2.1, where the same baseline VCO is used in

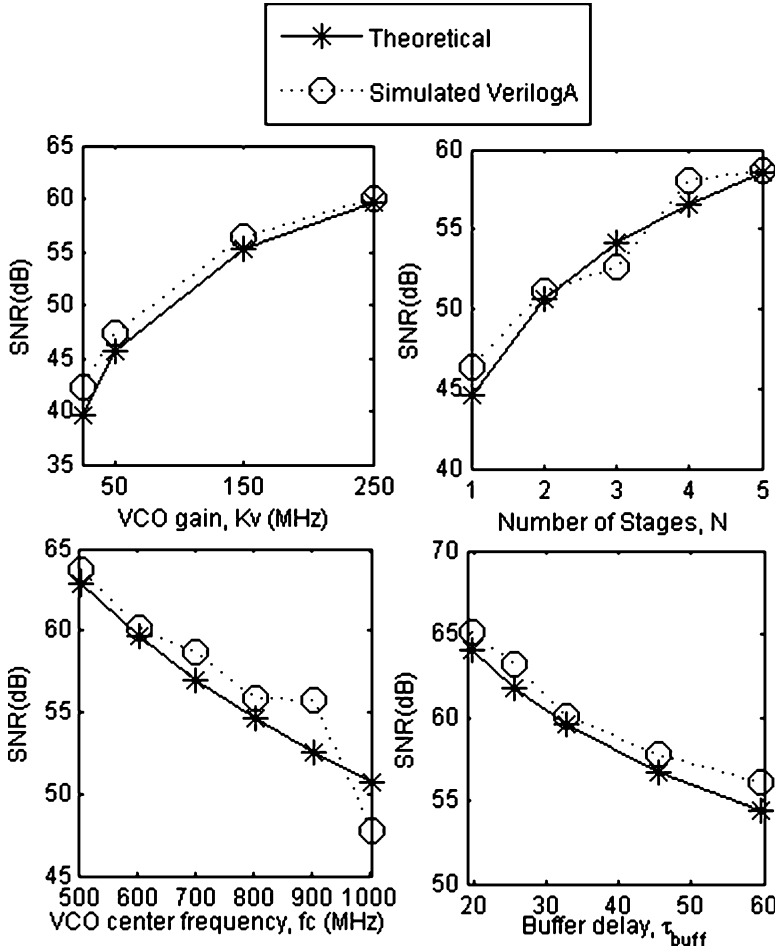


Fig. 2.15 TDC VCO-based quantizer SNR curves while varying design parameters: theoretical vs. simulated VerilogA model

Table 2.1 FDC/TDC design parameters to achieve SNR

Design parameters	FDC	TDC
f_s (GHz)	2	2
f_b (MHz)	10	10
A_m (V)	0.6	0.6
f_c (MHz)	500	500
K_v (MHz/V)	250	250
N	5	5
τ_{buff} (ps)	–	32.579

both quantizers. The theoretical SNR for this combination is shown in (2.32) and (2.33) for the FDC and TDC, respectively.

$$\text{SNR} = 10\log_{10}\left(\frac{9f_s^3(2NT_sK_vA_m)^2}{4\pi^2f_b^3}\right) = 60.11 \text{ dB}, \quad (2.32)$$

Table 2.2 FDC/TDC
time domain simulation
parameters

Simulation parameters	
$V_{DD} - V_{SS}$ (V)	1.2
f_m (kHz)	500
T_{start} (μ s)	2
T_{stop} (μ s)	100
$T_{simulator}$ (ps)	250
Points	392,000

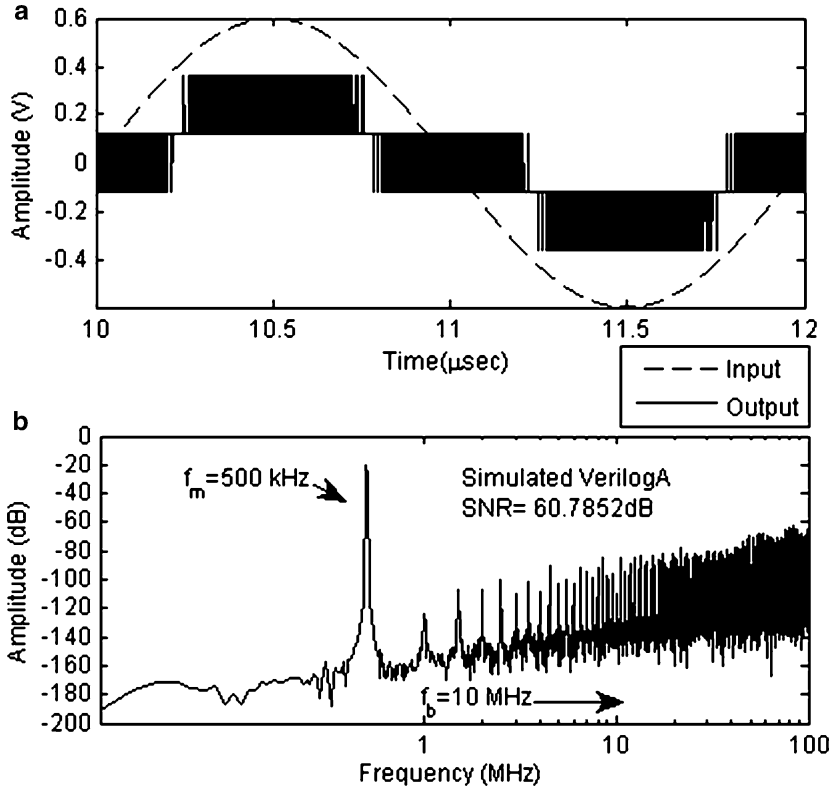


Fig. 2.16 Simulated VerilogA model FDC VCO-based quantizer: (a) input vs. output (time domain); (b) output (frequency domain)

$$SNR = 10\log_{10}\left(\frac{3f_s(NK_vA_m)^2}{4\tau_{buff}^2f_c^4f_b}\right) = 61.03 \text{ dB.} \quad (2.33)$$

For simulation purpose, Table 2.2 is given.

The results for both VCO-based quantizers are shown in both time domain and frequency domain, where the output FFT is Hann windowed. The FDC results are shown in Fig. 2.16 and the TDC results are shown in Fig. 2.17. The simulated VerilogA SNR closely matches the theoretical SNR.

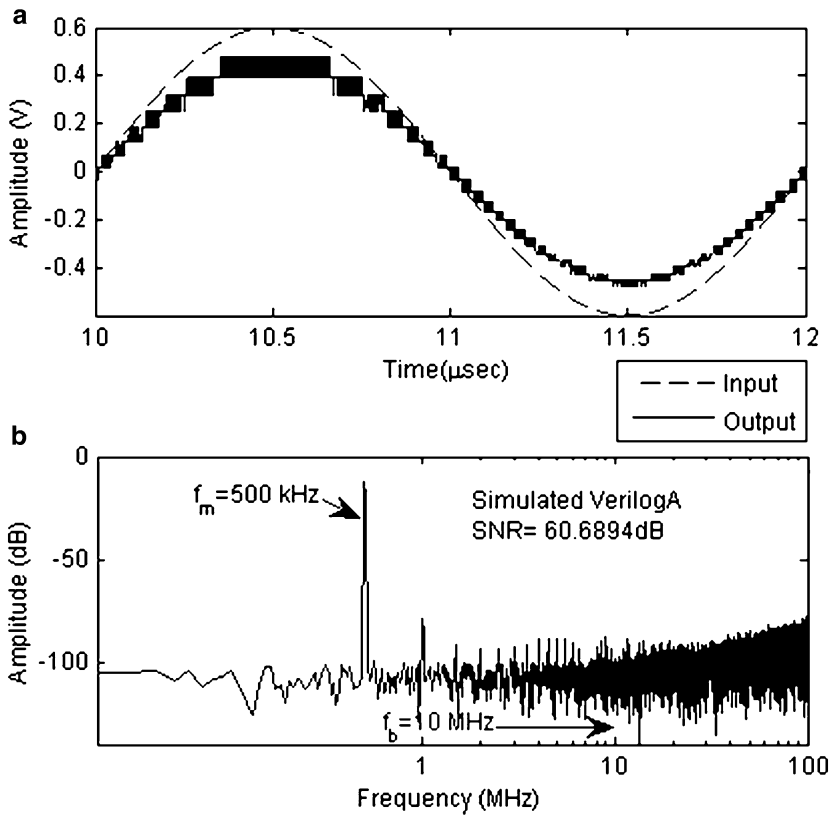


Fig. 2.17 Simulated VerilogA model TDC VCO-based quantizer: (a) input vs. output (time domain); (b) output (frequency domain)

2.5 Summary

Theoretical modeling and analysis of the VCO-based quantizer using an FDC and TDC has been developed to determine the resolution of the quantizers and verified through a VerilogA model. To make further comparison between the two quantization methods, the VerilogA models are used to achieve an SNR = 60 dB. The design parameters and characteristics for the two different quantizers are summarized in Table 2.3. Both systems are designed with the same sampling frequency and bandwidth. The VCO for both designs is the same and each quantizer consists of the same number of stages. The FDC has first-order noise shaping while the TDC does not. However, the TDC has two more SNR tuning knobs than the FDC.

Table 2.3 FDC/TDC VCO-based quantizer performance summary

Parameters	FDC VCO-based quantizer	TDC VCO-based quantizer
f_s , sampling frequency (GHz)	2	2
f_b , system bandwidth (MHz)	10	10
f_m $[0:f_b]$, VCO input signal frequency (kHz)	500	500
f_c , VCO center frequency (MHz)	500	500
K_v , VCO gain (MHz/V)	250	250
N , number of stages	5	5
Noise shaping	First order	None
SNR tuning knobs	$\uparrow(f_s, N, K_v)$	$\uparrow(f_s, N, K_v) \downarrow(\tau_{\text{buff}}, f_c)$
SNR (dB)	60.78	60.68

The FDC and TDC VCO-based quantizers will suffer from VCO nonidealities such as VCO nonlinearity and phase noise along with sampling clock jitter. The impact of these nonidealities on the VCO-based quantizer is analyzed and modeled in the next chapter.

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