Preface

These days, everything strongly relies on information. More and more, this information is digitized so that it can be stored and processed efficiently. The storage and processing cost is low and is still lowering thanks to the progress that is and has been made with the production technologies that are used for memories and processors, respectively. This evolution is caused mainly by the continuous scaling of transistors that can be realized on a chip. The consequence of this scaling is that a chip can contain an increasing number of transistors, a law which is generally known as *Moore's Law*. This ensures that more and more functionality can be integrated on a given area, which decreases the cost per function. However, the third cornerstone of information, namely communication, was never exposed to the same favourable development. By contrast with the processing and the storage of information, communication becomes increasingly critical because the applied channels cannot keep up with the high data rates.

Since long, optical communication is used as an alternative for wired and wireless communication networks because it offers a lot of advantages (high speed, low attenuation, low weight, high resistance against interfering signals, etc.), unfortunately at a high cost. Consequently, this type of communication is applied mainly in shared networks, such as transatlantic telephone networks, where the high cost is carried by the large number of users. In order to be able to use optical communication at a smaller scale, the expensive sender and receiver need to be manufactured in a standardized, cheap production technology. CMOS, the technology that is also used for the manufacturing of processors, is the preferred candidate. However, since CMOS is a standard process and is consequently not optimized to interact with light, the performance of the photodetector in this technology is weak compared to what can be achieved in dedicated processes.

The focus of the presented work is on the integration of the complete functionality of an optical receiver on a single CMOS chip. Due to the low speed and sensitivity of an integrated photodiode in this technology, innovative solutions are required both at the circuit and at the layout level. Therefore, a new photodiode is presented in this book that combines the speed of a differential photodiode and the sensitivity of a regular photodiode. The inherent disadvantage of a differential photodiode, namely the fact that half of the impinging light is reflected, is avoided with this *speed-enhanced*

photodiode. The innovations on the circuit level can be found in the transimpedance amplifier as well as in the equalizer and the post amplifier. For example, to reduce the effect of the parasitic capacitance of the photodiode on the bandwidth of the transimpedance amplifier, the *capacitance-relieved TIA* is introduced. This topology enables the bandwidth of the circuit to be increased significantly without boosting the noise excessively. In addition, innovations are presented for the equalizer and the post amplifier which improve their performance considerably compared to the current state-of-the-art. This way, the problems of every building block of an optical receiver are dealt with in this work.

In order to demonstrate the functioning of the proposed concepts in a realistic situation, a number of chips is discussed. The first chip implements the functionality of an optical receiver in a 130 nm CMOS technology. The integrated differential photodiode has a diameter of 60 µm so that this receiver can be used together with a multi-mode fiber. Additionally, this chip has a differential transimpedance amplifier, a differential equalizer and a post amplifier. Signals with a maximum bit rate of 4.5 Gbit/s can be received while the bit error ratio is below 10^{-12}. The sensitivity equals −3.4 dBm. The total power consumption of this receiver is 74.2 mW, which is low compared to the current state-of-the-art.

The second presented optical receiver has a similar architecture and is implemented in the same 130 nm CMOS technology. However, a *speed-enhanced photodiode* is used instead of a differential photodiode. Consequently, the maximum bit rate rises to 5.5 Gbit/s, while the power consumption drops to 58.6 mW. As before, the sensitivity is −3.4 dBm.

The subsequent optical receiver discussed in this book has an integrated photodiode with a diameter of 1 mm, which is the same as the diameter of a plastic optical fiber. The related capacitance of this large photodiode in the used 180 nm CMOS technology equals 63.6 pF. This chip enables the reception of signals with a bit rate of 300 Mbit/s if the optical input power is between −14.5 and −9 dBm. Raising the supply voltage from the nominal 1.12 to 1.42 V, increases the maximum bit rate to 500 Mbit/s if the input signal has a power between −15 and −9.1 dBm.

The final chip that is discussed implements a post amplifier in a 90 nm CMOS technology. In order to realize the large time constant that is required by the offset compensation circuit, a new technique is used that boosts the capacitance of the integrated capacitor. Consequently, a larger time constant can be realized on a smaller area. The post amplifier delivers a gain of 35 dB and has a bandwidth of 4.15 GHz. The cut-off frequency due to the offset compensation circuit equals 1.86 MHz. The total power consumption of this chip is 14.7 mW, which is very low in comparison with the current state-of-the-art.

http://www.springer.com/978-1-4419-9924-5

High-Speed Optical Receivers with Integrated Photodiode in Nanoscale CMOS

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2011, XIV, 226 p., Hardcover
ISBN: 978-1-4419-9924-5