Thermoelectric Effects in Current Induced Crystallization of Silicon Microstructures

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Abstract

We have observed melting of nanocrystalline silicon microwires self-heated through single high-amplitude microsecond voltage pulses which leads to growth from melt upon resolidification. The resolidified regions form two single-crystal domains for wires with sub-micrometer widths. The current densities (J) involved in this process are ~ 1-10 MA/cm^2 for suspended wires, and ~ 10-100 MA/cm^2 for wires on oxide. These extremely high current densities and the resulting high temperatures (~ 1700 K) and temperature gradients (~ 1 K/nm) along the microwires give rise to strong thermoelectric effects. The thermoelectric effects are characterized through capture and analysis of light emission from the self-heated wires biased with lower magnitude AC voltages (J < 5 MA/cm^2). The hottest spot on the wires consistently appears closer to the lower potential end for n-type, and the higher potential end for p-type microwires. Experimental light emission profiles are used to verify the linear thermoelectric models and material parameters used for simulations. Good agreement between these experimental and simulated profiles indicates that the linear models can be used to predict the thermal profiles for current induced crystallization of microstructures. However, the linear models are expected to be insufficient to fully explain the thermoelectric processes for higher current densities and stronger thermal gradients that are generated by high-amplitude short duration pulses.

Introduction

Polycrystalline (poly-Si), amorphous (a-Si) and nanocrystalline silicon (nc-Si) are commonly used for large area electronics such as flat panel displays [1], x-ray imaging arrays [2] and solar cells. Currently a-Si is used for silicon thin film transistors (TFTs) for large area electronics [1] due to its uniformity and low-temperature processing, despite its relatively low electrical carrier mobility [3]. There is a growing demand for displays and sensors on larger areas, using flexible and shatter-proof substrates like plastics, that can operate at higher speeds and sensitivities. Large areas require uniformity, flexible substrates require low temperature processing, and higher speed and sensitivity require use of crystalline material instead of amorphous. Cost effective techniques to achieve single-crystal Si on arbitrary substrates will also enable significant technological advancements, such as integration of high performance circuitry with displays or sensor arrays as complete systems.

The interest in achieving high speed circuitry for large area electronics has motivated studies on crystal growth on glass and plastics [4], transfer of crystalline structures onto glass and plastic substrates, and crystallization of low temperature deposited silicon [1, 2, 5].

Crystallization of low temperature deposited a-Si films is a promising approach that has been studied in the past decades. This requires thermal processing of a-Si. High temperature annealing of a-Si films typically results in polycrystalline films. However, it has been reported that patterning the films to form microstructures with widths smaller than 250 nm can result in growth of single crystals along the length with preferred crystal orientation. Metal induced crystallization [6, 7] reduces the required temperature significantly, making it more compatible with low-temperature substrates but there are some concerns regarding the metal contamination in the crystallized films [8].

Local heating techniques, where the energy required for heating is directly delivered to the film or the patterned structures, allow the substrate to remain at room temperature. These techniques include sequential lateral solidification using an excimer laser [9, 10], rapid melting and growth from melt using self-heating [11] or microfabricated heaters atop the structures [12]. Some of the laser annealing techniques, such as sequential lateral crystallization, are currently in industrial use.

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The approach described in this paper is crystallization of nc-Si microwires through single microsecond voltage pulses (J < 10 MA/cm^2) leading to self-heating, melting and growth from melt in a very short time (~ 1 μs). Larger current densities (J~20 MA/cm^2) are required for further reduction in voltage pulse duration (d ~ 20 ns). The short duration local heating of the structures to be crystallized makes this approach compatible with low-temperature substrates. Real-time current-voltage measurements can be made on these structures during the crystallization process which can help understanding the mechanisms involved. The extreme thermal gradients (~1 K/nm) and the short time scales involved in these experiments are similar to those in pulse laser annealing. The main differences in this case are due to formation of molten filaments in the current path and thermoelectric effects which appear to be very strong under the extremely high electric current densities during the voltage pulse. Here, we give an overview of our experimental observations on melting, growth from melt and thermoelectric effects, and computational studies on heating and cooling of the wires including the role of thermoelectric effects.

Fabrication

The microwires are patterned on n- and p-type nc-Si films deposited on oxidized single crystal Si wafers (~500 nm SiO_2) in a low pressure chemical vapor deposition (LPCVD) system at 580 C or 600 C with phosphorous doping or at 560 C with boron doping ([P], [B] > 10^{20} cm^{-3}). The room temperature resistivities of the n-type films deposited at 580 and 600 C are 30.4 ± 5.6 and 23.0 ± 0.3 mΩ.cm, respectively, and resistivity of p-type film is 12.9 ± 0.3 mΩ.cm. Some of the microwires are suspended by etching the underlying oxide using buffered oxide etch. The wires' dimensions range from 0.5 to 5.5 μm in length and 100 nm to 1 μm in width. Metal extensions (Ti/Al stack) are deposited to form ohmic contacts to the Si pads.

Microsecond voltage pulse crystallization

The experiments are conducted using a semiconductor probe station, a parameter analyzer, a pulse generator unit (PGU), and an oscilloscope. I-V characteristics of the microwires are measured before and after the voltage pulses using the parameter analyzer. The applied voltage and current through the microwire are measured by the oscilloscope during the pulse. Tungsten needles are used to probe the metal contacts or the silicon contact regions of microwires without metal extensions [13].

The melting of the wires is verified by extracting the wire resistivity during the pulse. This is achieved by calculating the resistance of a number of structures with different widths and lengths, yielding to resistivity of 73.3 ± 3.9 μΩ.cm [13, 14]. This value is in good agreement with previous reports on liquid Si resistivity of 83 μΩ.cm by Glazov et al.[15], 75.2±0.6 μΩ.cm by Schnyders et al.[16] and 72 μΩ.cm by Sasaki et al.[17]. Liquid silicon at melting temperature is reported to be ~10% denser than silicon at solid phase at room temperature [15], which scales down the extracted liquid silicon resistivity value to 66.0 ± 3.5 μΩ.cm.

Melting of the wires requires less current and the mechanical stress induced by the substrate is eliminated if the wires are suspended by removing some of the underlying oxide. The heat loss from the suspended wires is predominantly to the contact regions at the two ends. The as-fabricated suspended microwires, wide and thin with uniform nanocrystalline texture, as seen in scanning electron microscope (SEM) images taken after the pulse (Fig. 1a), acquire a cylindrical shape with smooth surfaces (due to surface tension) and a lump in the middle (Fig. 1b) upon melting and resolidification. The as-fabricated structures have compressive stress, seen as sagging of the structures after the release (Fig. 1a). The recrystallized wires are stretched between the contact pads indicating a tensile stress. The resolidification process starts from the silicon pads and move towards the middle of the microwire. Some of the liquid silicon cannot fit in the middle as the two solid-liquid fronts meet, since silicon expands as it solidifies. Excess silicon is ejected and forms a lump after resolidification (Fig. 1b). The microwires which experience longer duration pulses show tapering and breaking (Fig. 1c) through silicon migration towards the silicon pads. Strong thermal gradient along the suspended microwires, due to low heat loss to the substrate, is expected to suppress nucleation along the wire and consequently limits the number of grains to two, one starting from each end.

The conductance of the microwires is enhanced after the voltage pulse. Fig. 1b shows a 3.5 μm long microwire with pre-pulse total resistance of 56.7 kΩ. The total resistance (R_{Si}) consists of the microwire (~10 kΩ) and Si pad resistances (~40 kΩ). After the voltage pulse, the total resistance of the microwire in Fig. 1b was measured as 22.2 kΩ which is smaller than the pre-pulse Si pad resistance. Low post-pulse resistance is attributed to conductance enhancement in both the microwires and the contact regions, even though the changes in the contact regions are not observable under SEM in this case. Resistivity of the pulsed, unbroken microwires is reduced by a factor of up to10x [18] indicating crystal growth rather than solidification in amorphous form.

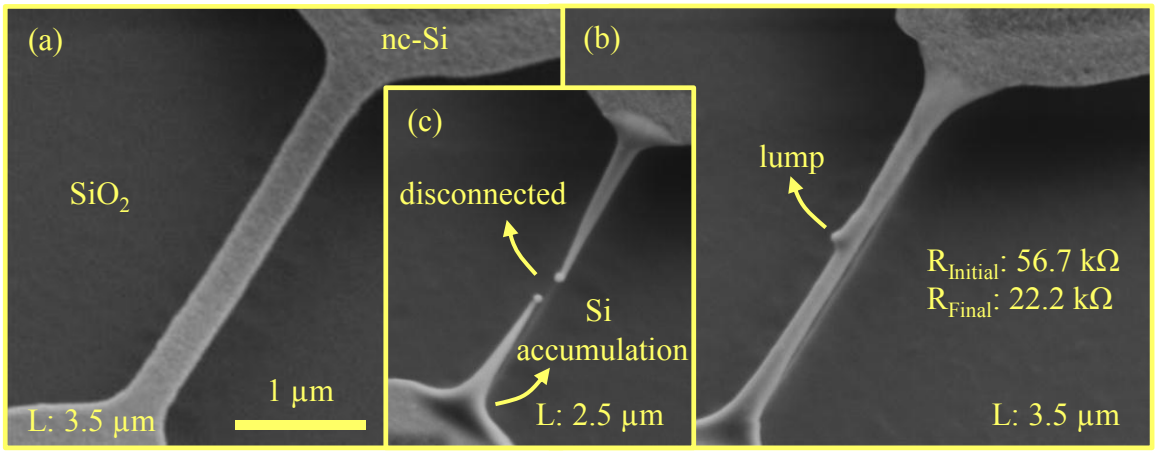

Fig. 1 (a) An as-fabricated, n-type, suspended microwire, and two microwires after (b) 40 V, 1 µs and (c) 40 V, 2 µs pulse. Resistance of the wire in b) decreased significantly after the pulse [19]

Capture and analysis of light emission from the microwires under long duration biases

The microsecond pulsing of the microwires results in very high current densities (1-100 MA/cm^2). The peak temperature on the wire reaches the melting temperature of Si (1690 K) while the contact pads remain at room temperature, leading to thermal gradients on the order of ~1 K/nm. Thermoelectric effects are expected to be very significant at such current densities and thermal gradients [20, 21]. The transient effects in the short time scales involved in melting and crystallization in these experiments are difficult to probe. However, it is possible to gain some information about the steady-state temperature profile and the thermoelectric effects from the light emission from the wire as it is heated up to ~1000 K and beyond. This allows for verification of the high temperature materials parameters and models used for the computational studies.

The first optical observation of thermoelectric effects in a single material system (Thomson effect) was reported by Mastrangelo et al. [22]. The authors observed that the peak light intensity (hottest spot) on p-type poly-Si micro-lamps was shifted from the center toward the higher potential end (V+). Englander et al. [23] observed a similar asymmetric light emission profile shifted towards the lower potential terminal in n-type poly-Si micro-heaters. Jungen et al. [24] also reported a shift towards the lower potential end for self-heated, n-type poly-Si, micro-bridges.

Thermoelectric effects (thermoelectricity) is due to the coupling of electronic and heat transport through heat transfer by charge carriers. Direct electrical-thermal energy conversion for power generation, solid-state cooling [20, 21] and characterization of semiconductor materials [25] are the most common applications of thermoelectricity. Thermoelectricity can be observed as an open-circuit voltage across a temperature difference in a circuit of two different materials (Seebeck effect), heating or cooling at a current-passing junction between two different materials (Peltier effect) and heating or cooling along a current carrying homogeneous material under a temperature gradient (Thomson effect). The Seebeck voltage polarity and heating versus cooling for Peltier and Thomson effects depend on temperature-dependent thermoelectric properties of the material and directions of temperature gradient and electric current. The three thermoelectric effects are characterized by the Seebeck (S), Peltier (Π) and Thomson (β) coefficients which are interrelated by the fundamental Kelvin relationships [21]:

$$\Pi = ST \quad , \tag{1}$$

$$\beta = T\frac{dS}{dT} \tag{2}$$

Thomson effect results in skewing of temperature profiles and is typically very small in macroscopic structures; however, it is significant in self-heated small-scale structures such as micro-lamps [22] and micro-heaters [23, 24] as mentioned above, as well as phase-change memory (PCM) elements [26], due to large current densities and temperature gradients. In all of these cases of self-heating at high temperatures, the hottest spot along the structures appears closer to the lower potential end (V-) for n-type structures and closer to the higher potential end (V+) for p-type structures, in agreement with expected high-temperature positive Thomson coefficient for n-type ($\beta > 0$) and negative Thomson coefficient for p-type ($\beta < 0$) materials.

DiCastro et al. [26] have calculated a Thomson coefficient of -100 µV/K for SbTe above room temperature using an analytical solution for the hottest spot location and indicated that a 5% reduction in RESET current was obtained in

asymmetric PCM structures due to Thomson effect. However, changes in the material during the heating process can contribute to the asymmetry in the temperature profile and hence the observed asymmetries may be larger than what is due to the pure contribution of thermoelectric effects.

In our experiments, we have recorded videos of light emission from self-heated nc-Si microwires using a high magnification optical setup and a commercial high-definition (full HD) camcorder at 30 frames per second. The wires self-heated to sufficiently high temperatures (T > 800 C [23]) emit light in the visible range. The speed of the measurement is limited by the sensitivity and the frame rate of the camera. Hence, the light emission from the wires was observed for low frequency AC signals at ~ 1 Hz. The light intensity profiles along the microwires and shift in the brightest (hottest) spot are extracted from the videos using MATLAB.

Fig. 2a-b show glowing of a 2.5 μm long, suspended, n-type microwire during positive and negative cycles of an AC signal generated by the parameter analyzer. The hottest spot on the microwire alternates position as the current direction changes, confirming that the shift of the hottest spot is not caused by any asymmetric geometrical or thermal boundaries, but is due to thermoelectric effects.

Fig. 2c shows current through the microwire and the shift in the hottest spot location as a function of time. The shift in the hottest spot for either cycle of the AC signal is approximately 250 nm (10% of the length).The shift in the hottest spot for the negative cycle gradually increases over time, showing a memory effect. Similar behavior is observed on other wires when they are biased with opposite polarity of the previous bias.

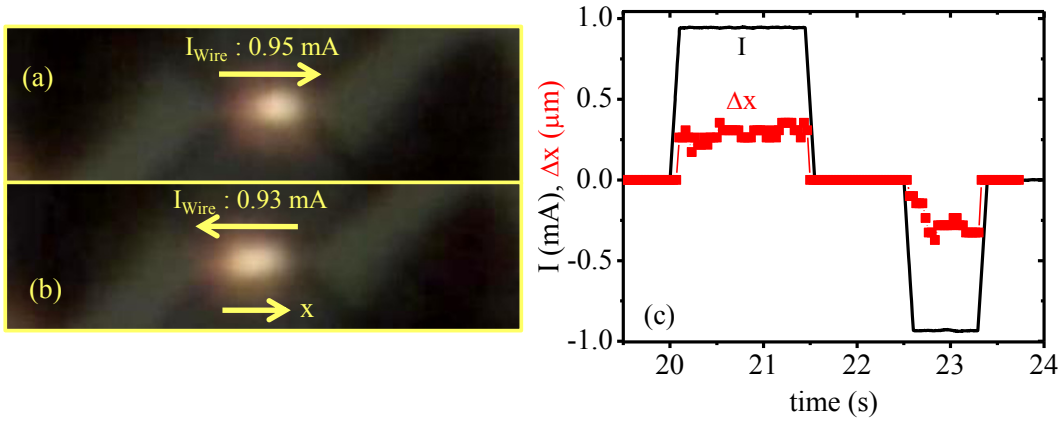

Fig. 2 A 2.5 μm long, suspended, n-type microwire during the (a) positive and (b) negative cycle of an applied square wave with ~ 0.95 mA (~3 MA/cm^2) amplitude. Current levels and directions are as indicated. Wire center is located at x= 0. (c) Current (I) through the microwire and shift (Δx) in the hottest spot location as a function of time [19]

Numerical modeling

The experimental results are complemented by finite element analysis of a 2.5 μm long, suspended, n-type microwire using COMSOL Multiphysics software [27] including the thermoelectric effects, using the parameters available in the literature. The thermoelectric effects are included in both current continuity and heat transfer equations [28]:

$$\nabla . J = -\nabla . \left(\frac{\nabla V + S \nabla T}{\rho} \right) = 0 \,, \tag{3}$$

$$d_{Si} C_P \frac{dT}{dt} - \nabla . (k \nabla T) = \rho J . J - TJ . \nabla S \,, \tag{4}$$

where d_{Si} is the density, C_P is the specific heat, k is the thermal conductivity, ρ is the electrical resistivity and S is the Seebeck coefficient. The thermoelectric term ($-TJ\nabla S$) in Eq. 4 reduces to the Thomson heat for homogeneous structures ($-\mathrm{d}S/\mathrm{d}T J\nabla T$).

The resistivity of the microwire is modeled as an exponentially decaying function from its room temperature value of 23 mΩ.cm to the melting temperature value of 3 mΩ.cm [17], following the trend of the measured resistivity in the 300 - 650 K range ($\rho = 3.2+195.5e^{-T/142}$ mΩ.cm). Temperature dependent thermal conductivity and Seebeck coefficient are not yet characterized for the heavily doped nc-Si used for the fabrication of the wires, nor are there any thermal conductivity or Seebeck coefficient data available in the literature on nc-Si, to the best of our knowledge. Hence, an inverse polynomial extrapolation function given in Ref. [29], fitting the experimental thermal conductivity of heavily-doped poly-Si in the 300 K to 800 K range, is used. Similarly, Seebeck coefficient of heavily doped poly-Si ([P] ~ 10^{20} cm^{-3}) is used at low temperature

range (150 K – 450 K) [30] and Seebeck coefficient of poly-Si with [P] = 6x 10^{17} cm^{-3} is used at high temperature range (700 K – 1350 K) for modeling [31]. The Seebeck coefficient in the 450 K – 700 K range is extrapolated linearly from these two poly-Si data sets which intersect at ~ 800 K, and it is also linearly extrapolated in the range between 1350 K – 1690 K using the high temperature data. Density and specific heat of c-Si are close to those of poly-Si and a-Si [32] and change only slightly with temperature, therefore constant (room temperature) c-Si values [27] are used. The room temperature values of the modeling parameters of nc-Si, SiO_2 and c-Si layers are shown in Table 1. Fig. 3a shows the 3D structure used for the modeling of the microwire and the electrical and thermal boundaries. A 5.8 V, 1 µs voltage pulse or square wave (AC) with increasing amplitude is applied across the wire. The current continuity and heat transfer equations including thermoelectric effects are solved self-consistently (Eq. 3 and 4). The modeling of pulsed wires is also performed without thermoelectric effects for comparison.

Table 1 Room temperature values of the physical parameters used for the modeling

	ρ (Ω.cm)	k (W/m.K)	C_P (J/kg.K)	d (kg/m^3)	S (µV/K)
nc-Si	[a,b] $23x10^{-3}$	[c] 54	[d] 703	[d] 2330	[e,f] -105
SiO_2	[d] 10^{16}	[d] 1.38	[d] 703	[d] 2203	-
Si	[d] 10^{-1}	[d] 163	[d] 703	[d] 2330	-

[a]This work, [b]Ref.[17], [c] Ref.[29], [d] Ref. [27],[e] Ref. [30], [f] Ref. [31]

Simulation results for the pulsed wire are seen in Fig. 3. The peak temperature on the wire reaches melting temperature of silicon (1690 K) in 1 µs for 5.8 V, 1 µs voltage pulse (Fig. 3b). The voltage pulse amplitude is chosen to keep the peak temperature on the wire below the melting temperature, since the phase change is not included in the modeling. The time to reach the melting temperature scales down as the voltage pulse amplitude is increased (Fig. 3c). The simulations suggest that the peak temperature on the wire can reach the melting temperature in less than 10 ns for voltage pulse amplitudes larger than 30 V. The cooling time of the wire is less than 250 ns for the given geometry. The simulated temperature profile along the wire just before melting is significantly skewed compared to the profile simulated without thermoelectric effects (Fig. 3d). The peak temperature is closer to lower potential end of the wire, which is in agreement with previous reports and our optical observations. Fig. 3d suggests that the melting of the wire starts on one end and continues until the whole wire melts.

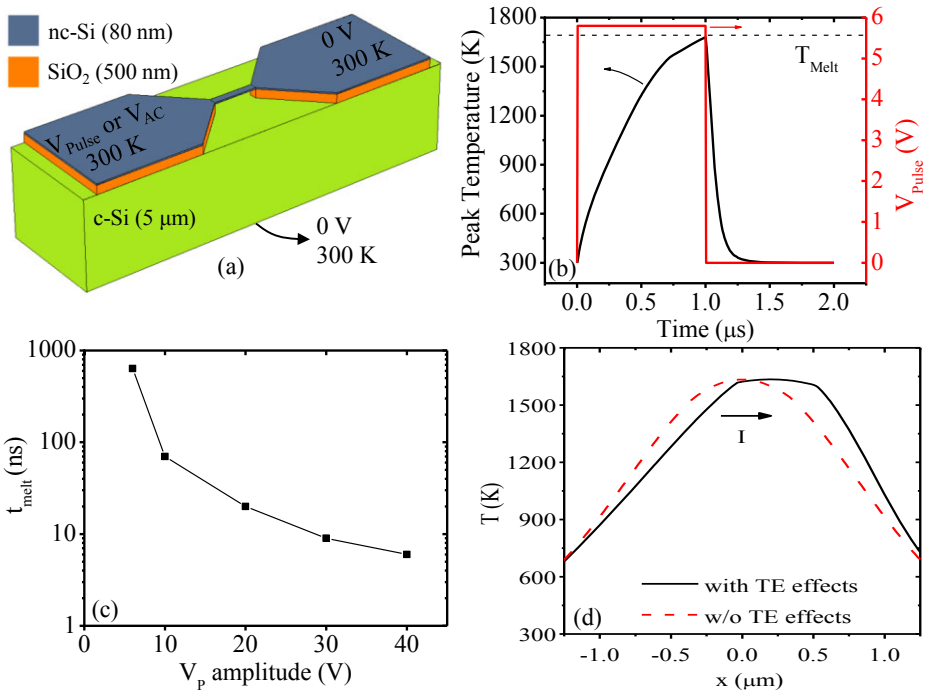

Fig. 3 (a) 3D structure used for numerical modeling. A voltage pulse or a AC signal with increasing amplitude is applied to the square section of the left pad, while the square section on the right pad and the bottom surface of the substrate are set to 0 V. The temperature at these electrical boundaries is kept at 300 K. (b) Simulated peak temperature on the wire during the voltage pulse. (c) Simulated time required to reach the melting temperature of silicon (1690 K) on the wire as a function of voltage pulse amplitude. (d) Simulated temperature along the wire just before reaching melting temperature with and without thermoelectric effects. The arrow indicates the current direction (I: 0.74 mA) [19]

The light emission from the self-heated microwires is expected to be due to black-body radiation [22]. The light emission intensity profiles corresponding to the simulated temperature profiles are calculated using Eq. 5 [22] in the visible range to compare the simulated and experimental light intensity results.

$$E(T) = \int_{\lambda} \varepsilon(\lambda, T) E(\lambda, T) d\lambda \,, \tag{5}$$

where ε(λ,T) is the emissivity of the microwires which is assumed to be constant since it changes only very slightly throughout the visible range for silicon [33].

E(λ,T) is the black-body radiation from the microwire as a function of radiation wavelength and temperature. The calculated light emission is convoluted using a point source approach to emulate the diffraction limited experimental light intensity profiles [34]. Each 1 nm segment of the microwire is assumed to be a point light source with a Gaussian intensity profile as given in Eq 6.

$$I_{Gaussian}(x) = \frac{I(x_{center})}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x - x_{center})^2}{2\sigma^2}} \,, \tag{6}$$

where x_{center} is the point where the Gaussian profile is evaluated, $I(x_{center})$ is the black-body radiation from that point and σ is the width for the profile. The optical resolution of our system, calculated as 1.11λ where λ is the wavelength of the emitted light [34], was used for σ. The intensity profiles from each point source are added together and scaled to have the same peak intensity as the experimental profile.

Fig. 4c shows the experimental (I = 0.95 mA, J~3 MA/cm^2) and simulated light intensity profiles (I = 0.96 mA) showing 250 nm and 154 nm of shift in the hottest spot (Fig. 4a-b), respectively. The simulated light intensity profiles are in good agreement with the experiments, showing the correct direction of the asymmetry and a comparable magnitude for the shift of the hottest spot location. The difference is expected to be due to a mismatch between the actual physical nc-Si parameters (electrical and thermal conductivities and Seebeck coefficient) and those used for the simulation from the literature for similar materials.

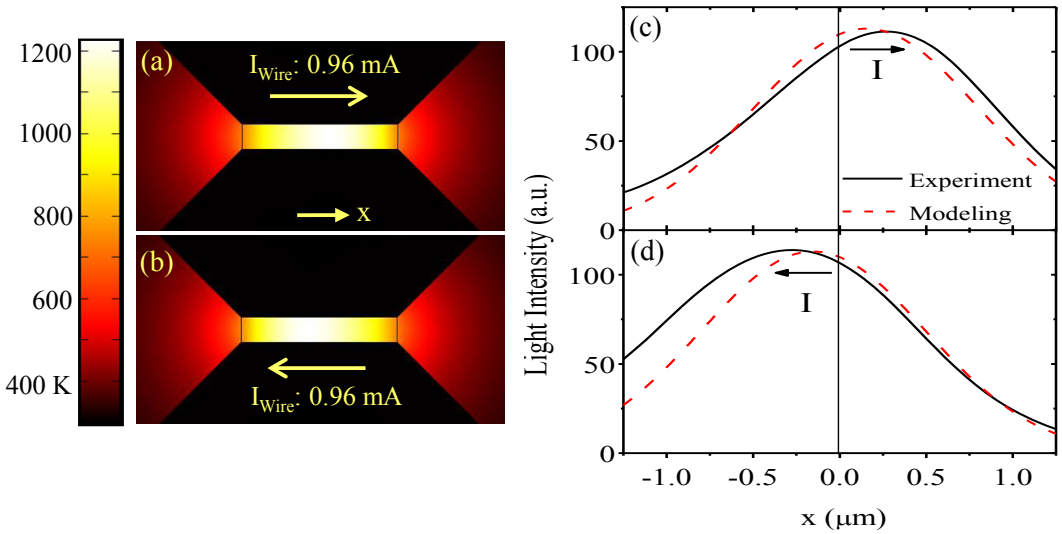

Fig. 4 (a, b) Simulated temperature profiles of the suspended, n-type microwire for indicated current level and direction. Experimental and simulated light intensity for (c) positive and (d) negative voltage cycles. Current direction for each cycle is as indicated. The simulated light intensity profiles are calculated as black-body radiation from the microwires in the visible range, at a current level (0.96 mA) that matches the experimental value [19]

Summary

Nanocrystalline silicon microwires are self-heated, melted and crystallized by microsecond voltage pulses. The crystallized microwires are under tensile stress and typically acquire a cylindrical shape with smooth surfaces. Significant reduction in resistivity of pulsed, suspended microwires indicates crystallization of the microwires upon resolidification, with growth of large single crystal domains.

The extremely high current densities (1-100 MA/cm^2) and temperature gradients (~ 1 K/nm) reached along the microwires result in strong thermoelectric effects as observed through asymmetric heating of the microwires. These thermoelectric effects are analyzed through capture of asymmetric light emission from both n- and p-type microwires during low-frequency AC signals. The hottest spot is always closer to the lower potential end for n-type microwires and closer to the higher potential end for p-type microwires. AC voltage applied to the microwires results in alternating location of the hottest spot, confirming the thermoelectric nature of the observed asymmetric self-heating, rather than being due to any asymmetric geometrical or thermal boundary condition.

Numerical modeling of the thermoelectric transport in an n-type microwire during an AC signal, including temperature dependent physical parameters shows good agreement with the experiments. Simulation results for a microsecond voltage pulsed microwire show significantly skewed temperature profiles for temperatures close to melting temperature of Si, suggesting this model can be used to predict the heating and cooling of microwires during the rapid self-heating and crystallization process.

The findings of this work are relevant for studies on crystallization techniques and thermoelectric effects under high current densities and thermal gradients. Higher performance may be achieved for small-scale electronic devices, such as phase-change memories, by accounting for thermoelectric effects in device design.

Acknowledgements

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