Chapter 2
Predictive Technology Model of Conventional CMOS Devices

Bulk CMOS has been the dominant device structure for integrated circuit design during the past decades, because of its excellent scalability. It is expected that such a device type will continue toward the 10 nm regime. To efficiently predict the characteristics of future bulk CMOS, the scaling trends of primary model parameters, such as the threshold voltage and gate dielectric thickness, need to be identified; their association in determining major device characteristics should be well included for accurate model projection. In this chapter, a new generation of Predictive Technology Model (PTM) for conventional CMOS technology is presented to accomplish these goals. Based on a set of essential device models and early stage silicon data, PTM of bulk CMOS is successfully generated down to the 12 nm node. The accuracy of PTM predictions is comprehensively verified with published silicon data: the error of I_{on} is below 10% for both NMOS and PMOS devices. By tuning only ten primary model parameters, PTM can be easily customized to cover a wide range of process uncertainties. Furthermore, PTM correctly captures the sensitivity to process variations.

2.1 PTM in Light of CMOS Scaling

The relentless scaling of CMOS technology has accelerated in recent years and will arguably continue toward the 10 nm regime [1]. In the nanometer era, physical factors that previously had little or no impact on circuit performance are now becoming increasingly significant. Particular examples include process variations, transistor mobility degradation, and power consumption. These new effects pose dramatic challenges to robust circuit design and system integration. To continue the design success and make an impact on leading products, advanced circuit design exploration must start in parallel with, or even earlier than silicon development. This new design paradigm demands predictive MOSFET models that are reasonably accurate, scalable with main process and design knobs, and correctly capture those emerging physical effects.

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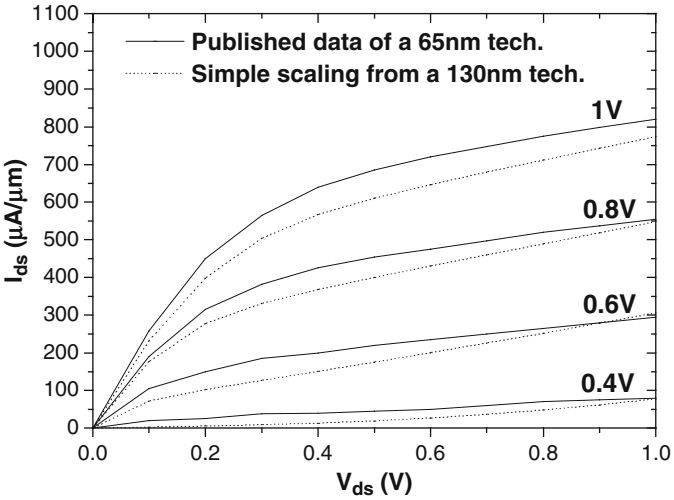

Fig. 2.1 A simple method fails the I-V prediction (Adapted from [8])

To predict future technology characteristics, an intuitive approach would simply scale down the geometry and voltages from an existing technology. For instance, based on the standard MOSFET model, BSIM4 [2], we can shrink the parameters of effective gate length (L_{eff}), equivalent electrical oxide thickness (T_{oxe}), threshold voltage (V_{th0}), drain and source paratactic resistance (R_{dsw}), and supply voltage (V_{dd}) to the target values, while keeping all the other parameters unchanged. However, as shown in Fig. 2.1, this approach is too simple to capture the basic MOSFET behavior. In Fig. 2.1, the I-V characteristics of a preliminary 65 nm technology are predicted based on a well-characterized 130 nm technology by scaling L_{eff}, T_{ox}, V_{th0}, R_{dsw} and V_{dd}. Compared to published measurement data, this simple prediction underestimates the overall performance. This observation matches the fact that during technology scaling, process developers will optimize many other aspects of the device beyond simple geometry scaling, in order to meet all performance criteria.

An improved predictive method was presented by Berkeley Predictive Technology Model (BPTM) [3]. Based on BSIM3 model, BPTM includes more physical parameters into the prediction. Their values are empirically extracted from published data during early stage technology development. Although BPTM provides reasonable models for technology nodes from 180 to 45 nm, its empirical nature constrains the physicality and scalability of the predictions. As the model file for each technology node is independently fitted, the overall scaling trend is not smooth from BPTM, as shown in Fig. 2.2. Furthermore, intrinsic correlations among physical parameters are not sufficiently considered. For instance, the scaling of V_{th0} not only requires the change of channel doping (N_{ch}), but further affects other physical parameters, such as mobility (μ_0), saturation velocity (V_{sat}), the body effect, etc. Insufficient modeling of these correlations limits the prediction accuracy

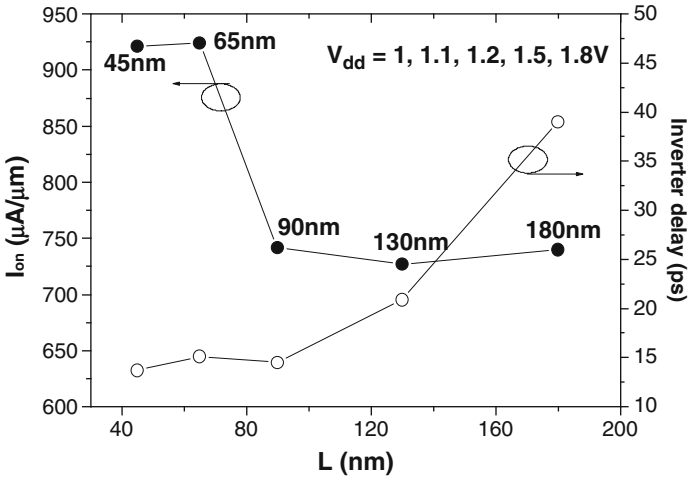

Fig. 2.2 The prediction in BPTM is not smooth with scaling (Adapted from [8])

of process sensitivities. As process variations become increasingly significant in scaled CMOS technology, it is critical to include these parameter correlations into future predictive models, such that robust circuit design can be correctly guided [4].

In this context, a new generation of PTM is developed to overcome these shortcomings. Two cornerstones ensure the accurate and smooth prediction:

1. Essential device physics that governs key device characteristics and parameter correlations. PTM identifies a set of simplified equations for critical electrostatic behavior and carrier transport, rather than the full set of BSIM models. Such simplification allows more transparent correlation between model parameters and device performance; it further facilitates physical prediction of the scaling trends. Given the expectations of device geometry and voltage conditions, these models help project the underlying physical parameters to be tuned.
2. Silicon data from previous technology generations and early stage technology development. A comprehensive collection of published data from various sources provides a practical ground to predict the evolution of CMOS technology. It reflects the limits of CMOS manufacturability and fabrication cost during technology scaling, especially in the definition of device geometries. By recognizing these engineering limits, prediction of PTM is realistic and reasonable.

Based on these principles, first, new physical models are integrated into the predictive methodology to correctly capture the correlations among model parameters. These models include V_{th0} dependence on N_{ch}, mobility degradation, and velocity overshoot. Second, based on comprehensive studies of published data over various technology generations, i.e., from 250 nm node to 45 nm node, the scaling trends of key physical parameters are extracted. By integrating these results into PTM, both nominal and variational transistor characteristics are predicted, following the traditional trend of scaling. Smooth and accurate predictions are

obtained from 250 to 12 nm nodes, with L_{eff} down below 10 nm. Compared to various published data, the error in the prediction of I-V characteristics is less than 10%. PTM can be conveniently customized by adjusting only ten primary parameters, in order to cover a wide range of process uncertainties. Using PTM, the impact of process variations is further investigated for nanoscale CMOS design. Overall, this chapter develops a solid predictive base for exploratory circuit design with extremely scaled bulk CMOS. The following chapter (Chap. 3) will further describe how PTM incorporates physical models for new technology advances, such as strained silicon, high-k dielectrics and metal gate, in order to make a far-reaching impact on future design.

2.2 Predictive Methodology

2.2.1 Parameter Taxonomy

Based on our previous work on BPTM, it is recognized that the appropriate categorization of transistor model parameters is crucial for an efficient and physical prediction [3, 5, 6, 7]. Although there are typically more than 100 parameters in a compact transistor model to calculate the I-V and C-V characteristics, only about ten of them are critical to determine the essential behavior of a nanoscale transistor. The performance of a transistor is less sensitive to the rest of secondary parameters. Based on their physical meanings, these first order parameters are listed in Table 2.1 [5–7], including technology specifications as well as process and physical parameters. Such taxonomy keeps the physics of scaling while reducing the complexity of prediction. Furthermore, this categorization is relatively independent on model formats as those key parameters are mostly shared among different transistor models to represent the underlying silicon technology. Accurate modeling and prediction of their values is the key to the development of PTM. In this work, BSIM4 is used as the model basis while the predictive methodology is general enough to be applied to other model formats [8].

In addition to predicting nominal values, it becomes increasingly important to capture process sensitivities as well. As process variations are vastly exacerbated at future technology nodes, current deterministic design paradigm needs to be shifted towards a statistical design flow in order to reduce design uncertainties [1, 4]. Thus, physical correlations among main model parameters, such as the transport behavior [9–11], should be explicitly expressed in compact models for both accurate

Table 2.1 Primary parameters in the development of new PTM

Technology specifications	V_{dd}, V_{th0}, T_{oxe}, L_{eff}, R_{dsw}
Process parameters	N_{ch}, E_{ta0}
Physical parameters	K_1, μ_0, V_{sat}

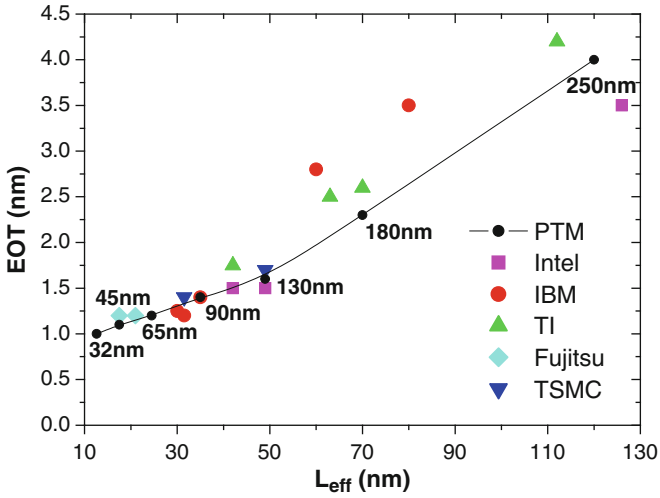

Fig. 2.3 The trend of EOT scaling (Adapted from [8])

technology extrapolation and robust design exploration. While such a consideration is absent in BPTM [3], the new generation of PTM identifies those critical correlations, particularly the interactions among $L_{eff,}$ V_{th}, mobility, and saturation velocity.

2.2.2 Prediction of Model Parameters

As presented in Table 2.1, the first group of parameters is related to the process specifications in technology scaling, including V_{dd}, T_{oxe}, L_{eff}, V_{th0} and R_{dsw}. Their nominal values are determined by literature survey from published industry data, including the ITRS [1]. Based on the collected data, Fig. 2.3 presents the trend of equivalent oxide thickness (EOT). EOT is steadily scaling down, although the pace may slow down in recent years. The trend of V_{dd} and V_{th} scaling is plotted in Fig. 2.4, where the value of V_{th} is extracted from the sub-threshold I-V curves, using the constant current definition. Due to the concern of sub-threshold leakage, V_{th} stays almost the same in the nanoscale. The fifth technology parameter, R_{dsw}, is extracted by fitting the I-V curves in the linear region, after the low-field mobility, μ_0, is predicted (i.e., Eqs. 2.1 and 2.2). The trend of R_{dsw} is shown in Fig. 2.5. The reduction of R_{dsw} becomes more difficult in short-channel devices and results in a constant scaling as the data shows. These trends, which are supported by experimental data, are then integrated into PTM to predict the nominal values during CMOS technology scaling.

Values of technology specifications not only define the basic characteristics of a process; they further determine other important electrical details of a transistor.

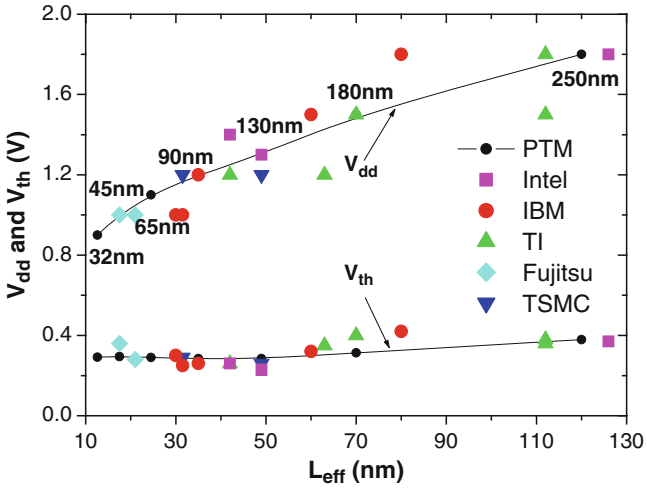

Fig. 2.4 The trends of V_{dd} and V_{th} scaling (Adapted from [8])

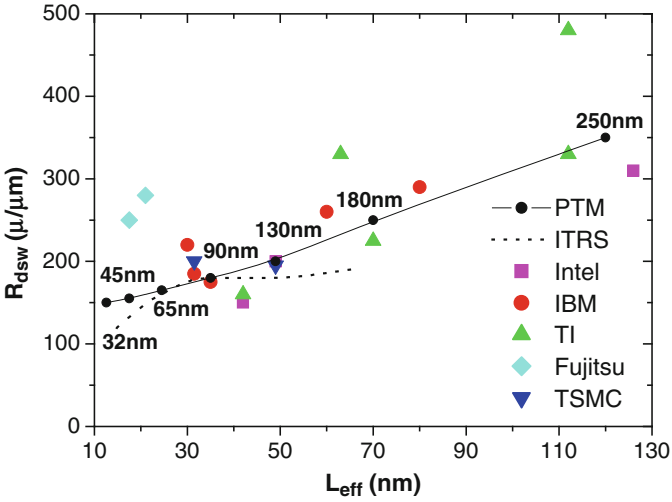

Fig. 2.5 The trend of R_{dsw} scaling (Adapted from [8])

In particular, channel doping concentration, N_{ch}, is mainly defined by the threshold voltage. Exact value of N_{ch} is extracted from published data of V_{th0} in [12–27], using the V_{th} model in BSIM [2]. Figure 2.6 illustrates the trend of N_{ch} scaling. Based on N_{ch}, the main coefficient for the body effect of V_{th}, K_1, is also estimated with analytical models [2]. Furthermore, to model the V_{th} behavior of short-channel transistors, drain-induced-barrier-lowering (DIBL) must be accounted for.

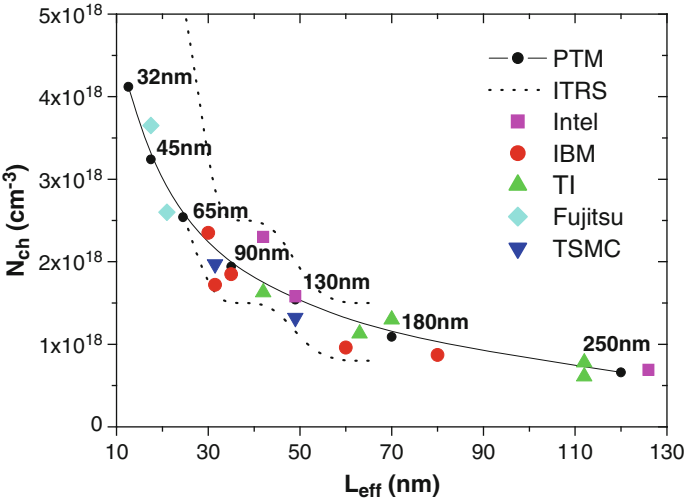

Fig. 2.6 The trend of N_{ch} scaling (Adapted from [8])

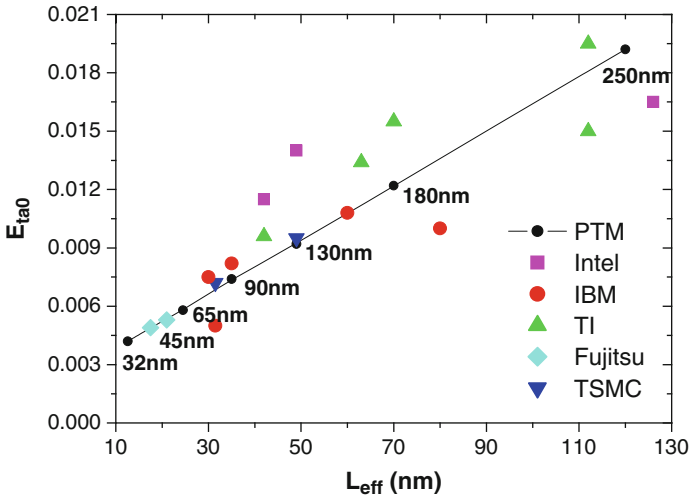

Fig. 2.7 The trend of DIBL coefficient E_{ta0} (Adapted from [8])

To the first-order, this effect is captured by E_{ta0}, which is a model parameter for the DIBL effect. Its value is extracted from published data of V_{th} roll-off [12–27]. A clear trend of E_{ta0} is illustrated in Fig. 2.7.

The amount of channel doping, N_{ch}, is actually important for both threshold voltage and the transport property in a conductive channel, i.e., effective carrier mobility (μ_{eff}) and the saturation velocity (V_{sat}). For example, low field carrier mobility degrades as N_{ch} increases, so does also the effective carrier mobility;

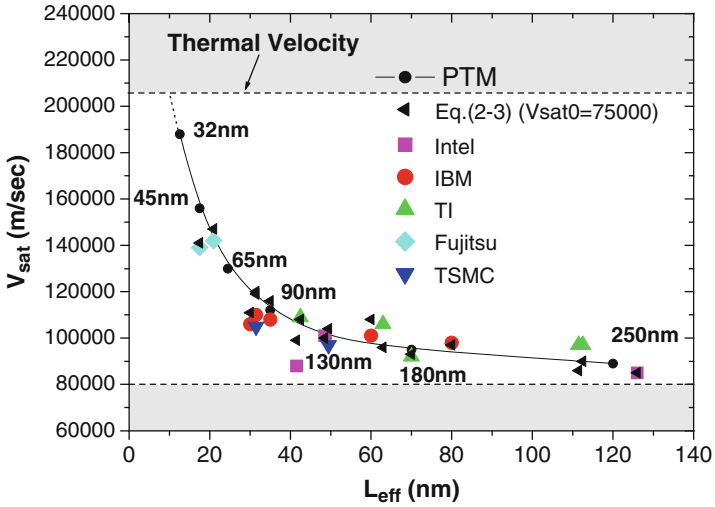

Fig. 2.8 The trend of V_{sat} scaling from traditional velocity saturation to the overshoot region

V_{sat} also depends on N_{ch} and L_{eff} due to the phenomenon of velocity overshoot [9]. To account for these effects, the following formulas are adopted in the new PTM to estimate V_{sat} and μ_0 respectively [8, 9]:

$$\text{NMOS}: \quad \mu_0 = 1150 \cdot \exp\left(-5.34 \cdot 10^{-10}\sqrt{N_{ch}}\right) \tag{2.1}$$

$$\text{PMOS}: \quad \mu_0 = 317 \cdot \exp\left(-1.25 \cdot 10^{-9}\sqrt{N_{ch}}\right) \tag{2.2}$$

$$V_{sat} = V_{sat0} + 0.13\mu_{eff}\sqrt{\tau\mu_{eff}kT/q} \cdot \left(V_d \Big/ L_{eff}^2\right) \tag{2.3}$$

Equations 2.1 and 2.2 are based on the physical model of mobility [9–11]; the coefficient values are extracted from advanced silicon data. Equation 2.3 of velocity overshoot is a simplified solution of the energy-balance equation in [9]. These equations describe the important dependence on N_{ch} and are compatible with the current BSIM framework. The value of V_{sat} is extracted from published I-V data, particularly the saturation current I_{on}; its trend during scaling is plotted in Fig. 2.8. The effect of velocity overshoot is pronounced as technology scales down to sub-100 nm regime. Figure 2.8 also demonstrates excellent model prediction by Eq. 2.3 with the extracted V_{sat}.

Combining these steps together, the ten primary parameters, e.g., V_{dd}, T_{oxe}, L_{eff}, V_{th0}, R_{dsw}, N_{ch}, E_{ta0}, K_1, μ_0 and V_{sat} can be extrapolated towards future technology nodes. Furthermore, their values can be adjusted to cover a range of process uncertainties, e.g., from one company's to another one's, or from intrinsic process

variations. In general, the error by only considering these primary parameters can be reduced to 5%, as demonstrated in [8]. This is further verified by comparing the model predictions with published data, as shown in Sect. 2.3.

The rest of model parameters are secondary ones, without explicit methods to predict their values. To improve the accuracy of predictions, they are further classified into two groups, depending on their importance in the determination of transistor performance. The first group is not as critical as the primary parameters, but still has an observable impact on I-V characteristics. They are related to the determination of short channel effects (e.g., D_{vt0} and D_{vt1} are short channel effects coefficients and their values are extracted from published data of V_{th} roll-off [12–27]), subthreshold behavior (D_{sub}, N_{factor}, V_{off}, C_{dsc}, C_{dscd}), mobility (μ_a, μ_b), and Early voltage. During the scaling of CMOS technology, their values may change from one generation to the next, but are relatively stable within one generation. In this context, their values are fit from experimental data for each technology node and then fixed over a range of process conditions. The remaining secondary parameters have little impact on transistor performance. Thus, for the purpose of early prediction, it is reasonable to leave these parameters unchanged. Finally, the parameters for parasitic C-V characteristics are extrapolated based on BSIM models.

The predictive methodology was first implemented using Verilog-A, since the physical models (i.e., Eqs. 2.1–2.3) are currently not available in the standard model format. After generating the PTM for each technology node, the Verilog-A models can be mapped to standard BSIM4 models for nominal performance prediction, so that designers can directly use them with available circuit simulators. In addition, the Verilog-A format is also compatible with SPICE simulation tools, such that circuit designers can use them directly. Presently, PTM model files for 130 to 12 nm technology generations are available. For easy access, a webpage was established to release the latest models (http://ptm.asu.edu) [8].

2.3 Evaluation of PTM

2.3.1 Verification and Prediction of I-V Characteristics

About twenty sets of published I-V data from the 250 nm node to the 45 nm node at room temperature are collected to verify the prediction by PTM. Using the methodology presented above, we are able to generate corresponding PTM model files. By tuning ten primary parameters, the predicted I-V characteristics are then compared to published data for verification. The parameter tuning steps are explained below. First, V_{dd}, T_{oxe}, L_{eff} and V_{th0} are directly adjusted to the published values. Then N_{ch} is reversely calculated from V_{th0}, using analytical models [2]. Based on N_{ch}, μ_0 and V_{sat} can be calculated with Eqs. 2.1–2.3. Finally, R_{dsw} is extracted from the linear region of I-V curves. Figures 2.9 and 2.10 illustrate two examples at

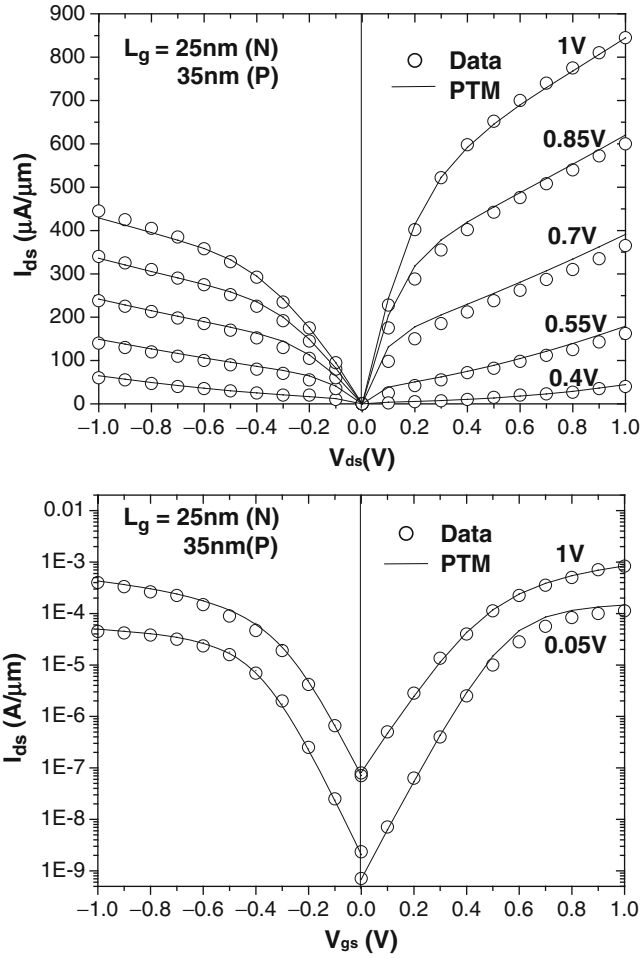

Fig. 2.9 The verification of 45 nm PTM with [13] (Adapted from [8])

45 and 65 nm nodes, respectively. Predicted I-V curves are compared to the measured silicon data from [13] and [14]. Excellent agreement between prediction and published data is achieved in both sub- and super- threshold regions. More comprehensive verifications are listed in Table 2.2 [12–27]. Without any further model optimization, the error of I_{on} predictions is smaller than 10%, for both NMOS and PMOS transistors. Such an excellent matching proves the physicality and scalability of PTM.

Based on the successful verifications, PTM for 130 to 12 nm technology nodes have been generated and released at http://ptm.asu.edu. Figure 2.11 illustrates the trend of nominal I_{on} and I_{off}. Figure 2.12 illustrates the trend of nominal CV/I and switch power (CV_{dd}^2). Table 2.3 further highlights the major characteristics of

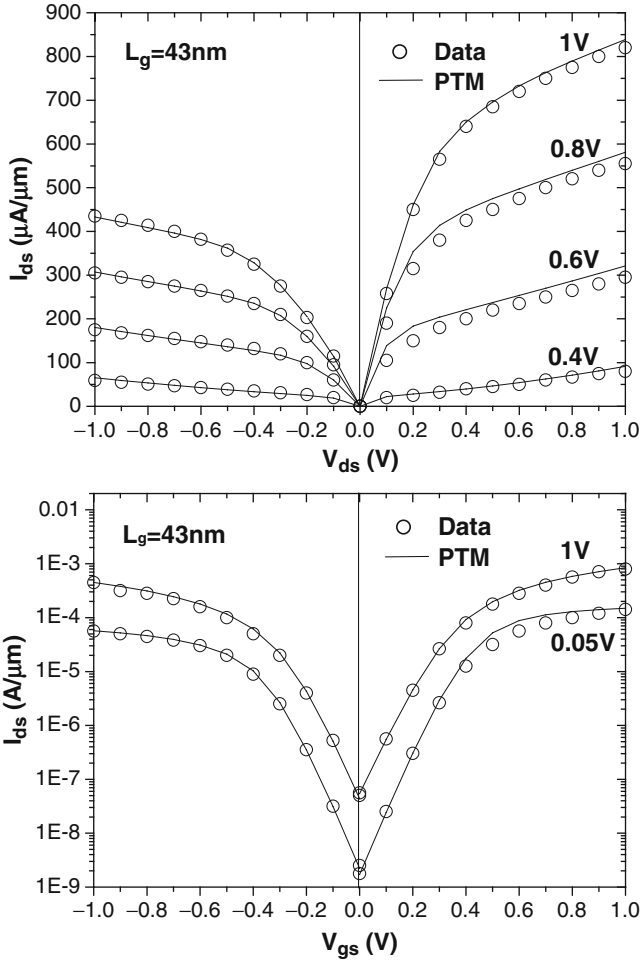

Fig. 2.10 The verification of 65 nm PTM with [14] (Adapted from [8])

PTM predictions for technology scaling. Note that the threshold voltage remains almost unchanged due to the leakage concern (Fig. 2.4). With continuous efforts, PTM will be extended toward the 12 nm technology node and below.

2.3.2 Impact of Process Variations

According to the ITRS, similar or larger amount of process variations are expected at future technology nodes. What matters is not only the amount of variations, but also the sensitivity to variations. In the nanometer regime, the sensitivity of transistor performance on process variations becomes more significant and is

Table 2.2 Evaluation of PTM predictions with published data (adapted from [8])

Data source	V_{dd} (V)	T_{oxe} (nm)	L_{eff} (nm)	V_{th} (V)	R_{dsw} (Ω/μm)	I_{on} (μA/μm)	I_{on} (Pred.)	I_{off} (nA/μm)	I_{off} (Pred.)	Error of I_{on} (%)
[12]	1	1.85	21	0.28	280	940	950	150	120	1
[13]	1	1.85	17	0.36	250	845	855	80	20	1
[14]	1	1.9	30	0.30	220	820	845	50	40	3
[15]	1.2	2.05	32	0.29	200	1090	1187	80	50	9
[16]	1	1.85	32	0.25	185	1005	1045	160	130	4
[17]	1.2	2.05	35	0.26	175	1160	1210	130	100	4
[18]	1.2	2.4	42	0.26	160	1000	995	70	30	−1
[19]	1.4	2.15	42	0.26	150	1120	1205	10	10	8
[20]	1.3	2.15	49	0.23	200	1155	1145	130	140	−1
[21]	1.2	2.35	49	0.26	195	930	970	100	60	4
[22]	1.5	3.6	60	0.32	260	820	855	230	130	4
[23]	1.8	4.3	80	0.42	290	780	775	0.6	0.6	−1
[24]	1.2	3.3	63	0.35	330	586	555	5	4	−5
[25]	1.5	3.4	70	0.40	225	750	755	1	1	1
[26]	1.5	4	112	0.36	330	615	570	1	1	−7
[27]	1.8	4.3	126	0.37	310	690	690	1	1	0
[26]	1.8	5.0	112	0.38	480	605	580	0.6	1	−4

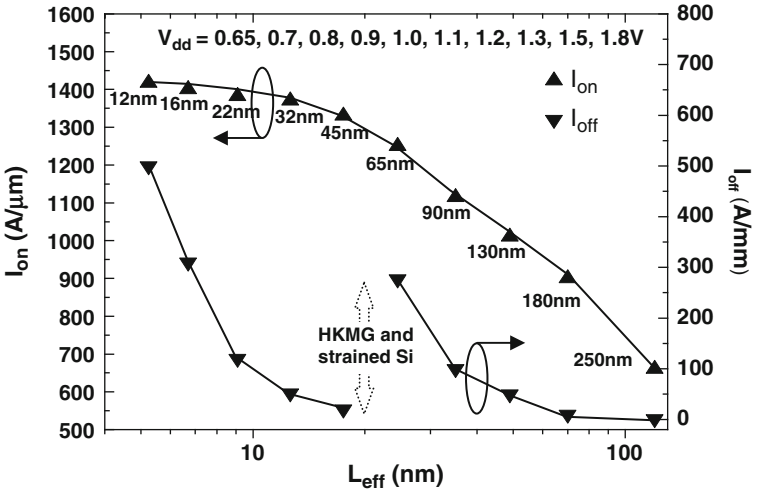

Fig. 2.11 Predictions of the scaling of nominal I_{on} and I_{off}. The jump in I_{off} is due to the adoption of high-k/metal gate and stained Si technology, as described in Chap. 3

critical for robust CMOS design. One particular phenomenon is velocity overshoot (Eq. 2.3). Figure 2.8 illustrates the trend of V_{sat} for successive technology nodes. When L_{eff} is larger than 100 nm, V_{sat} can be treated as a constant value, e.g., about 80,000 m/s. However, as L_{eff} scales below 100 nm, V_{sat} can no longer be

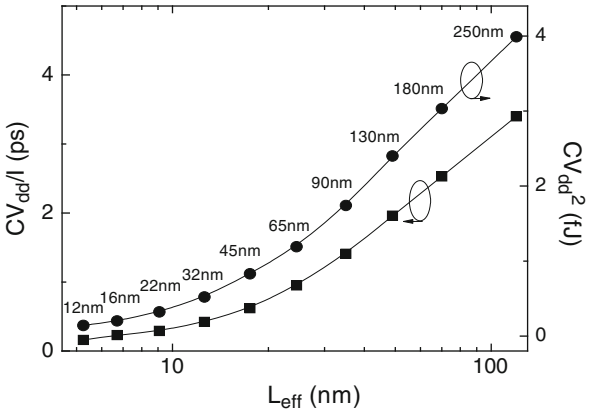

Fig. 2.12 The prediction of nominal CV/I and CV_{dd}^2

Table 2.3 The summary of PTM predictions for NMOS devices.

Tech.node (nm)	V_{dd} (V)	T_{oxe} (nm)	L_{eff} (nm)	V_{th} (V)	R_{dsw} (Ω/μm)	I_{on} (μA/μm)	I_{off} (nA/μm)	CV/I (ps)
12	0.65	0.6	5.25	0.265	135	1417	500	0.16
16	0.7	0.7	6.7	0.285	140	1400	310	0.23
22	0.8	0.8	9.1	0.31	145	1382	120	0.29
32	0.9	0.9	12.6	0.292	150	1370	52	0.42
45	1.0	1.0	17.5	0.295	155	1330	20	0.62
65	1.1	1.2	24.5	0.290	165	1250	277	0.95
90	1.2	1.4	35	0.284	180	1105	100	1.31
130	1.3	1.6	49	0.284	200	1000	50	1.96
180	1.5	2.3	70	0.309	280	890	10	2.53
250	1.8	4.0	120	0 379	350	610	1	3.34

approximated as a constant. Even though mobility (μ_{eff}) decreases with technology scaling due to higher N_{ch}, V_{sat} increases because of the inversely quadratic dependence on L_{eff} (Eq. 2.1) due to velocity overshoot. As a consequence, I_{on}, which is somewhat proportional to V_{sat}, is more sensitive to variations of L_{eff}, mobility, and V_{dd} in the nanoscale (Eq. 2.3). When the channel length is further reduced, the importance of velocity overshoot may degrade due to the ballistic transportation and the source-injection limit [2].

The importance of velocity overshoot in the study of process variations is further illustrated in Fig. 2.13. Figure 2.13 decomposes the variation of I_{on} into various physical mechanisms at the 45 nm node, for the variation of L_{eff}. Without considering DIBL and velocity overshoot, I_{on} is relative insensitive to L_{eff} variations as a result of pronounced velocity saturation in a nanoscale transistor. However, V_{th} of a nanoscale transistor changes when there exists the variation of L_{eff}, i.e., DIBL. For example, -20% L_{eff} variation will result in approximate 18% higher I_{on} due to DIBL. An additional amount of 27% I_{on} variation can be observed if velocity

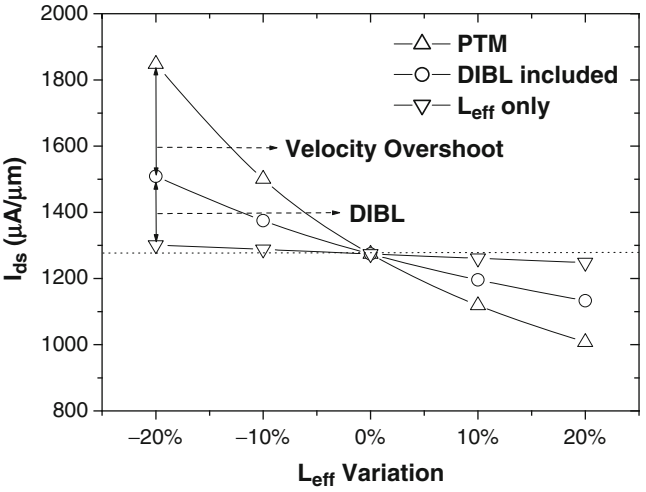

Fig. 2.13 The impact of L_{eff} variation at 45 nm (Adapted from [8])

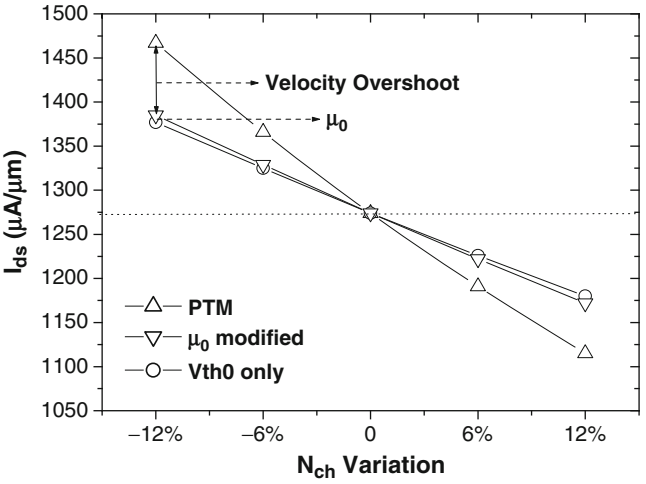

Fig. 2.14 The impact of N_{ch} variation at 45 nm (Adapted from [8])

overshoot is included (Fig. 2.13). Therefore, it is critical to include these physical models in prediction, in order to provide correct guidance to robust design explorations.

Besides L_{eff} variation, the random fluctuation of channel doping concentration is another leading source of process variations. When N_{ch} deviates from the target value, not only V_{th0}, but also K_1 (the body effect), μ_0 (mobility) and V_{sat} will change accordingly. Figure 2.14 shows the impact of N_{ch} variation on I_{on}. Similar to

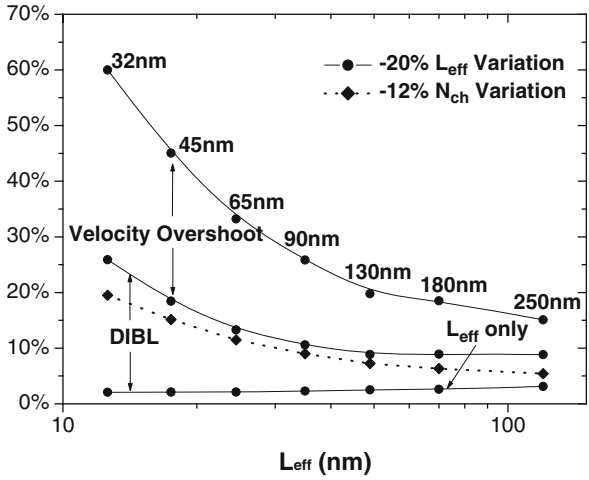

Fig. 2.15 The impact of L_{eff} variation on I_{on} during CMOS technology scaling (Adapted from [8])

Fig. 2.13, the sensitivity of I_{on} on N_{ch} variation increases when additional physical mechanisms are included. Considering the dependence of μ_0 and V_{sat} on N_{ch}, -12% N_{ch} variation leads to 15% increase in I_{on} at 45 nm node. These physical correlations were not considered in previous BPTM, which could cause significant underestimation of performance variability.

The overall map of process sensitivities is shown in Fig. 2.15 across technology generations from 130 to 32 nm. Due to increasing process sensitivities, the variation of I_{on} becomes larger during technology scaling, even if the normalized process variation remains constant, e.g., -20% and -12% for L_{eff} and N_{ch} variation, respectively (Fig. 2.15). For future technology generations, L_{eff} will continue to be the dominant factor affecting performance variation, because of its role in velocity and the DIBL effect. Second to L_{eff} variation, the impact of N_{ch} variation also keeps increasing as technology scales. Figure 2.15 shows the decomposition of the impact of L_{eff} variations during technology scaling. It reveals that velocity overshoot plays a more important role than DIBL for nanoscale MOSFET. Therefore, physical modeling of velocity overshoot is necessary in variation-aware design. Since PTM can be easily customized by tuning L_{eff}, T_{oxe}, R_{dsw}, V_{th0}, E_{ta0}, V_{dd}, and the other primary parameters, robust circuit design research under different conditions are fully supported.

In summary, a new generation of PTM was developed for 130 to 12 nm bulk CMOS technology [8]. As compared to previous BPTM, the new predictive methodology has better physicality and scalability over a wide range of process and design conditions. Both nominal values and process sensitivity are captured in the new PTM for robust design research. Excellent predictions have been verified with published transistor data. The importance of physical correlations among parameters and the impact of process variations have been evaluated. Model files

for bulk CMOS down to the 12 nm node are available at http://ptm.asu.edu. These predictive model files enable early stage circuit design for end-of-the-roadmap technologies. Feedbacks from both industrial and academic researchers will be very helpful to improve the accuracy and flexibility of PTM.

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