# Preface

The story of PTM, standing for Predictive Technology Model, is dated back to the year of 1999, when IC designers were hectically migrating from 0.25 μm to 0.18 μm CMOS technology. At that moment, many new problems were emerging from the physical level, such as short-channel effects and crosstalk noise, posing significant challenges that slowed down the product development. PTM was proposed to help bridge the technology and design groups, such that these issues can be brought to the attention as early as possible in the design process. Enabled by PTM, the new concept of concurrent process-design development is then widely practiced by university and industry groups. PTM effectively enhances design productivity and catalyzes the silicon evolution into the nanoscale regime.

Ten years after the start, PTM has successfully developed state-of-the-art CMOS models toward the 10 nm node. They are well disseminated through the web interface, and adopted into university curriculums. The demand of predictive modeling becomes even stronger today, as we are facing much more complicated and more diverse technological choices, as well as much larger scale of integration. This book covers both the essence of modeling principles and the application of PTM in nanoelectronic design. The chapters are intended primarily for IC designers and EDA tool developers, who have the background in transistor physics and circuit performance analysis. The discussion will especially benefit those with research interests in the areas of technology scaling and compact modeling.

The book starts with the background and overview of PTM. Chapter 1 reviews the important issues as CMOS technology is scaling toward the 10 nm node. It motivates the shift of IC design paradigm, in which PTM is the essential component. Current PTM provides standard compact model of bulk CMOS devices, BSIM4, down to the 12 nm node. Chapter 2 presents the systematic approach to scale device model parameters for future bulk devices, based on the solid understanding of device physics and silicon data as a reality check. Furthermore, Chap. 3 deals with recent extensions of conventional CMOS devices, including strained Si, high-k/metal gate, and the double-gate structure. Below the 90 nm node, these non-traditional materials and structures are vitally important to enhance the device

performance. Modeling solutions to them are compatible with standard CMOS model and circuit simulation tools.

With CMOS scaling approaches fundamental physics and manufacturing limits, process variability and reliability degradation becomes the key limiting factors for future integrated system design. Chapters 4 and 5 address these concerns by developing statistical modeling, extraction and simulation techniques. New compact models are proposed for emerging variability and reliability effects, such as NBTI, in order to support design exploration for reliability. Besides these parasitic effects of transistor scaling, interconnect parasitics play an increasingly significant role in contemporary IC design. Chapter 6 presents modeling results of wire capacitance, capturing the latest advancement in interconnect technology.

These device models provide the basis of design benchmarking and tool development. Using PTM, Chap. 7 quantitatively evaluates various technology factors in scaled CMOS design, helping shed light on the performance trend along the roadmap. Moreover, Chap. 8 describes a 45 nm predictive process design kits (PDK), which are the critical interface between circuit design and silicon fabrication. Under the increasing stress of the manufacturability, such a PDK facilitates designers assess layout dependent effects and manage their impact.

Beyond the 10 nm node, more radical solutions will be vital to meet the scaling criteria. While there have been significant accomplishments in scientific discovery, it is only the beginning of the engineering research that is required to transfer the science into device, circuit, and system integration. In Chap. 9, PTM outreaches the effort to the compact modeling of carbon nanotube devices, helping illustrate their enormous design potentials. Finally, Chap. 10 concludes the book with a brief outlook on future nanoelectronic modeling and design.

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http://www.springer.com/978-1-4614-0444-6

Predictive Technology Model for Robust Nanoelectronic Design

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2011, XV, 173 p., Hardcover
ISBN: 978-1-4614-0444-6