

The SAM images of the chip-to-substrate interface show no indications of any fatigue in the chip solder interfaces, but it presents black areas in the regions, where solder delaminations are found in the substrate-to-base plate solder layer. This artifact is produced by a lack of acoustic energy in these regions, because most of the signal was already reflected in the delaminations found in the substrate-to-base plate solder layer. Since the SAM signal is injected from the base plate surface, reflections nearer to the base plate reduce the signal propagating into deeper layers. However, this common artifact allows conveniently evaluating how close the delamination has come to the chip position. As clearly shown in Fig. 11.37 the delaminations have propagated much deeper under the chip areas for the SnPb solder system as for the SnAg solder system with a stronger unfavorable impact on the thermal resistance of the chips.

The lifetime under temperature cycles is determined by the combinations of different materials (with different coefficients of thermal expansion) and the stability of the interconnect layers. Due to the mechanical deformation, smaller packages as the TO family are more stable than larger modules that are more complex. Since the source for the passive temperature cycles is located outside of the module, only the used materials and interconnection layer decide about the reliability of a package.

11.6.7 Power Cycling Test

In contrast to the temperature cycling test, the power chips are actively heated by the losses generated in the power devices themselves in a power cycling test. This accounts for a fundamental difference between the two tests: In a power cycling test, the amount of losses can be affected by the chip technology and by the silicon area implemented in the module. Therefore, any power cycling lifetime requirement can be met just by implementing sufficient silicon area to reduce the temperature swing generated by the chip losses. However, commercial aspects limit this option in practical applications.

During power cycling test, the device under test is mounted on a heat sink as in a real application. A load current is conducted by the power chips and the power losses are heating up the chip. When the maximum target temperature in the chip is reached, the load current is switched off and the system cools down to a minimum temperature. The reaching of the minimum temperature completes the cycle and the next cycle begins by starting the load current again. During each cycle, considerable temperature gradients are generated inside the module. An exemplary temperature evolution is shown in Fig. 11.38.

The control is executed using the heat sink temperature. When the upper limit of T_h is reached, the load current is turned off and the cooling is turned on. The temperature decreases. When the lower limit of T_h , identical to the lower limit of the junction temperature T_{low} , is reached, the load current is turned on again and the cycle is repeated. The characteristic parameter for power cycling tests, the temperature swing ΔT_j , is given by the temperature difference between maximal junction temperature T_{high} at the end of the heating phase and the minimal junction temperature at the end of the cooling interval:

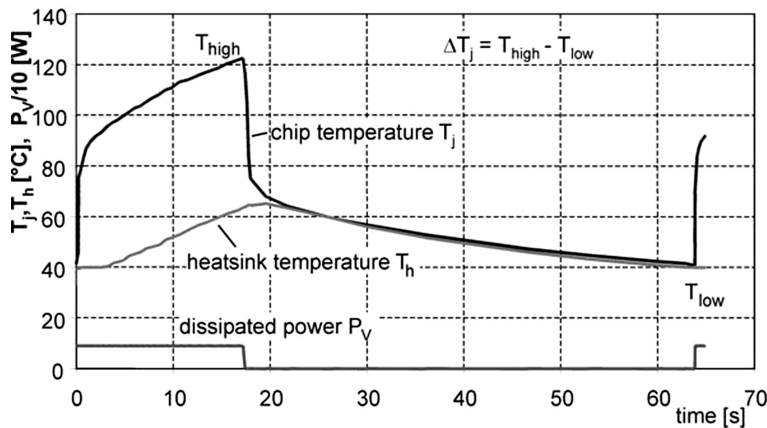


Fig. 11.38 Temperature profile of a power cycling pulse resulting from a constant load current

$$\Delta T_j = T_{\text{high}} - T_{\text{low}} \quad (11.15)$$

In Fig. 11.38 ΔT_j can be read as 82°C.

A further important parameter for the power cycling test is the medium temperature T_m :

$$T_m = T_{\text{low}} + \frac{T_{\text{high}} - T_{\text{low}}}{2} \quad (11.16)$$

Instead of T_m also T_{high} or T_{low} can be used as a characteristic parameter, because they are related by ΔT_j . Further parameters, e.g., the duration of the cycle, are of importance as is shown below. A long power cycle time (64 s in Fig. 11.38) usually represents a higher stress for the devices.

The different coefficients of thermal expansion of materials during the temperature swing create mechanical stress at the interfaces. This thermal stress leads in the long run to fatigue of materials and interconnections. Figure 11.39 shows the result of a power cycling test with a standard module. During the test, the forward voltage V_C of an IGBT is monitored. Additionally, it is possible to feed a defined sense current of some milliamperes through the device after the turn-off of the load current, which allows to determine the upper temperature T_{high} with the use of a calibration function (compare Fig. 11.19). The power losses P_v are also measured online. From junction temperature T_{high} , heat sink temperature T_h , and P_v the thermal resistance is calculated using Eq. (11.4). Since the measurement of the fast changing heat sink temperature is difficult due to the response time of the applied sensor, the thus measured thermal resistance can deviate from the true stationery value, especially for short cycles below 10 s. However, even then this relative value can be used to monitor relative changes in R_{thjh} .

In Fig. 11.39 one can recognize that the on-state voltage drop at the IGBT remains almost constant up to a large number of cycles, and the thermal resistance increases slowly after approximately 6000 cycles. This is an indication for

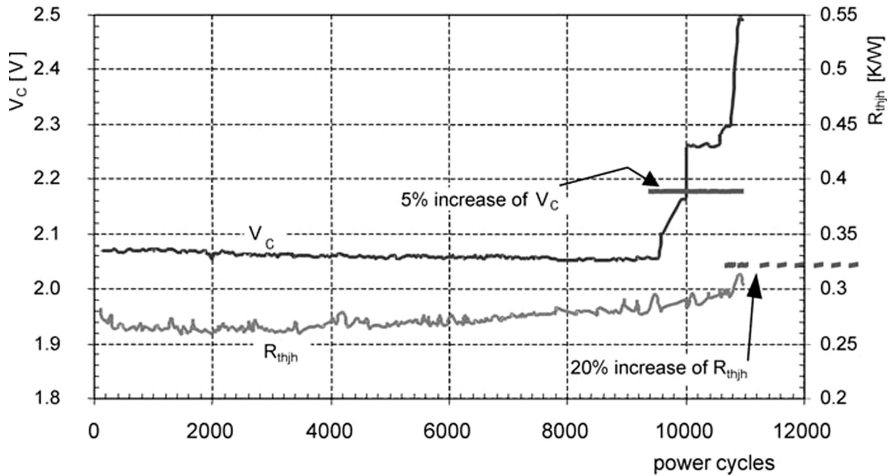


Fig. 11.39 Behavior of on-state voltage drop V_C and thermal resistance R_{thjh} at a power cycling test with $\Delta T_j = 123$ K

an increase of thermal resistance in the thermal path, mostly attributed to solder fatigue. After more than 9000 cycles one finds a first step in the V_C characteristic, which is due to lift-off of bond wires. Shortly after that, the next step is observed and finally all bond wires are lifted off, the power circuit is open and the test can no longer be continued.

Bond wire lift-off and solder fatigue are the main failure mechanisms in standard power modules. But from the shape shown in Fig. 11.39 it is difficult to determine the primary failure mechanism. The failure limit of R_{thjh} would be reached at after approximately 11,000 cycles. But increase of R_{thjh} results in increasing temperature T_{high} and this will escalate the thermal stress for the bond wires. Therefore, solder fatigue is a significant failure mechanism in this test; it could be even the main failure mechanism. On the other hand, bond wire lift-off leads to increased V_C , which together with the constant current causes increasing losses and raises the upper junction temperature T_{high} , resulting in more thermal stress in solder layers. Due to the interdependency of the failure modes, power cycling tests require a careful failure analysis.

Failure limits are defined as:

- an increase of V_C by 5% or by 20%, varying for different suppliers, depending on the measurement accuracy for V_C . Different failure limits, however, have only a negligible impact on the lifetime. Usually, after the first significant increase of V_C the bond wires will soon fail completely, as can also be seen in Fig. 11.39
- an increase of R_{th} by 20%
- failure of one of the functions of the device, e.g., failure of blocking capability or of the gate to emitter (gate to source) insulation capability for IGBTs and MOSFETs

11.6.7.1 Weibull Statistics for Power Cycling Analysis

An estimation of the lifetime of a power device as a series product is possible by evaluating the power cycling results using a Weibull statistics. The Weibull statistics is specially suited for the description of end-of-life phenomena. It is applicable for failure mechanisms determined by aging mechanisms of materials. An example is shown in Fig. 11.40. The test was executed until five of six devices under test failed. The numbers of cycles to failure are marked. The Weibull distribution is described by the probability density $f(x, \alpha, \beta)$ and the accumulated probability $F(x, \alpha, \beta)$ as follows:

$$F(x, \alpha, \beta) = 1 - \exp\left(-\left(\frac{x}{\beta}\right)^\alpha\right) \quad (11.17)$$

The accumulated probability corresponds to the rate of parts, which have already failed. For a power cycling test analysis, x is the number of cycles to failure. The scale parameter β defines the range of the distribution; for $x = \beta$ the rate $1/e$ of the parts have survived. For $F = 1$, all parts have failed. The shape parameter α characterizes the spread of the distribution. The higher the α , the more concentrated are the numbers of cycles to failure of the different parts around the median of the distribution. The derivative $dF/dx = f$ corresponds to the probability density; it determines the probability that the failure occurs in an interval $x + dx$:

$$f(x, \alpha, \beta) = \frac{\alpha}{\beta^\alpha} x^{\alpha-1} \exp\left(-\left(\frac{x}{\beta}\right)^\alpha\right) \quad (11.18)$$

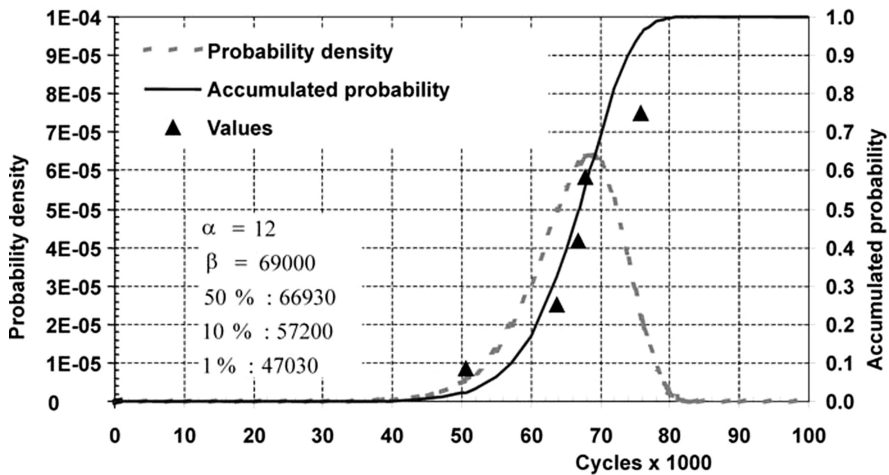


Fig. 11.40 Weibull analysis of a set of power cycling tests on a series product

Even though Weibull statistic on power cycling test results are based on a comparatively low number of devices, this statistical analysis allows to predict the survival rate under defined application conditions for a series product. The restriction of a limited number of failures is caused by the fact that these tests are very time consuming and that it is not easy to perform the test simultaneously on groups of devices since the test conditions will change when some of the devices fail during the test. Therefore, the first failure of a set of devices under test is often used to define N_f .

11.6.7.2 Models for Lifetime Prediction

Since a standard technology is established for the construction of power modules with base plate and technologies and materials are very similar even for different suppliers, a research program for determination of lifetime for standard power modules was implemented in the early 1990s. In this project named LESIT, modules from different suppliers from Europe and Japan have been tested; a common feature was the standard package according to Fig. 11.13 with the use of an Al_2O_3 ceramics according to Table 9.1, left row. Tests were executed at different ΔT_j and different medium temperatures T_m ; the results have been summarized in [Hel97] and are shown in Fig. 11.41 in the form of characteristics of cycles to failure N_f depending on ΔT_j and for different medium temperatures T_m .

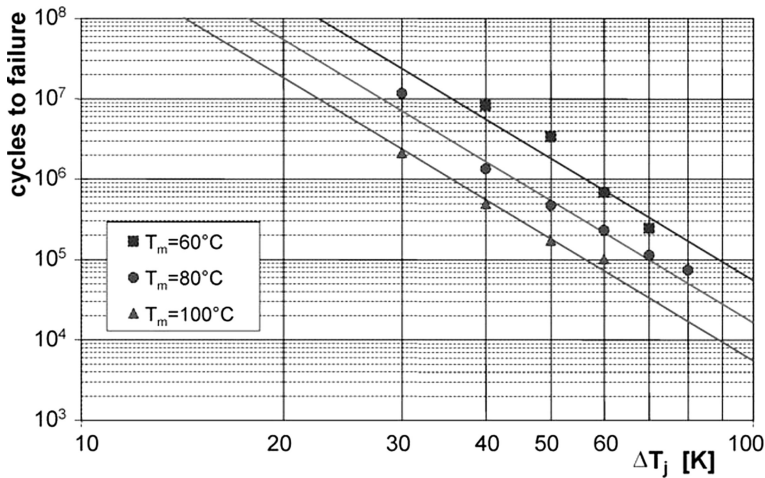


Fig. 11.41 LESIT results

The lines in Fig. 11.41 represent a fit from [Scn02b] to the experimental data: The expected number of cycles to failure N_f at a given temperature swing ΔT_j

and an average temperature T_m , the absolute medium temperature in K, can be approximated with the equation

$$N_f = A \cdot \Delta T_j^\alpha \cdot \exp\left(\frac{E_a}{k_B \cdot T_m}\right) \quad (11.19)$$

with k_B (Boltzmann constant) = 1.380×10^{-23} J/K, activation energy $E_a = 9.89 \times 10^{-20}$ J, and the parameters $A = 302,500 \text{ K}^{-\alpha}$ and $\alpha = -5.039$.

Equation (11.19) consists of a Coffin–Manson law, i.e. the number of cycles to failure (N_f) is assumed to be proportional to $\Delta T_j^{-\alpha}$ [Hel97]. It appears as a straight line when plotting $\log(N_f)$ over $\log(\Delta T_j)$. In addition, an Arrhenius factor containing an exponential dependency on an activation energy is added to the Coffin–Manson law [Hel97]. From models for solder fatigue the impact of dwell time, ramp time, or cycle time are also known as factors influencing the lifetime. However, in the past such models have been suggested rather for passive thermal cycling tests and not for power cycling tests.

Using Eq. (11.19) it is possible to calculate the number of cycles to failure for given ΔT_j and T_m according to the LESIT results. If the typical cycles in the application are known, it is possible to calculate the expectation for the lifetime of a module under these conditions.

Technologies for standard modules have been improved since 1997. Power cycling results for more recent power modules of two different suppliers are shown in Fig. 11.42. They are compared with Eq. (11.19) for the condition $T_{low} = 40^\circ\text{C}$,

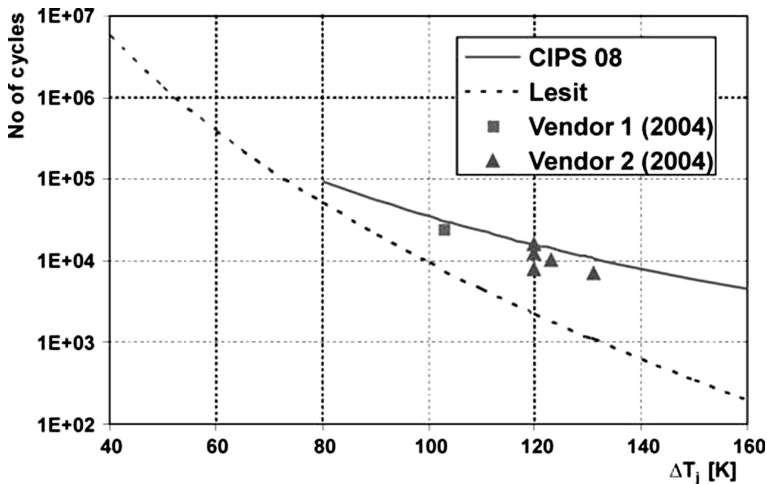


Fig. 11.42 Comparison of experimental power cycling results of state-of-the-art 2004 modules with predictions by the extrapolated LESIT model (11.19) and new CIPS 08 model (11.20); $T_{low} = 40^\circ\text{C}$

extrapolated to higher temperature swings outside of the data in Fig. 11.41. It is visible that the number of cycles to failure is increased by a factor of 3 to 5 in the range of $\Delta T_j > 100$ K compared to the prediction using Eq. (11.19).

A fundamental problem in performing power cycling tests is the difficulty in the selection of test conditions. The target ΔT_j is a function of the dissipated energy – which for a given chip technology is determined by the forward current and the t_{on} duration in the test – and of the thermal resistance of the test setup. It is therefore very difficult to repeat a test with exactly the same test conditions, but it is even more difficult to select test parameters for different ΔT_j values with the same current and heating times. If these parameters have an impact on the test results, they have to be taken into account by a lifetime model.

This was the motivation to present an extended model for the lifetime of standard power modules [Bay08]. Based on a large number of power cycling results of modules, the following equation was derived:

$$N_f = K \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{low}}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \quad (11.20)$$

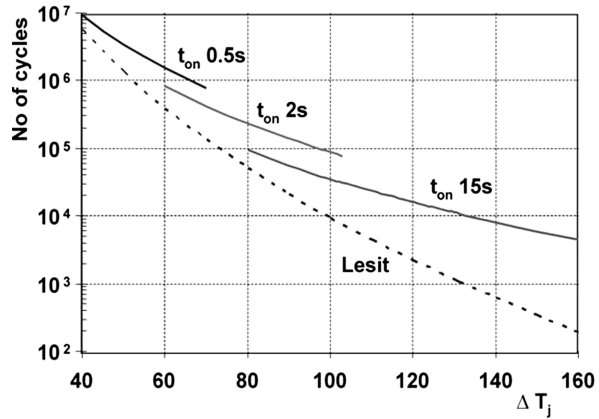
As parameter K we use the value 9.30×10^{14} , the other parameters $\beta_2 - \beta_6$ are given in Table 11.8 [Bay08]. Equation (11.20), which we denote as CIPS 08 model, contains additionally the dependence on the heat-up time t_{on} in seconds, the current per bond stitch on the chip I in A, the voltage range of the device V in V/100 (reflecting the impact of the semiconductor die thickness), and the bond wire diameter D in micrometers. The prediction by the new CIPS 08 model is also shown in Fig. 11.42 for $t_{on} = 15$ s. The CIPS 08 model holds for standard modules with Al_2O_3 substrates; it is not valid for high-power traction modules which are built with the materials AlN and AlSiC, see Table 11.1.

Equation (11.20) was a result of purely statistical analysis and is not a result of physics-based models [Bay08]. The dependency on the cycling time t_{on} in Eq. (11.20) – higher number of cycles to failure for short cycling times – may be explained by the fact that in a short cycle time mainly the semiconductor itself is heated up. Thermal-mechanical stress occurs mainly at the interface between semiconductor and bond wire, while in layers closer to the heat sink the temperature increase is marginal and less thermal stress is applied. The dependency on current per bond stitch on the chip I can be attributed to improved current distribution on the chip with more bond stitches and presumably to a positive impact of the thermal capacity of the bond stitches. The dependency on the bond wire diameter D is

Table 11.8 Parameters for calculation of power cycling capability according to Eq. (11.20)

β_1	–4.416
β_2	1285
β_3	–0.463
β_4	–0.716
β_5	–0.761
β_6	–0.5

Fig. 11.43 CIPS 08 model according to Eq. (11.20) for different heating times t_{on} , compared to the LESIT model; $T_{low} = 40^\circ\text{C}$



related to the greater mechanical stress applied to the bond stitch by thicker bond wires. The dependency on the voltage range V is in fact a dependency on device thickness, which increases from 600 to 1700 V. With thinner devices, the mechanical stress implied on the solder interface by the Si-material will be reduced. Note that the used devices are produced in a thin-wafer technology for 1200 V ($V = 12$) and 600 V ($V = 6$). For devices fabricated from epitaxial wafers, e.g., PT-IGBTs or Epi-diodes, Eq. (11.20) is not applicable.

As a consequence of the statistical approach of the CIPS 08 model, the parameters are not physically independent, which was pointed out and discussed by the authors themselves [Bay08]. For low ΔT_j , for example, a short heating time will be typical. The influence of different heating times t_{on} is shown in Fig. 11.43. Figure 11.42 gives the impression that for a $\Delta T_j < 60$ K the new model predicts less cycles to failure N_f than the former LESIT model. But the dependency on the heating time shows that the lifetime N_f is higher for state-of-the-art 2008 modules, if a short heating time t_{on} for low ΔT_j is assumed.

Despite the fact that data for Eq. (11.20) were only generated with modules of one manufacturer, the equation seems also useful for lifetime calculation of modules of other manufacturers. If lifetime calculations are of vital importance in an application with high reliability requirements, the manufacturing company should always be consulted.

11.6.7.3 Superimposition of Power Cycles

Additionally to the already discussed restrictions, lifetime models are derived from the repetition of identical power cycles, but in real applications various different cycles are superimposed.

To calculate the lifetime under realistic application conformal conditions with superimposed power cycles, a linear accumulation of damage is often assumed as discussed, for example, in [Cia08]

$$Q(\Delta T) = \frac{N(\Delta T)}{N_f(\Delta T)} \quad (11.21)$$

If the number of cycles N reaches N_f – the number of cycles to failure calculated by a lifetime model – Q is equal to 1. For superimposition of n conditions Q_n , the failure is expected when the sum of $Q_n = 1$. Since this so-called Miner's rule [Min45] is independent of the considered lifetime model, the simple Eq. (11.21) which is only a function of ΔT_j can be extended using the model in Eq. (11.20):

$$Q(\Delta T_j, T_{\text{low}}, t_{\text{on}}, I, V, D) = \frac{N(\Delta T_j, T_{\text{low}}, t_{\text{on}}, I, V, D)}{N_f(\Delta T_j, T_{\text{low}}, t_{\text{on}}, I, V, D)} \quad (11.19)$$

An investigation with two superimposed power cycles is reported in [Fer08]. A cycle with high ΔT_j of 140°C is superimposed with short cycles with low ΔT_j . However, the cycle with high ΔT_j was dominant for the failure under the chosen superposition. It is generally difficult to define two superimposed power pulses in such a way that each of them contributes with exactly 50% to the final failure.

A different approach was reported in [Scn02b], where first conventional power cycling tests with uniform cycles were performed at two different temperature swings and then a test with both cycling conditions interleaved was conducted. The test results showed that in contradiction to the assumption of linear fatigue accumulation, the number of cycles to failure was equal to the sum of cycles for each single test condition. The explanation for this phenomenon was that the test conditions are initiating different failure mechanisms, which do not interact with each other.

Before we discuss the failure mechanisms in power cycling test known today in more detail, a deficiency common to all of the above-presented lifetime models must be added. The models (11.19) and (11.20) are based on a purely statistical analysis of data under different conditions. No physical relationship is attributed to the impact of different test parameters. Currently, many research groups are working on physics-of-failure lifetime models, which promise to result in better lifetime prediction models and give more insight into the physical mechanisms that limit the lifetime of power modules for active power cycles.

A final remark addresses the problem of cycle counting in application conformal temperature evolutions known as mission profiles. A simple collection of maximum–minimum temperature swings is very sensitive to the resolution of the analysis. A more robust approach, which is also consistent with the strain–stress characteristic in physics-of-failure-oriented models, is the widely accepted rainflow counting method [Dow82]. It is less sensitive to resolution changes and evaluates the fundamental frequencies with a higher weight.

11.6.7.4 Bond Wire Lift-Off

A typical fault image after power cycling of a standard module with base plate is shown in Fig. 11.44. All bond wires are lifted off from the IGBT chip. The bond wire in the background was the last one to fail and the current was flowing in a short time via an arc flash-over which caused a crater below the bond wire stitch. The bond wire failure in the foreground shows a characteristic feature of the lift-off failure mode. The dissection did not occur at the interface between bond wire and chip metallization, but it emerges partially in the volume of the bond wire. Residues of bond wire material can still be detected on the surface of the chip metallization.

Fig. 11.44 Lifted bond wires after power cycling test with $\Delta T_j = 100$ K of a standard IGBT module. The total failure occurred between 10,791 and 13,000 cycles



Fig. 11.45 Lift-off pattern as a result of power cycling



Figure 11.45 shows a magnified image of the lift-off area on the chip metallization. This example shows no adherence in the center of bond area. Improvements of the wire bond process can enhance the quality of the adherence significantly. In [Amr06] it was shown that an improved wire bond process in combination with a replacement of the chip solder by a silver sinter technology can achieve a very high-power cycling capability for power cycles up to $T_{\text{high}} = 200^{\circ}\text{C}$. In the viewpoint of high-temperature applications, bond wires seem not to be the main limiting factor.

It was found that bond wires have a higher lifetime if they are coated with a polyimide cover layer [Cia01]. Additionally, optimization of the wire bond geometry and the wire bond material can increase the lifetime of bond wires during active power cycles.

Special attention has to be paid to gate wire bonds on chips with a center gate contact. For power devices with a field effect gate structure, the leakage current of the gate is so small that it takes days to discharge the gate via the leakage current. Therefore, a wire bond lift-off of the gate wire bond will not be noticed if the gate is continuously switched on and the load current is controlled by an external switch. In this case, a special functional test must be performed during the cooling phase of each cycle to verify the gate functionality. This can be done by switching of the gate voltage during the cooling phase. The constant current source, that supplies the sense current during this phase, must then go into voltage limitation mode. This technique ensures that a gate bond wire lift-off will not remain undetected.

11.6.7.5 Reconstruction of Metallization

A phenomenon observed during active power cycles with a high temperature swing is the reconstruction of the chip metallization. This contact metallization is conventionally made of a vacuum-metallized aluminum layer, which is formed in a grain structure. Due to the difference in thermal expansion between silicon and aluminum, this layer suffers from a considerable stress during repeated temperature swings. While the silicon chip is only marginally expanding with increased temperature (2–4 ppm/K), the grains of the Al metallization expand considerably (23.5 ppm/K). Thus, the metallization layer is subjected to a compressive stress during the heating phase of temperature cycles.

The surface reconstruction of aluminum films on silicon was first reported in the late 1960s [Pad68] followed by detailed investigations of this degradation effect. Comparison between temperature-cycled samples with annealed (uncycled) samples for equivalent time-at-temperature revealed that the surface reconstruction is increased by thermal cycling by a factor 2 to 5 depending on temperature and grain size of the aluminum film [San69]. Analysis of reconstruction phenomena at high temperatures (above 175°C) and low temperatures (below 175°C) suggests different fatigue mechanisms for these temperature ranges. Diffusional creep and plastic deformation involving conservative motion of dislocations are assumed as dominant contributions for high temperatures, while for low temperatures the only possible mechanism of mass transport is plastic deformation caused by compressional fatigue [Phi71].

While the former investigations were triggered by surface reconstruction observed in integrated circuits, the same effect was found in power electronic devices [Cia96]. The periodical compressive stress during the heating phase in temperature cycles results in plastic deformation of grains when the elastic limits are exceeded. According to [Cia01] this is the case for junction temperature above 110°C. The plastic deformation can lead to the extrusion of single grains. This process leads to an increasing surface roughness of the metallization with the macroscopic observable effect of a dull non-reflective surface appearance. In the cooling phase of the temperature cycle, tensile stress can lead to cavitation effects at the grain boundaries if the elastic regime is exceeded. This can explain the observed increase in electrical resistance of the surface metallization [Lut08].

Reconstruction of the aluminum contact layer was also found in failed devices after repetitive short-circuit operation of IGBTs [Ara08]. Recently, a similar effect of increasing surface roughness was observed also in thick aluminum layers of “direct bonded aluminum” (DBA) substrates after temperature cycling between –55 and 250°C. After 300 cycles the surface roughness of 300 μm thick aluminum layers on AlN substrates increased by more than a factor of 10, while a multitude of voids were observed in a cross section. The authors attribute this effect to grain boundary sliding [Lei09].

Figure 11.46 shows the optical image of such a metallization reconstruction after the power cycling test. The reconstruction appears as a milky white discoloration of the diode metallization. It is concentrated at the center of the chip. Especially interesting is the area around the solder void, which can be seen in the X-ray image. The reconstruction is also very pronounced in this region, corroborating that the reconstruction is generated by the temperature swing. The maximum temperature has its peak in the center of the die, while the thermal resistance is locally increased in the area of the solder void. The dissymmetry of the reconstruction clearly follows this temperature profile [Scn99].

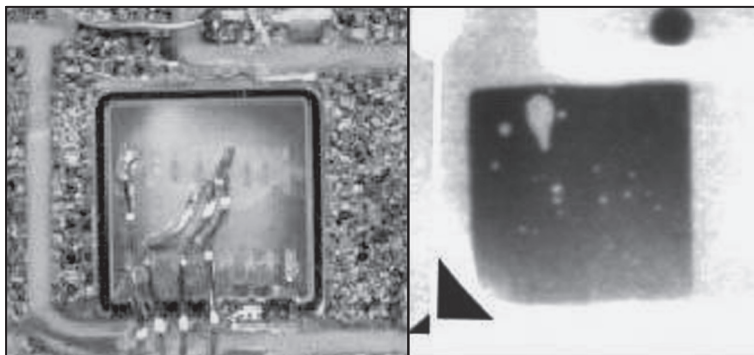
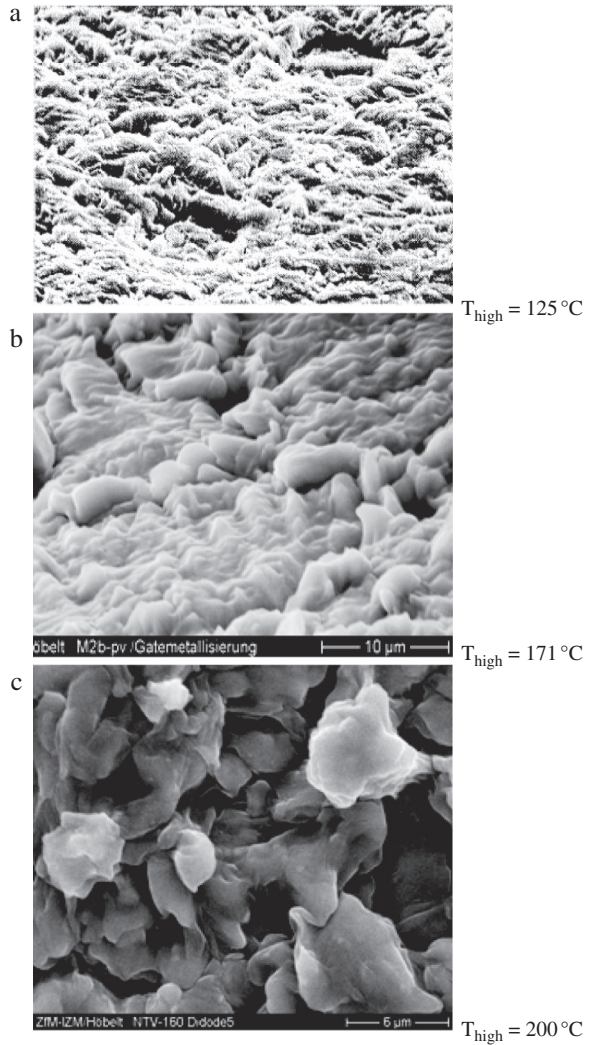


Fig. 11.46 Optical image (*left*) and X-ray image (*right*) of a diode after active power cycling – the reconstruction of the metallization appears as a milky non-reflecting discoloration, which is most pronounced in the chip center and in the area of the solder void [Scn99]

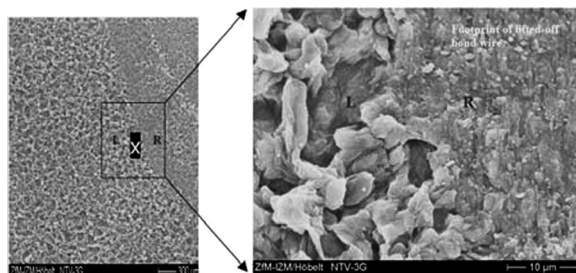
Fig. 11.47 REM images show the augmentation of contact reconstruction with increasing maximum cycle temperature T_{high} during power cycling



The impact of the maximum temperature during power cycling is illustrated in Fig. 11.47. Figure 11.47a shows an IGBT metallization after 3.2 millions of power cycles between 85 and 125°C ; the figure is taken from [Cia02]. Figure 11.47b shows an IGBT metallization after 7250 power cycles with $\Delta T = 131\text{ K}$ and $T_{\text{high}} = 171^{\circ}\text{C}$. Figure 11.47c finally shows the metallization of a diode after 16,800 cycles at $\Delta T = 160\text{ K}$ with $T_{\text{high}} = 200^{\circ}\text{C}$; significant grains of approximately $5\text{ }\mu\text{m}$ diameter appear on the surface leaving voids in the metallization layer.

The reconstruction effect is suppressed beneath wire bond stitches. Figure 11.48 shows a detail of the metallization at the edge of a bond stitch after wire bond lift-off. This diode survived 44,500 cycles with $\Delta T_j = 130\text{ K}$, $T_{\text{high}} = 170^{\circ}\text{C}$. The high number of cycles was achieved because of single-side silver sinter technology

Fig. 11.48 REM image of the edge of bond stitch area after a wire bond lifted-off – the reconstruction is more pronounced outside of the stitch area. The diode failed after approximately 44,500 cycles with $\Delta T_j = 130$ K and $T_{high} = 170^\circ\text{C}$



[Amr06]. Other investigations have shown that a polyimide cover layer suppresses the reconstruction effect as well [Ham01]. This is an expected phenomenon, because any cover layer will restrict the movement of the grains out of the contact layer. Nonetheless remains the high stress in the layer and it can be expected that the initiation and the growth of fractures in the interface of bond stitches is driven by the same CTE mismatch that generates the metallization reconstruction.

The reconstruction of the chip metallization reduces the density of the contact layer and therefore increases the specific resistivity of the contact. Since the layer thickness is typically in the range of 3–4 μm , the movement of grains sized in the range of the layer thickness as in Fig. 11.47c can be expected to change the conductivity of the layer considerably.

The layer resistivity can be measured according to the method of van der Pauw [Pfu76]. For the example of the power cycled diode in Fig. 11.47c, a specific resistance of 0.0456 $\text{m}\Omega\text{ m}$ was measured. The resistivity of an unstressed diode of the same type was found to be 0.0321 $\text{m}\Omega\text{ m}$. This is close to the literature value for pure bulk Al of 0.0266 $\text{m}\Omega\text{ m}$; a slightly higher value can be expected because the chip metallization has a grain structure and contains some small admixture of Si. The observed resistivity increase of 42% during power cycling [Lut08] is a severe change of the device characteristics. Even though only a very small increase of V_F was detected during the power cycling tests of the devices in Figs. 11.47c and 11.48, an impact on the current distribution in the device must be expected which will reduce the lifetime of the power device under high stress conditions.

Latest investigations on device failure under repetitive short-circuit exposure below the critical thermal destruction level have shown that the increase in contact resistance caused by reconstruction of the contact layer is the root cause of the failure [Ara08]. It must be expected that this reconstruction also has an impact on the surge current capability of freewheeling diodes.

11.6.7.6 Solder Fatigue

The degradation of the solder interface is a fundamental failure mode during active power cycling. The so-called solder fatigue is caused by the formation of fractures in the solder interface, which lead to an increase in thermal resistance and are thus accelerating the total failure of the device. In devices with a positive temperature coefficient of the forward voltage drop (i.e. IGBT and MOSFET), the increasing

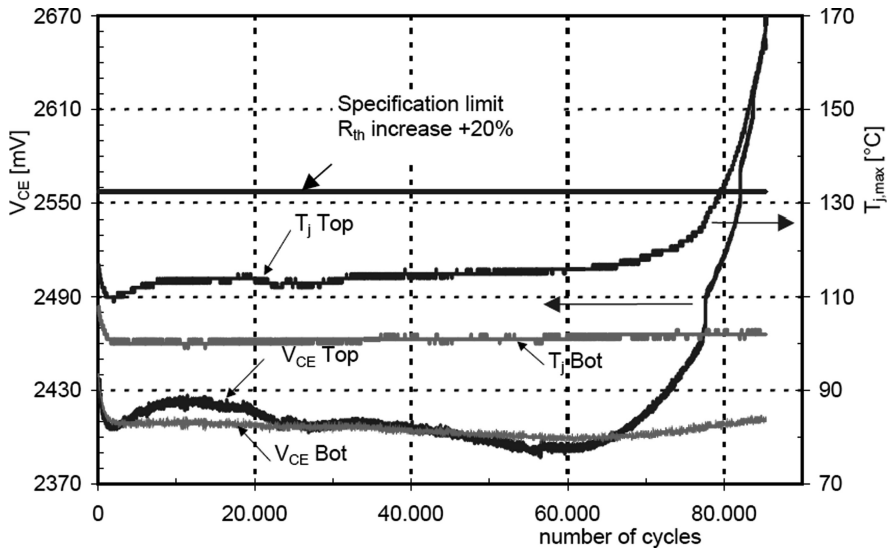


Fig. 11.49 Power cycling results in an IGBT phase leg in a module without base plate with $\Delta T_j = 80$ K [Scn02b]. The temperature evolution is a strong indication of solder fatigue

temperature leads to increasing power losses and therefore expedites the degradation in a positive feedback loop. However, the final end-of-life failure of the conventional module design will typically be the breakdown of the wire bond contacts. If no investigation of the solder interface is performed by scanning acoustic microscopy (SAM) after a power cycling test, the impact of solder fatigue cannot be evaluated and the wire bond breakdown is often mistakenly assumed to be the root cause of failure.

Figure 11.49 shows the evolution of the forward voltage drop and the maximum temperature reached at the end of each heating phase of the IGBTs in the center phase leg of a six pack module without base plate. The maximum temperature starts to increase after 65,000 cycles and generates increasing power losses in the device due to the positive temperature coefficient. After 85,000 cycles, the temperature swing has already increased to $\Delta T_j = 125$ K and it would continue to grow fast until the liquidus temperature of the solder is reached, if the wire bond contacts would not have failed first. This example illustrates that only marginal lifetime can be gained by improving the top side chip contact (i.e. the wire bonds) without improvement of the bottom side contact (i.e. the solder layer), because the increasing temperature amplitude would destroy any top side chip contact.

The geometry of the solder fatigue depicted in the SAM image in Fig. 11.50 follows the expected deterioration pattern. The discontinuity at the chip edges is responsible for a stress peak at the edges and especially at the chip corners. Therefore, the fractures start at the outside corners and edges and propagate toward the chip center. In this case, the arrangement of the four chips in parallel generates

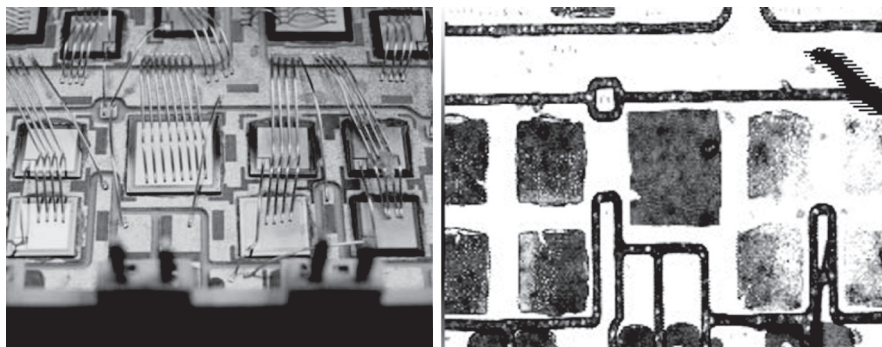


Fig. 11.50 Optical image and SAM image of the IGBT module in power cycling test shown in Fig. 11.46. The four IGBTs in parallel of the failed TOP switch (right side of the images) show the effect of solder fatigue

a temperature distribution with the maximum temperature being located at the chip corners close to the center of this quadruple chip assembly. Thus the degradation of the solder layers starts at the corners pointing toward the center of the group and moves outward.

The continuous improvement of the package thermal resistance and the enhanced heat extraction capability of advanced cooling systems have considerably increased the power density in modern IGBT chips. Assisted by the trend to minimized chip thicknesses (down to 70 μm for latest generation 600 V trench chips), which reduces the lateral thermal conductivity and thus diminishes possible heat spreading effects, the lateral temperature gradient in the chip has become more and more pronounced. Figure 11.51 illustrates this effect, where the diagonal temperature gradient exceeds 40°C for a 12.5 \times 12.5 mm² IGBT on a water-cooled copper heat sink with 9°C cooling liquid temperature [Scn09].

For such pronounced lateral temperature gradients, the stress in the chip center generated by the high temperature exceeds the stress induced by the edge discontinuity and the degradation begins in the center instead of the edges and corners. This is confirmed by the SAM image of a state-of-the-art power module after the power cycling test in Fig. 11.52. Here the damaged region is located in the chip center, indicated by the light areas of high reflection, while the chip edges seem unaffected.

This observation was also reported from other authors. While some publications attribute this phenomenon to special solder types used [Mor01], other authors have observed this effect with lead-free and lead-rich solder systems [Her07]. The characteristics of the solder interface layer might have a small impact on the solder fatigue progress; however, the driving force for the deterioration of the solder interface results from the high stress induced by the differences in thermal expansion.

This change in the failure mechanism could have a considerable impact on the evolution of the degradation process. Fractures in solder interface increase the local thermal resistance of the affected chip region and thus raise locally the chip temperature. If the fractures start at the edges, the temperature of relatively cool chip

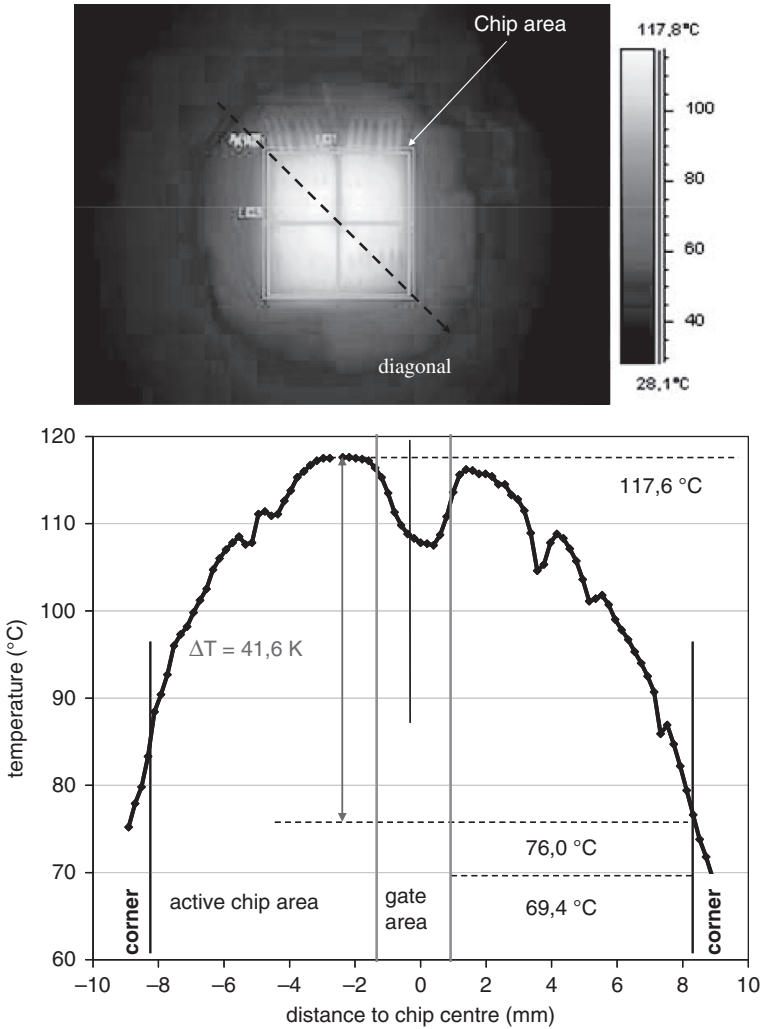


Fig. 11.51 Infrared image of a $12.5 \times 12.5 \text{ mm}^2$ 1200 V IGBT chip heated by a continuous DC current of 150 A. The module was mounted on a Cu water cooler with 9°C cooling liquid temperature. The equilibrium temperature distribution along a diagonal line through the chip center (*bottom* diagram) shows a temperature gradient between center and corner of more than 40°C

regions is increasing, while the maximum temperature remains unchanged in the chip center. The situation is different, when the fractures start at the center, which has the highest temperature to begin with. Therefore, with fractures in the center of the chip, the maximum chip temperature is immediately increased and it can be expected that this positive feedback loop will accelerate the fatigue progress and thus reduce the power module lifetime.

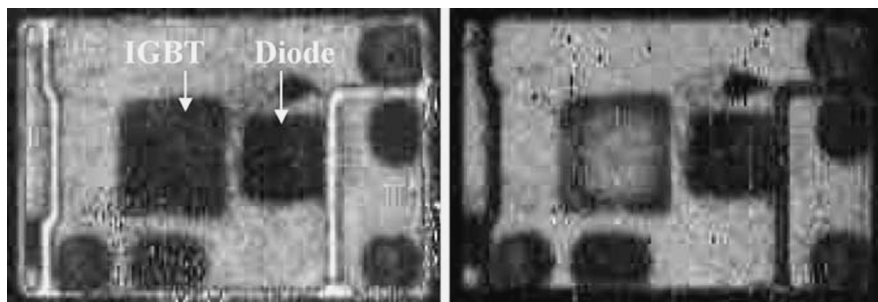
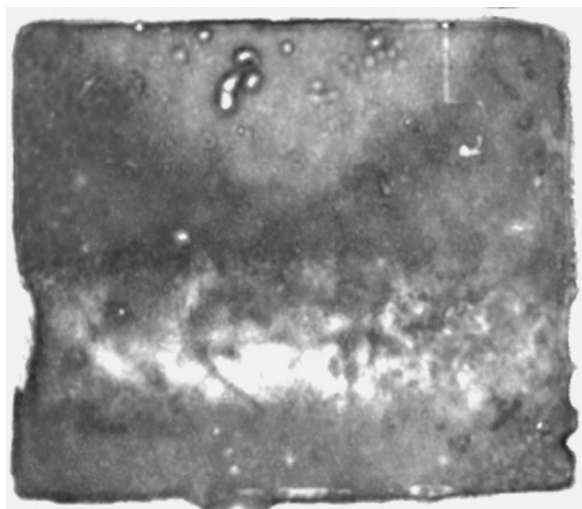


Fig. 11.52 SAM images of the initial solder layer (*left*) in comparison to the end-of-life image (*right*) after 113,400 power cycles of the IGBT with $T_{\text{high}} = 150^{\circ}\text{C}$, $\Delta T_j = 70\text{ K}$, heating phase $\sim 2\text{ s}$ – the unstressed diode solder remains unchanged

Fig. 11.53 SAM image of solder degradation below active power cycled IGBTs in a lead-free substrate solder joint of an AlSiC base plate module



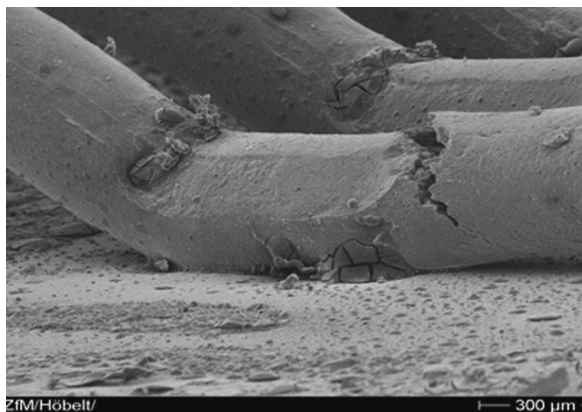
The considerable temperature gradients on the chip level also generate temperature gradients in the solder layer between the substrate and the base plate. Test results from a power cycling test at $\Delta T_j = 67\text{ K}$ and $T_{\text{high}} = 150^{\circ}\text{C}$ on a module with AlSiC base plate show degradation effects in the substrate-to-base plate interface that start below the chip position as shown in Fig. 11.53

These results illustrate the complexity of solder fatigue effects due to the interaction of thermal and mechanical characteristics of the interconnection interface. The problem of solder fatigue must be solved to exceed the limits in reliability of the classical module design.

11.6.7.7 Power Cycling Capability of Molded TO Packages

A high power cycling capability was found for DBC-based transfer molded TO housings, which were described in the context of Fig. 11.6 [Amr04]. The power

Fig. 11.54 Failure analysis of a DBC-based soft-molded TO package after 75,000 power cycles with $\Delta T = 105$ K, showing a footprint of a detached bond wire in the foreground (*left*) and a heel crack in a still attached bond wire



cycling results in Fig. 11.40 were gained in power cycling test with this package type for $\Delta T = 105^\circ\text{C}$ and $T_m = 92.5^\circ\text{C}$. The number of cycles to failure (Weibull 50% accumulated probability) is about a factor of 10 higher than predicted by the LESIT results (Eq. (11.19)) and still significantly above the CIPS 08 model (Eq. (11.20)). Figure 11.54 shows a picture of bond wires in a device which survived 75,000 power cycles under said conditions. On the dark area in the foreground, a bond foot was initially attached. In the first of the still attached bond wires, a heel crack is visible.

The stiff mold material has a similar effect as a bond wire coating; it additionally hinders mechanically the detachment of bond wires from the chip surface. Even though the bond wire shows signs of heavy deterioration, the electrical contact is still maintained. In contrast to standard TO packages with copper lead frames, the implementation of Al_2O_3 substrates accounts for a lower thermal mismatch between the semiconductor material Si and the assembly layer.

The classical TO package with Cu-lead frames (Fig. 11.55) exhibit a great mismatch in thermal expansion between copper and silicon. For large chip sizes, the



Fig. 11.55 Crack in the silicon diode chip in a transfer mold TO package on a Cu-lead frame after 3800 cycles with $\Delta T_j = 110$ K and $T_m = 95^\circ\text{C}$

power cycling capability was found to be clearly inferior to packages with ceramic substrates. In a power cycling test of standard TOs with chips of 63 mm^2 area, two of six chips lost their blocking capability after only 3800 cycles with $\Delta T_j = 110^\circ\text{C}$ and $T_m = 95^\circ\text{C}$. The failure analysis of these TOs revealed cracks in the silicon device as the root cause. Figure 11.55 shows such a fracture of a silicon chip.

Even though no more failures occurred up to more than 38,000 cycles when the test was continued with the four remaining samples, the early failures caused by fractures in the silicon device are alarming. Presumably, the relatively large area of the silicon devices is responsible for these early failures, because this effect was not observed for power cycling tests of smaller chips ($< 30 \text{ mm}^2$) in the same package type.

11.6.7.8 Comparability of Power Cycling Lifetime Curves

The general statement on the comparability of qualification test results given at the beginning of this section holds even more for power cycling results of different manufacturers of power modules. The lifetime characteristics published by different manufacturers are of limited value for the evaluation of the lifetime in real application, because the test conditions and control strategies are mostly not disclosed.

In addition to the selection of the load current, the cooling system, the cycle duration, and the medium temperature – which all have an impact on the power cycling lifetime as discussed before – as well as the reaction to degradation effects during the test is of fundamental importance for the number of cycles to failure during a power cycling test. Four different strategies are possible for the control of a power cycling test, which account for degradation effects completely different:

- Cycle time control with fixed turn-on and turn-off times only. In this strategy, the desired ΔT_j is adjusted by selecting appropriate turn-on and turn-off times. These times are then kept constant during the test and no other control parameters are used to react to degradation effects. This is the most severe test condition, because degradation effects can increase the ΔT_j during the test and thus shorten the lifetime to failure considerably.
- Control of the turn-on and turn-off times by a reference temperature. This is the prevalent strategy used by European manufacturers, where either the case temperature or the heat sink temperature is used as control parameter. This strategy eliminates the impact of any changes of the cooling conditions (i.e. changes in coolant temperature or coolant flow) from the test progress. If the case temperature is used for the control, even changes in the case to heat sink thermal resistance have no impact on the test result.
- Control strategy that maintains constant power losses. This strategy, which is typically combined with fixed turn-on and turn-off times, keeps the power losses generated in each heating phase constant by controlling either the current or the gate voltage. Single bond wire failures increase the on-state voltage of a power device during the test and thus increase the power losses. For devices with a positive temperature coefficient (i.e. IGBT or MOSFET), solder fatigue may increase

the junction temperature and therefore will also increase the on-state voltage of the device (see Fig. 11.49, for example). The control for constant power losses will reduce the losses in these devices artificially and will thus lengthen the lifetime of the device. Some Japanese manufacturers use the control of the gate voltage during power cycling.

- Control strategy to maintain a constant temperature swing ΔT_j . In this strategy, the control parameter is the junction temperature itself, which is measured at the end of each heating phase. Typically, the turn-on time and the turn-off time during the cycling test are controlled to maintain a constant temperature swing, but a control of the current or the voltage drop by means of a gate voltage adaptation could alternatively be applied. In this case, no degradation effect in the module would alter the temperature swing. This is the least challenging test strategy and it will deliver the highest lifetime.

Lifetime curves for power modules always are based on accelerated test results, but they are of great importance for the estimation of lifetime in real applications. Therefore, the test results are extrapolated to real conditions in the field. However, no control strategy is implemented in real converter systems to account for degradation effects in the power module. Only a temperature sensor to monitor the heat sink temperature is incorporated into many power electronic applications. Thus, only the first two strategies should be applied for power cycling tests that are used as a basis for lifetime estimation.

11.6.8 Additional Reliability Tests

A test sequence similar to the example given in Table 11.6 is mandatory for all series products of a power module manufacturer. However, additional test sequences can be negotiated for specific applications.

For applications in extreme environmental conditions, special tests under corrosive atmospheres are recommended. Corrosive gases can interfere seriously with the reliable function of power modules. The silicone soft mold represents almost no protection against corrosive gases. SO_2 interacts with all metal surfaces except noble metals, H_2S is highly corrosive for silver and silver alloys, and Cl_2 together with high humidity will produce HCl , which corrodes non-noble metals, especially Al. The contribution of NO_x is not fully understood today, but its corrosion effect in connection with humidity is comparable to the impact of SO_2 and H_2S . The reliability of non-hermetically sealed modules must be verified in accelerated corrosive atmosphere tests in single or mixed corrosive gas environments for these applications.

Similar corrosion effects are connected with the impact of salt spray. This specific stress condition is found particularly in seaside or off-shore applications, which are typical environments for wind generator systems. The NaCl dissociates in aqueous solution and produces HCl , which over time can penetrate the soft mold cover layer

Semiconductor Power Devices

Physics, Characteristics, Reliability

Lutz, J.; Schlangenotto, H.; Scheuermann, U.; De
Doncker, R.

2011, XII, 536 p., Hardcover

ISBN: 978-3-642-11124-2