

Preface

As LSI industry has been growing, there appear such kinds of CMOS LSI as Microprocessor, MCU, gate array, ASIC, FPGA, and SOC. There is no CMOS LSI that does not use the SRAM memory cell arrays. The best reason is that the SRAM can be fabricated by the same process as logic process, and it does not need extra cost to fabricate. Also, SRAM cell array operates fast and consumes low power in LSI. Despite the SRAM cell size is larger than the other RAM cell such as DRAM cell and Flash, SRAM cell continue to be used in CMOS LSI, thanks to the natures of the cell.

Before 90 nm technology, we can design SRAM cell for CMOS LSI without paying attention to electrical stability, so that we could get operable SRAM bit cell only when we connect the six transistors of the cell. However, after 90 nm technology, we must design SRAM bit cell more carefully, because variability and leakage of transistors in SRAM cell have become large. Also, we must pay attention to such reliability issues as soft errors, and NBTI at low supply voltages.

This book is focusing on the design of CMOS memory cell and memory cell array, taking low voltage operation and reliability into consideration. The authors are specialists who have engaged in these issues for tens of years in Hitachi Ltd, and Renesas Technology Corporation that is currently Renesas Electronics Corporation. I believe this book can help readers understand fundamentals of CMOS SRAM memory cell and cell array design, design methods of memory cell, and cell array taking variability of transistors into considerations, thereby obtaining low power and reliable SRAM arrays. This book also introduces new memory cell design techniques those we can apply to future LSI technologies such as SOI devices.

Acknowledgments

The editors and authors express special thanks to Dr. Kiyoo Itoh of Hitachi Ltd. for encouragement in editing this book. We also appreciate Dr. Toshiaki Masuhara, Dr. Osamu Minato, Mr. Toshio Sasaki, and Dr. Toshifumi Shinohara for leading

the authors in various SRAM and SOC development projects. We would like to appreciate many colleagues, who have been working on the various projects with us.

Tokyo, April 2011

Koichiro Ishibashi
Kenichi Osada

Low Power and Reliable SRAM Memory Cell and Array
Design

Ishibashi, K.; Osada, K. (Eds.)

2011, XII, 144 p., Hardcover

ISBN: 978-3-642-19567-9