

# Chapter 1

## Introduction

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### 1.1 History and Trend of SRAM Memory Cell

Static random access memory (SRAM) has been widely used as the representative memory for logic LSIs. This is because SRAM array operates fast as logic circuits operate, and consumes a little power at standby mode. Another advantage of SRAM cell is that it is fabricated by same process as logic, so that it does not need extra process cost. These features of SRAM cannot be attained by the other memories such as DRAM and Flash memories. SRAM memory cell array normally occupies around 40% of logic LSI nowadays, so that the nature of logic LSI such as operating speed, power, supply voltage, and chip size is limited by the characteristics of SRAM memory array. Therefore, the good design of SRAM cell and SRAM cell array is inevitable to obtain high performance, low power, low cost, and reliable logic LSI.

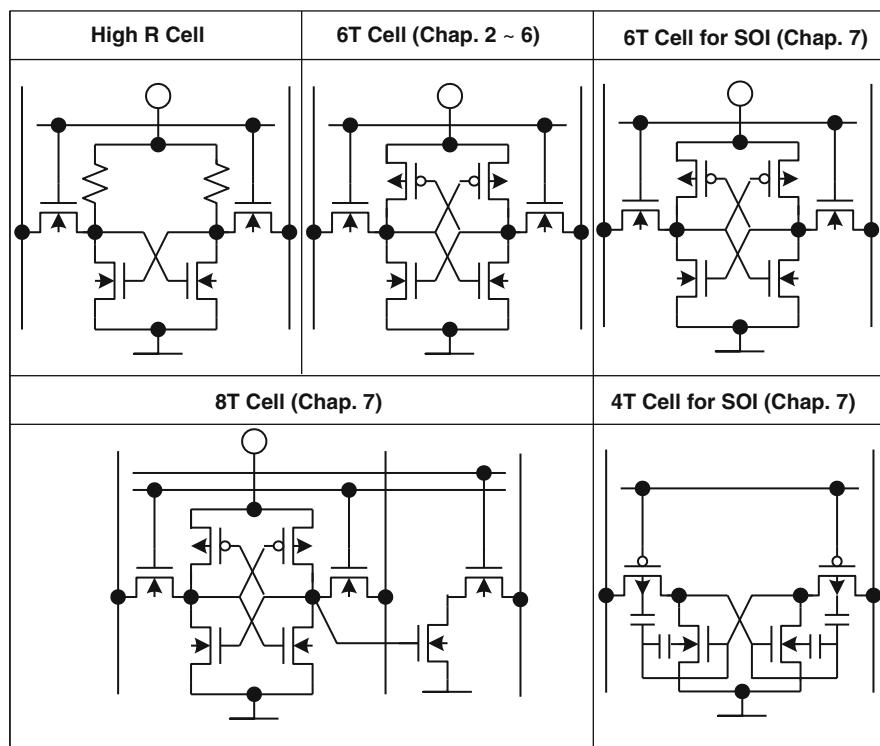
Various kinds of SRAM memory cell has been historically proposed, developed, and used. Representative memory cell circuits are shown in Fig. 1.1.

High-R cell was first proposed as low power 4 K SRAM [1.1]. In the High-R cell, high-resistivity poly-silicon layer is used as load of inverter in the SRAM cell. The High-R cell does not need bulk PMOS, so that the memory cell size was smaller than 6-Tr. SRAM. As the resistivity of the poly-silicon layer is around  $10^{12}$ , the standby current of the memory cell was dramatically decreased to  $10^{-12}$  per cell. The high-R cell was widely used for high density and low power SRAM memory LSI from 4 K to 4 M bit [1.2, 1.3]. The disadvantage of the high-R cell is low voltage operation. At low supply voltages less than 1.5 V, the cell node voltage should be charged to supply voltage level during write operation. Since the resistivity of the load poly-silicon is high, the time required to charge up the high node to supply voltage level is quit large, high-R cell cannot operate at supply voltages less than 1.5 V.

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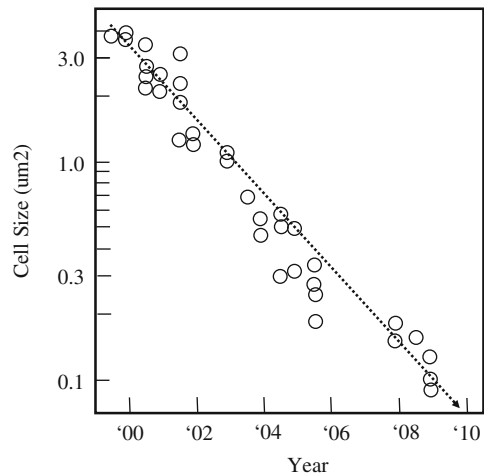


**Fig. 1.1** Representative SRAM memory cell circuits

Six-transistor cell (6T cell), which is sometimes called as full CMOS cell, has been widely used as memories for logic LSIs instead of high-R cell. Most parts of this book deals with this type of memory cell. Although the 6T cell uses PMOS transistors and cell area becomes larger than high-R cell, the cell does not need extra process to logic process. Hence, it has been widely used for memories for logic LSIs even during high-R cell was popular for standalone SRAM. In addition, the PMOS transistors in the cell pull up the cell nodes voltages fast, so that 6T cell operates at lower supply voltages than high-R cell. Therefore, recent supply voltage reduction at advanced technologies has made the 6T cell inevitable for logic LSI. Figure 1.2 shows the size of 6T cell in recent VLSI symposia and International Electron Devices Meeting (IEDM). The cell size has been decreasing by half every 2 years, and it corresponds to density enhancement by Moore's law. Therefore, 6T cell is main-stream memory cell for past, nowadays, and future logic LSIs. Even though structure of transistor will be changed to SOI or FINFET, the 6T cell could be used as the main memory cell for logic LSI.

For further needs to extremely low supply voltage and fast operation, eight-transistor cell (8T cell) has been proposed. Moreover, such special four-transistor

**Fig. 1.2** 6T cell size trend in VLSI and IEDM



cell (4T cell) has been proposed using FINFET transistor structure. These kinds of new SRAM memories are treated in Chap. 7 as future technologies of SRAM cell.

## 1.2 Memory Cell Design Techniques and Array Design Techniques

There are a lot of issues to obtain low power, reliable, and small cell size 6T memory cell. Since the 6T SRAM cell size is scaled by Moore's law, the feature size of transistors in 6T cell is also reduced by Moore's law. Supply voltage of 6T cell is also reduced as the feature size is reduced. Variation in the transistors' threshold voltage has increased and leakage of transistors has also increased by the scaling. Supply voltage of memory cell array has been reduced by the scaling. Recent low power circuit techniques such as Dynamic Voltage Frequency Scaling (DVFS) also need further low voltage operation of memory cell arrays.

The 6T SRAM cell must be designed so that it must be electrically stable at the low supply voltages despite the large variation of transistors. The memory cell size must be as small as possible to obtain small chip size LSIs. The leakage of 6T SRAM cell array must be small despite large leakage in transistors in the cell. In addition, immunity to soft errors due to alpha particles or neutrons must be minimized to obtain reliable LSIs.

This book is focusing on design techniques of SRAM memory cell and array, and covers issues on variability, low power and low voltage operation, reliability, and future technologies.

This book first explains electrical stability issue as fundamentals of electrical operation of 6T cells in Chap. 2. Precise analysis techniques of electrical stability,  $V_{th}$  window analysis, and sensitivity analysis will be introduced in Chap. 3. Using

the analysis techniques, suitable  $V_{th}$  for PMOS and NMOS transistors in 6T cell are determined, so that electrically stable 6T cell at low supply voltages under large variability circumstances is obtained.

The SRAM cell array must operate at low voltage operation to reduce operating power. It must retain data with low leakage at standby mode. Many low power techniques for obtaining low power SRAM have been proposed. This book covers important low power memory cell array design techniques as well as memory cell design techniques.

Two important memory cell design techniques will be introduced in Chap. 4. Lithographically Symmetric Cell (LS cell) is symmetric memory cell layout, so that balance of characteristics in the paired MOS transistors in 6T cell, and good electrical stability can be obtained with advanced super-resolution photolithography. Source voltage control technique, which can reduce not only subthreshold leakage but also gate-induced drain leakage (GIDL), will also be shown to reduce data retention current in standby mode.

SRAM cell array design plays also an important role in reducing power consumption. Dummy cell design technique to adjust activation timing of sense amplifier will be shown in Chap. 5, so that stable SRAM operation is achieved with PVT variation circumstances. Assisting circuits at read operation as well as write operation will be proposed to attain low voltage operation of memory cell arrays. Array boost technique is also shown to obtain the lowest operation voltage of 0.3 V.

Reliability issue is another inevitable issue for SRAM memory cell and cell array design. Among various reliability issues, soft errors caused by alpha particles and neutron particles are serious issue. This book first shows the phenomena of the soft error on SRAM memory cell array and explains mechanisms of the soft errors in Chap. 6. Then memory cell array design techniques drastically reduce the soft errors.

Chapter 7 is the final chapter of this book. This chapter introduces future design techniques of SRAM memory cell and array. Such SRAM cell with such larger number of transistors as 8T cell will be shown to obtain SRAM array with lower supply voltages. Then SRAM memory cell using SOI and FINFET technology will be discussed for future design techniques.

## References

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Design

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