

Preface

This book describes the research carried out by our PhD student Simon Louwsma at the University of Twente, The Netherlands in the field of high-speed Analog-to-Digital (AD) converters. AD converters are crucial circuits for modern systems where information is stored or processed in digital form. Due to increasing data rates and further digitization of systems, the demands on the AD converters are increasing in both sample-rate and number of bits. A fast and accurate AD converter combined with digital signal processing offers an attractive alternative for the analog signal chain still present in many actual receivers. This book offers an exploration of fundamental and practical limits of high speed AD conversion, aiming at a step forward in number of bits and sample-rate, while keeping the power consumption low. To achieve high performance, a technique called time interleaving is used. Time interleaving is the analog equivalent of parallel processing in the digital domain. To implement this, instead of a single Track-and- Hold (T&H), we use a whole series of them, each sampling a bit later than the previous one. In the design example in this book we use 16 T&H circuits, followed by 16 sub-AD converters. The timing alignment of these T&H circuits needs to be extremely accurate, and conventionally, complex timing calibration is used to achieve this. Here however, it is shown that even better performance can be achieved by a compact and good design of the timing circuit without requiring any timing calibration. The circuits use a minimum of transistors that cause timing inaccuracies and special layout techniques are the finishing touch. Thanks to the absence of a control range for the timing, the amount of jitter is also reduced. To save power and to keep the input capacitance low, small sized transistors are used in the time-interleaving T&H circuitry. Only simple DC calibrations are needed to make the 16 paths behave equally over the whole input frequency range. An extensive analysis of accuracy and timing requirements is given and circuit solutions are described in detail. After the input signal is sampled by a T&H section, a sub-ADC finalizes the conversion. Pipeline AD converters are popular for conversion rates around 100 MS/s, but they suffer from the fact that even in the first stage of the pipeline the full accuracy for settling is required. This makes the design of high speed in combination with a high accuracy quite a challenge. Instead of that, we use sub-ADCs based on Successive Approximation (SA). As explained in this book, this has quite some advantages: A SAR ADC contains

less critical analog blocks, and its power consumption can be ten times less than a comparable pipeline ADC. A potential disadvantage of Successive Approximation converters is the relatively low maximum sample-rate. This problem is tackled with a new overrange technique that greatly reduces the demands on settling time per conversion step and that postpones the critical decision to the last conversion step. This offers great advantage over a Pipeline ADC, where the first residue amplifier must settle to full accuracy to avoid unrecoverable analog errors in the conversion process. The work described in this book shows state-of-the art performance and describes techniques, which gain popularity among today's AD converter designers. We enjoyed carrying out the research with Simon and we hope you will enjoy reading the results.

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