Modeling and Simulation of Statistical Variability in Nanometer CMOS Technologies

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1 Introduction

The years of 'happy scaling' are over and the fundamental challenges that the semiconductor industry faces at technology and device level will deeply affect the design of the next generations of integrated circuits and systems. The progressive scaling of CMOS transistors to achieve faster devices and higher circuit density has fuelled the phenomenal success of the semiconductor industry—captured by Moore's famous law [1]. Silicon technology has entered the nano CMOS era with 35 nm MOSFETs in mass production in the 45 nm technology generation. However, it is widely recognised that the increasing variability in the device characteristics is among the major challenges to scaling and integration for the present and next generation of nano CMOS transistors and circuits. The statistical variability of transistor characteristics, which has been previously concern only in the analogue design domain, has become a major concern associated with CMOS transistors scaling and integration [2, 3]. It already critically affects SRAM scaling [4], and introduces leakage and timing issues in digital logic circuits [5].

In the next section we review the major sources of statistical variability in nano CMOS transistors focusing at the 45 nm technology generation and beyond. In Sect. 3 we use advanced 3D physical statistical simulation to forecasts the magnitude of statistical variability in contemporary and future CMOS devices. The compact model strategies suitable for capturing the statistical variability in industrial strength compact models such as BSIM and PSP are outlined in Sect. 4. Section 5 presents example of statistical SRAM circuit simulation employing the statistical compact model strategies discussed in Sect. 4. Finally the conclusions are drawn in Sect. 6.

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2 Sources of Statistical Variability

The statistical variability in modern CMOS transistors is introduced by the inevitable discreteness of charge and matter, the atomic scale non-uniformity of the interfaces and the granularity of the materials used in the fabrication of integrated circuits.

The granularity introduces significant variability when the characteristic size of the grains and irregularities become comparable to the transistor dimensions. For conventional bulk MOSFETs, which are still the workhorse of the CMOS technology, Random Discrete Dopants (RDD) are the main source of statistical variability [6]. Random dopants are introduced predominantly by ion implantation and redistributed during high temperature annealing. Figure 1 illustrates the dopant distribution obtained by the atomistic process simulator DADOS by Synopsys. Apart from special correlation in the dopant distribution imposed by the silicon crystal lattice, there may be also correlations introduced by the Coulomb interactions during the diffusion process. Line Edge Roughness (LER) illustrated in Fig. 2 stems from the molecular structure of the photoresist and the corpuscular nature of light. The polymer chemistry of the 193 nm lithography used now for few technology generations mainly determines the current LER limit of approx 5 nm [7]. In transistors with poly-silicon gate Poly Gate Granularity (PGG) illustrated in Fig. 3 is another important source of variability. This is associated surface potential pinning at the grain boundaries complimented by doping non-uniformity due to rapid diffusion along the grain boundaries [3].

The introduction of high-k/metal gate technology improves the RDD induced variability, which is inversely proportional to the equivalent oxide thickness (EOT). This is due to the elimination of the polysilicon depletion region and better screening of the RDD induced potential fluctuations in the channel from the very high concentration of mobile carriers in the gate. The metal gate also eliminates the PGG induced variability. In the same time it introduces high-k granularity illustrated in Fig. 4 and variability due to work-function variation associated with the metal gate granularity

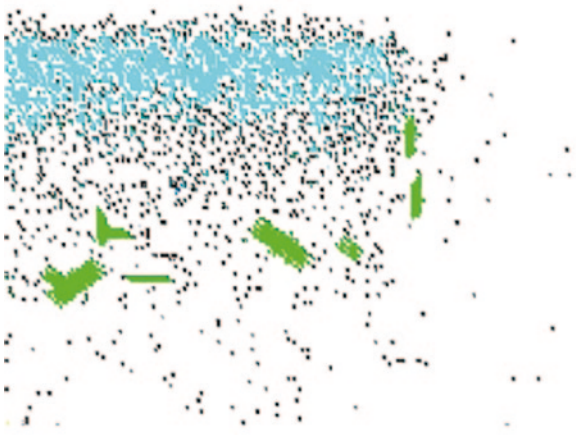

Fig. 1 KMC simulation of RDD. (DADOS, Synopsys)

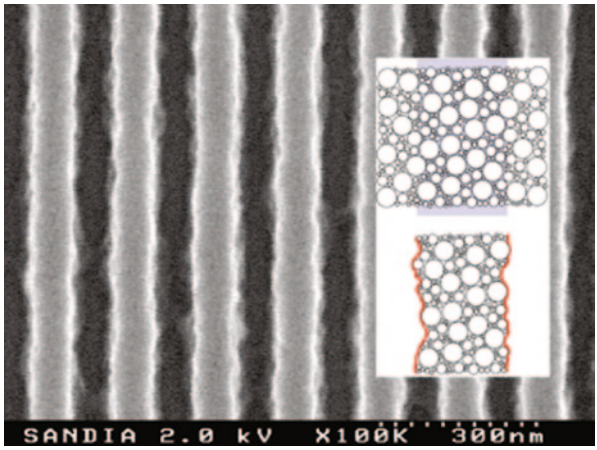

Fig. 2 Typical LER in photoresist. (Sandia Labs)

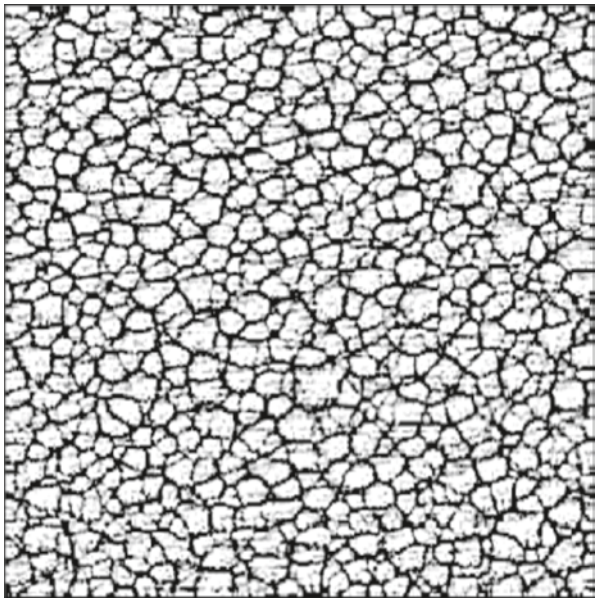

Fig. 3 SEM micrograph of typical PSG from bottom

illustrated in Fig. 5 [8]. In extremely scaled transistors atomic scale channel interface roughness illustrated in Fig. 6 [9] and corresponding oxide thickness and body thickness variations [10] can become important source of statistical variability.

3 Statistical Variability in Advanced CMOS Devices

The simulation results presented in this chapter were obtained using the Glasgow statistical 3D device simulator, which solves the carrier transport equations in the drift-diffusion approximation with Density Gradient (DG) quantum corrections

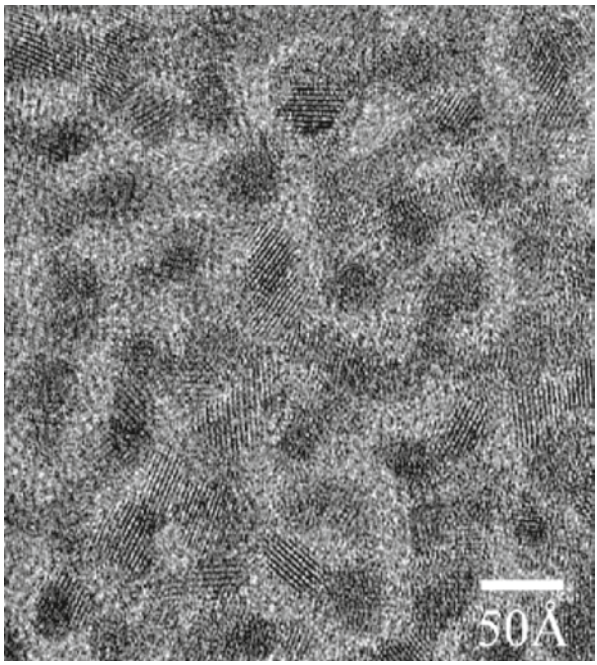

Fig. 4 Granularity in HfON high-k dielectrics. (Sematech)

[11]. In the simulations, the RDD are generated from continuous doping profile by placing dopant atoms on silicon lattice sites within the device S/D and channel regions with a probability determined by the local ratio between dopant and silicon atom concentration. Since the basis of the silicon lattice is 0.543 nm a fine mesh of

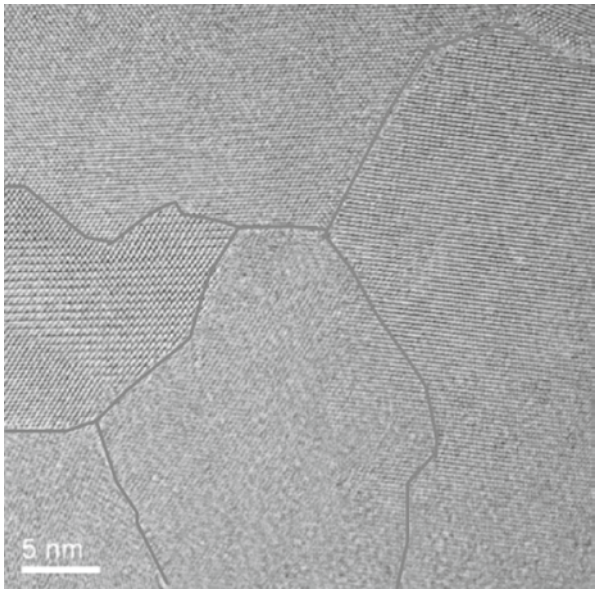

Fig. 5 Metal granularity causing gate work-function variation

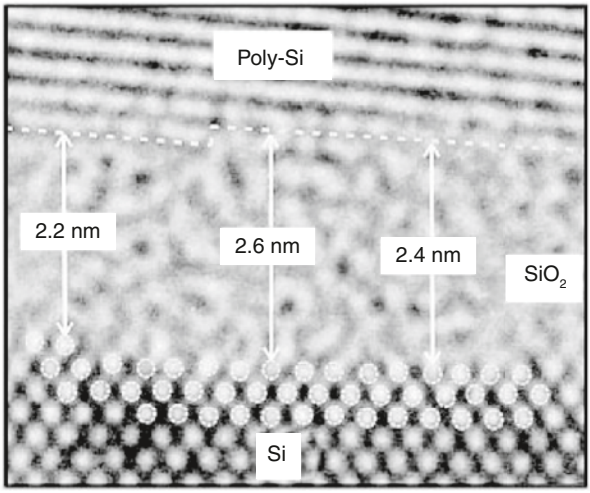

Fig. 6 Interface roughness. (IBM)

0.5 nm is used to ensure a high resolution of dopant atoms. However, without considering quantum mechanical confinement in the potential well, in classical simulation, such fine mesh leads to carrier trapping at the sharply resolved Coulomb potential wells generated by the ionised discrete random dopants. In order to remove this artifact, the DG approach is employed as a quantum correction technology for both electrons and holes [11].

The LER illustrated in Fig. 4 is introduced through 1D Fourier synthesis. Random gate edges are generated from a power spectrum corresponding to a Gaussian autocorrelation function [9], with typical correlation length Λ=30 nm and root-mean-square amplitude Δ=1.3 nm, which is the level that is achieved with current lithography systems. The quoted in the literature values of LER are equal to 3Δ. The procedure used for simulating PGG involves the random generation of poly-grains for the whole gate region [3]: a large atomic force microscope image of polycrystalline silicon grains illustrated at the top of Fig. 3 has been used as a template and the image is scaled according to the average grain diameter (65 nm in the following simulations). Then the simulator imports a random section of the grain template image that corresponds to the gate dimension of the simulated device, and along grain boundaries, the applied gate potential in the polysilicon is modified in a way that the Fermi level remains pinned at a certain position in the silicon bandgap. In the worst case scenario the Fermi level is pinned in the middle of the silicon gap. The impact of polysilicon grain boundary variation on device characteristics is simulated through the pinning of the potential in the polysilicon gate along the grain boundaries. The individual impact of RDD, LER and PSG on the potential distribution in a typical 35 nm bulk MOSFET is illustrated in Figs. 7, 8 and 9 respectively.

The validation of our simulation technology is done in comparison with measured statistical variability data in 45 nm low power CMOS transistors [12]. The simulator was adjusted to match accurately the carefully calibrated TCAD device simulation results of devices without variability by adjusting the effective mass parameters involved in DG formalism, and the mobility model parameters.

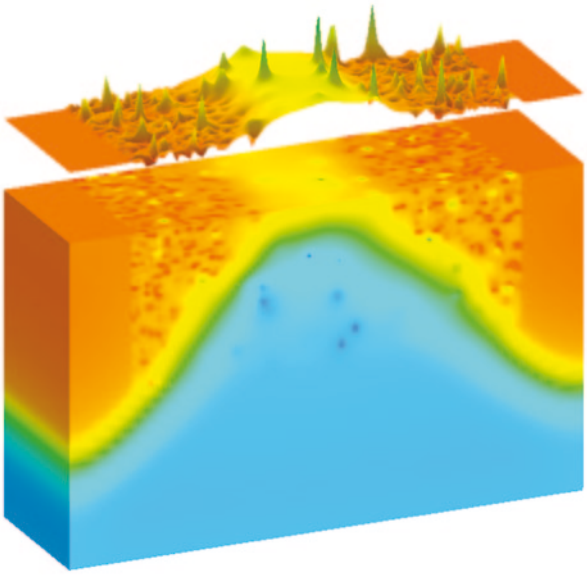

Fig. 7 Potential distribution in a 35 nm MOSFET subject to RDD

The potential distributions in the n- and p-channel transistors in Fig. 7, at gate voltage equal to the threshold voltage and low drain voltage of 50 mV, is illustrated in Fig. 10. In the n-channel transistor RDD, LER and PSG are considered simultaneously while in the p-channel transistor only RDD and LER are considered. The electron concentration at the interface of the two transistors is mapped on top of

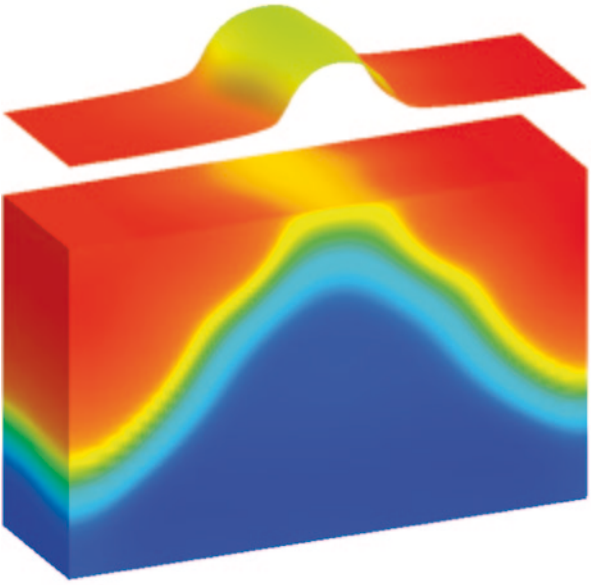

Fig. 8 Potential distribution in a 35 nm MOSFET subject to LER

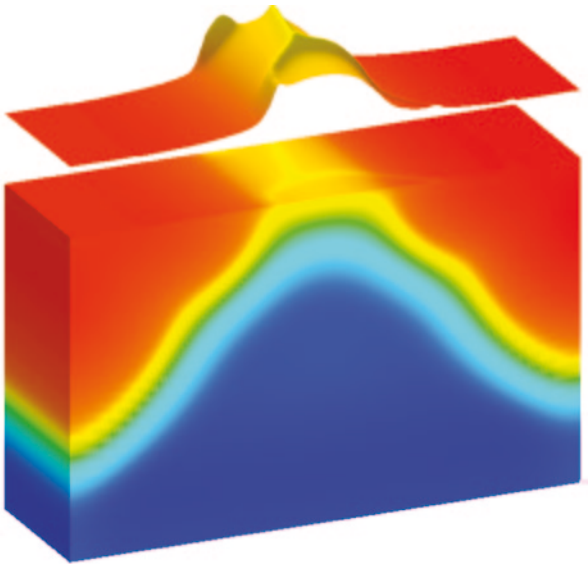

Fig. 9 Potential distribution in a 35 nm MOSFET subject to PSG

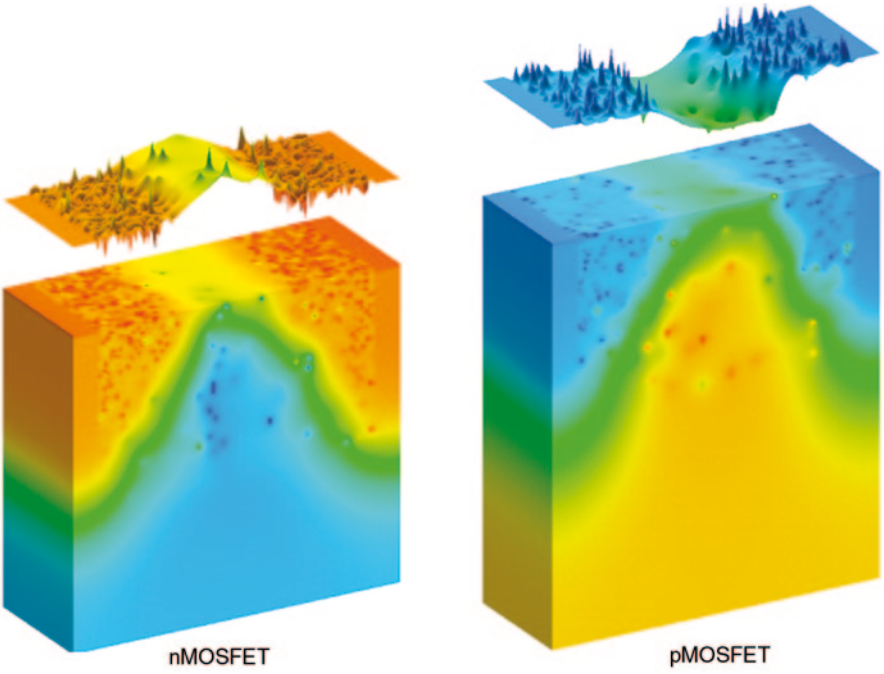

Fig. 10 *Top:* electron (*left*) and hole (*right*) concentration distribution at the interface; *Bottom:* potential distribution

Table 1 σV_T introduced by individual and combined sources of statistical variability

	n-channel MOSFET		*p*-channel MOSFET	
	σV_T (mV) (V_{DS}=0.05 V)	σV_T (mV) (V_{DS}=1.1 V)	σV_T (mV) (V_{DS}=0.05 V)	σV_T (mV) (V_{DS}=1.1 V)
RDD	50	52	51	54
LER	20	33	13	22
PSG	30	26	–	–
Combined	62	69	53	59
Experimental	62	67	54	57

the potential distributions. For example acceptors in the channel of the n-channel transistor create sharp localized potential barrier for the electrons near the interface but act as potential wells for the holes in the substrate. In the same time the donors in the source/drain regions create sharp potential well for electrons.

The simulation results for the standard deviation of the threshold voltage σV_T introduced by individual and combined sources of statistical variability are compared with the measured data in Table 1. In the n-channel MOSFET case the accurate reproduction of the experimental measurements necessitates the assumption that, in addition to RDD and LER, the PSG related variability has to be taken into account. Good agreement has been obtained assuming that the Fermi level at the n-type poly-Si gate grain boundaries is pinned in the upper half of the bandgap at approximately 0.35 eV below the conduction band of silicon.

However, in the p-channel MOSFET case the combined effect of just the RDD and LER is sufficient to reproduce accurately the experimental measurements. The reason for this is the presence of acceptor type interface states in the upper half of the bandgap which pin the Fermi level in the case of n-type poly-Si, and the absence of corresponding donor type interface states in the lower part of the bandgap which leaves the Fermi level unpinned in the case of p-type poly-Si [13].

In order to foresee the expected magnitude of statistical variability in the future we have studied the individual impact of RDD, LER and PSG on MOSFETs with gate lengths 35, 25, 18, 13 and 9 nm physical gate length. We also compare the results with the statistical variability introduced in the same devices when RDD, LER and PSG are introduced in the same devices simultaneously. The scaling of the simulated devices is based on a 35 nm MOSFET published by Toshiba [14] against which our simulations were carefully calibrated. The scaling closely follows the prescriptions of the ITRS in terms of equivalent oxide thickness, junction depth, doping and supply voltage. The intention was also to preserve the main features of the reference 35 nm MOSFET and, in particular, to keep the channel doping concentration at the interface as low as possible. Figure 11 shows the structure of the scaled devices. More details about the scaling approach and the characteristics of the scaled devices may be found in [11].

Figure 12 compares the channel length dependence of σVT introduced by random dopants, line edge roughness and poly-Si grain boundaries with Fermi level

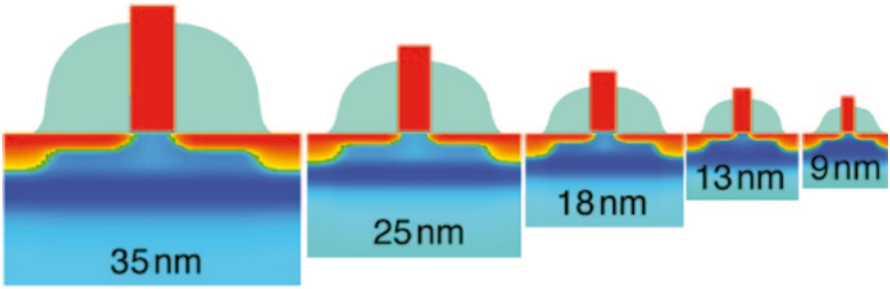

Fig. 11 Examples of realistic conventional MOSFETs scaled from a template 35 nm device according to the ITRS requirements for the 90, 65, 45, 32 and 22 nm technologies, obtained from process simulation with Taurus Process

pinning. The average size of the polysilicon grains was kept at 40 nm for all channel lengths. Two scenarios for the magnitude of LER were considered in the simulations. In the first scenario the LER values decrease with the reduction of the channel length following the prescriptions of the ITRS 2003 of 1.2, 1.0, 0.75, and 0.5 nm for the 35-, 25-, 18-, and 13-nm channel length transistors, respectively. In this case the dominant source of variability at all channel lengths are the random discrete dopants. The variability introduced by the polysilicon granularity is similar to that introduced by random discrete dopants for the 35 nm and 25 nm MOSFETs, but at shorter channel lengths the random dopants take over. The combined effect of the three sources of variability is also shown in the same figure. In the second scenario LER remains constant and equal to its current value of approximately 4 nm ($\Delta = 1.33$ nm). The results for the 35 nm and the 25 nm MOSFETs are very similar to the results with scaled LER but below 25 nm channel length LER rapidly becomes the dominant source of variability.

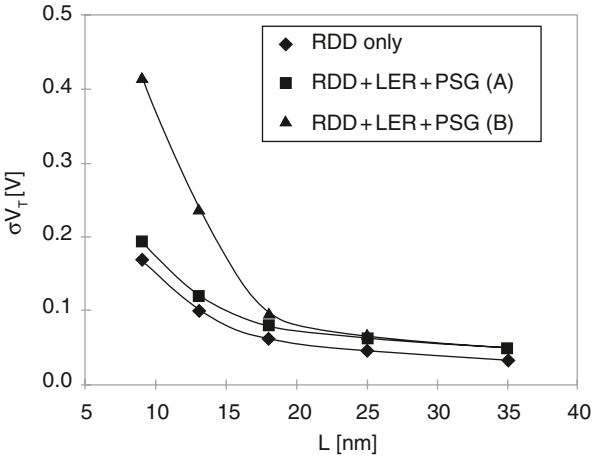

Fig. 12 Channel length dependence of σV_T introduced by random dopants, line edge roughness and poly-Si granularity: *(A)* LER scales according ITRS; *(B)* LER = 4 nm

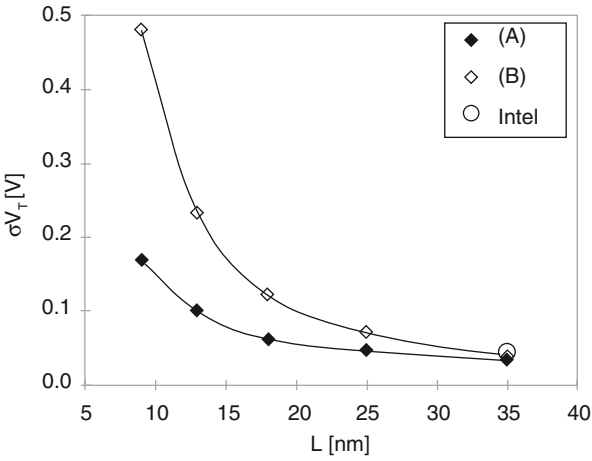

Fig. 13 Channel length dependence of σV_T introduced by random dopants, line edge roughness and poly-Si granularity: *(A)* t_{ox} scales according ITRS; *(B)* $t_{ox} = 1$ nm

Figure 12 is analogous to Fig. 13 exploring the scenario of the oxide thickness, which is difficult to scale further. The LER is scaled according to the ITRS requirements listed above. Even with the introduction of high-k gate stack it is likely to remain stagnated at 1 nm. This will lead to an explosion in the threshold voltage variability for bulk MOSFETs with physical channel length below 25 nm.

4 Statistical Compact Model Strategy

It is very important to be able to capture the simulated or measured statistical variability in statistical compact models since this is the only way to communicate this information to designers [15]. Previous research on statistical compact model identification was focused mainly on variability associated with traditional process variations resulting from poor control of critical dimensions, layer thicknesses and doping clearly related to specific compact model parameters [16].

Unfortunately, the current industrial strength compact models do not have natural parameters designed to incorporate seamlessly the truly statistical variability associated with RDD, LER, PGG and other relevant variability sources. Despite some attempts to identify and extract statistical compact model parameters suitable for capturing statistical variability introduced by discreteness of charge and matter this remains an area of active research [16, 17]. Figure 14 shows the spread in ID–VG characteristics obtained from 'atomistic' simulator due to the combined effect of RDD, LER and PGG.

We use the standard BSIM4 compact model to capture the information for statistical variability obtained from full 3D physical variability simulation. The statistical extraction of compact model parameters is done in two stages [17].

In the first stage, one complete set of BSIM4 parameters is extracted from the I–V characteristics of 'uniform' (continuously doped, no RDD, LER and PGG) set of devices with different channel lengths and widths and process flow identical to the one of the 35 nm testbed transistor (Fig. 15). Target current voltage char-

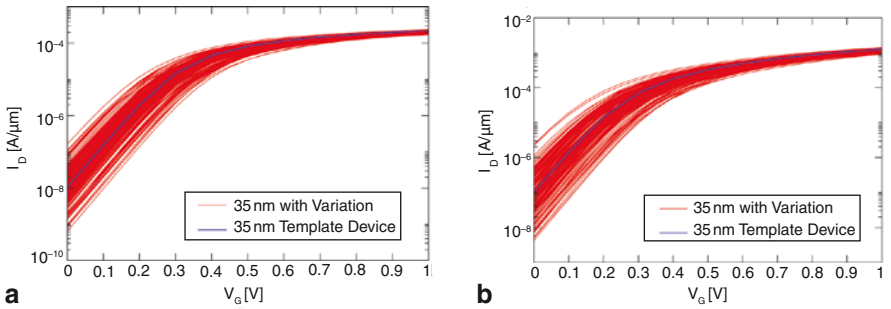

Fig. 14 Variability in the current voltage characteristics of a statistical sample of 200 microscopically different 25 nm square (W=L) n-channel MOSFETs at **a** V_D=50 mV and **b** V_D=1 V

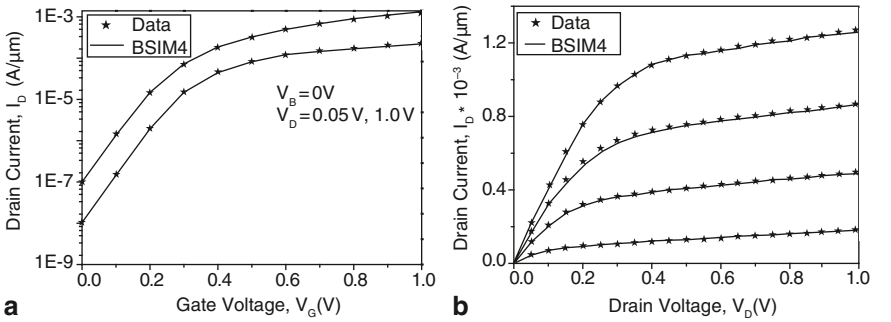

Fig. 15 Comparison of **a** I_D–V_G characteristics, **b** I_D–V_D for characteristics for 'uniform' devices obtained from physical simulations and BSIM

acteristics are simulated over the complete device operating range and parameter extraction strategy combining group extraction and local optimization is employed. Figure 16 compares the corresponding BSIM4 generated I–V characteristics of the 35 nm transistor with the original device characteristics obtained from our 'atomistic' simulator. The RMS error for this extraction is 2.8%.

At the second stage, we re-extracted a small carefully chosen subset of the BSIM4 model parameters from the physically simulated characteristics of each microscopically different device in the statistical ensemble keeping the bulk of the BSIM parameters unchanged. The transfer (ID–VG) characteristics at low and high drain bias are used as extraction target at this stage. The seven re-extracted model parameters are L_{pe0}, R_{dswmin}, N_{factor}, V_{off}, A_1, A_2 and D_{sub}.

Figure 16 compares the BSIM4 results for the worst, the best and the typical devices with the physically simulated device characteristics. The good match between the BSIM results and the physically device characteristics validates the choice of seven parameters which guaranty high accuracy of the compact model over the whole statistical range of physically simulated device characteristics. Figure 17 illustrates the distribution in the error of the 200 statistically different BSIM4 cards depending on the density of the data points in the ID–VG characteristics used as

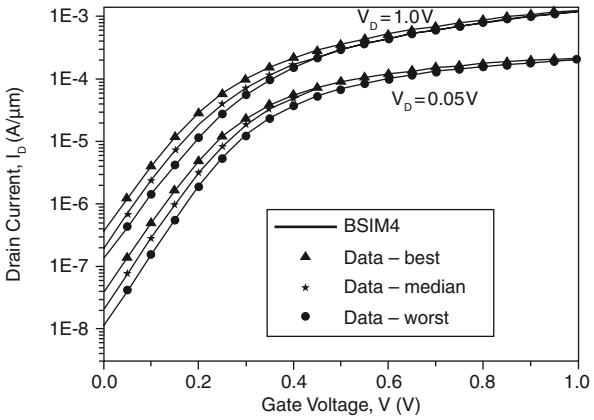

Fig. 16 Comparison of physical and simulation results obtained after second stage statistical extraction for the devices with best, worst and median extraction error

targets in the statistical compact model extraction. Relatively few simulation data points are needed to extract high accuracy statistical compact model parameters.

Above statistical compact model extraction and 3D physical device simulation are based on minimum size square device (W = L), which has the maximum magnitude of statistical variation. However, in real circuits, most of devices have multi-width/length ratio value. In order to reproduce the right statistical behavior of such devices in statistical circuit simulation, wider device are constructed by connecting in parallel minimum size devices randomly selected from the statistic compact model library.

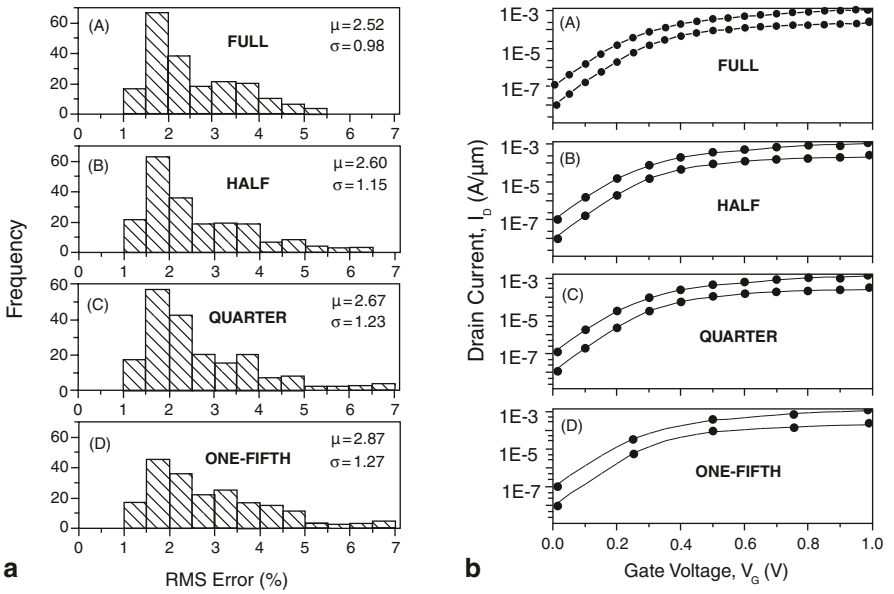

Fig. 17 Distribution of the statistical error as a function of a different number of data points on the target I_D–V_G characteristics used in the statistical compact model extraction

5 Impact of Statistical Variability on SRAM

One area where the digital and the analogue design expertise overlap is in the design of SRAM and particularly SRAM cells which are extremely sensitive to statistical variability. The statistical circuit simulation methodology described in the previous section, which can transfer all the fluctuation information obtained from 3D statistical device simulations into circuit simulation, is employed to investigate the impact of RDF on 6T and 8T SRAM stability for the next three generations of bulk CMOS technology. In the following discussions, we use 25, 18 and 13 nm channel length transistors from Sect. 3.

Currently, 6T SRAM is the dominant SRAM cell architecture in SoC and microprocessors. However, the disturbance of bit lines on the data retention element during read access makes the 6T cell structure vulnerable to statistical variability, which in turn will have a huge impact on 6T SRAM's scalability. The functionality of SRAM is determined by both static noise margin (SNM) defined as the minimum dc voltage necessary to flip the state of the cell and the write noise margin (WNM) defined as the DC noise voltage needed to fail to flip a cell during a write period. The meaning of SNM and WNM is defined in Fig. 18. Figure 19 illustrates the statistical nature of SNM and WNM in the presence of statistical transistor variability.

The magnitude of WNM in SRAM is mainly determined by the load and access transistors illustrated in the 6T SRAM schematics inset in Fig. 20. Since they are the smallest transistors in an SRAM cell, the WNM variation will be larger than the SNM variation. However, the mean value of WNM is much larger than its SNM counterpart. Previous studies [18] suggested that under normal circumstances the limiting factor for the operation of bulk 6T SRAM cells is SNM.

The statistical circuit simulation results for the distribution of SNM for 6T SRAM with the cell ratio of 2 is shown in Fig. 20, while the schematic of a 6T

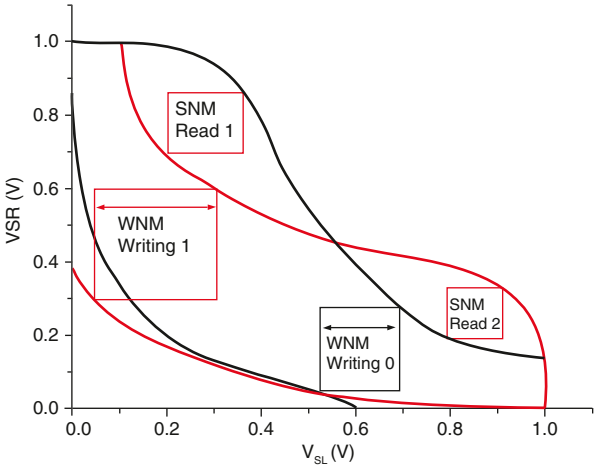

Fig. 18 Static voltage transfer characteristics and definition of SNM and WNM

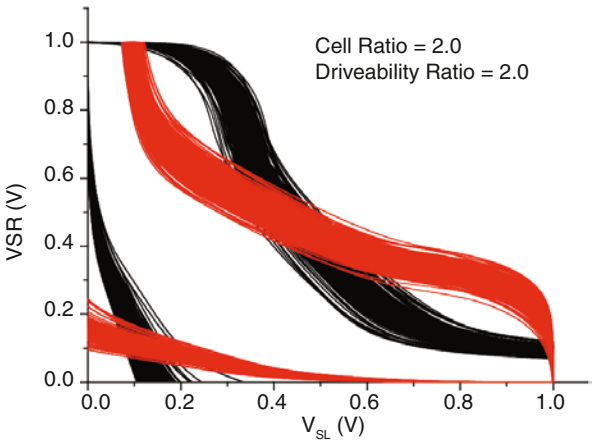

Fig. 19 Statistical behavior of the SNM and WNM of SRAM made of 25 nm bulk MOSFETs subject to RDD

SRAM cell with the bias configuration at the initiation of read operation is illustrated in the inset. The cell ratio is defined as the ratio of the driver transistor to access resistor channel widths. For the 13 nm generation, around 2% of SRAM cells with cell ratio of 2 are not readable even under ideal conditions since their SNM values are negative. The standard deviation σ of SNM, normalized by the

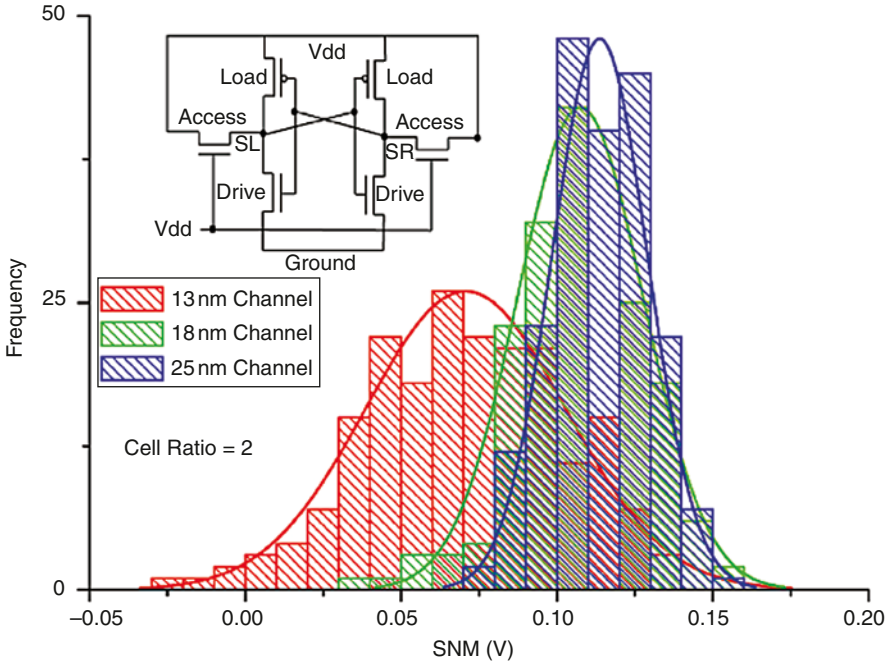

Fig. 20 Distribution of 6T SRAM SNM over an ensemble of 200 SRAM cells for 25, 18 and 13 nm generations

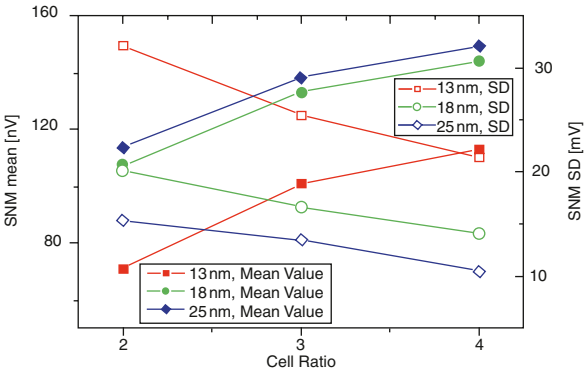

Fig. 21 Mean value and SD of 6T SRAM SNM against SRAM cell ratio

average value μ of the SNM increases from 13% for the 25 nm generation, to 19% for the 18 nm generation, and reaches 45% for the 13 nm generation. As a guideline, $\mu - 6\sigma$ is required to exceed approximately 4% of the supply voltage to achieve 90% yield for 1 Mbit SRAM's. Although the 25 nm generation is three times better with respect to SNM fluctuation performance compared to the 13 nm generation at cell ratio of 2, it still cannot meet the "$\mu - 6\sigma$" test on yield control.

Increasing the cell ratio is the most straightforward way to improve SNM performance of a SRAM cell [19]. The mean value (μ) and the standard deviation (σ) of SNM at different SRAM cell ratios are shown in Fig. 21, which clearly illustrates the benefits of larger cell ratio. For the 25 nm transistors, the increase of the cell ratio from 2 to 4 results in nearly two times NSD of SNM improvement, and the "$\mu - 6\sigma$" criterion is met at a cell ratio of 3. Although the 18 nm and 13 nm generations follow a similar trend, a cell ratio of 4 is required for 18 nm technology in order to achieve reasonable yield. For the 13 nm generation, a cell ratio of 4 can only achieve the level of performance of the 18 nm generation at a cell ratio of 2. At the same time, the increase in the cell ratio tends to degrade the WNM. Therefore, the approach of increasing the cell ratio becomes less attractive for extremely scaled devices even from the prospect of the yield.

6 Conclusions

The statistical variability introduced by discreteness of charge and matter has become one of the major concerns for the semiconductor industry. More and more the strategic technology decisions that the industry will be making in the future will be motivated by the desire to reduce statistical variability. The useful life of bulk MOSFETs, from statistical variability point of view, can be extended below the 20 nm technology mark only if the line edge roughness and the equivalent oxide thickness could be successfully scaled to the required values. SRAM which uses

minimum channel width transistors is the most sensitive part of the integrated systems in respect of statistical variability and needs special care and creative design solution in order to take full advantage from scaling in present and future technology generations.

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