

Chapter 2

Fabrication of Nanowire Crossbars

Nanowire crossbars gained an increasing interest in the last years, namely because the fabrication techniques have become more mature and versatile. Parallel research works have been carried out on different levels ranging from device to circuit and system levels in order to identify and address the challenges facing the utilization of this emerging paradigm in the future.

Interestingly, the circuit and system level problems and their proposed solutions depend on some properties of the fabrication techniques. Thus, understanding the fabrication techniques and the device properties enable a better assessment of the global problem. Numerous fabrication technologies have been suggested previously, focusing on different objectives. Some of them focus on the use of CMOS techniques while shrinking the dimensions below the CMOS limits [1]. Other techniques focus on reducing the pitch far below the CMOS limits by using novel methods that are not CMOS-compatible and that may be too expensive for mass production of VLSI systems [2]. In another set of techniques, the focus is to integrate the nanowires into vertical stacks in a CMOS-compatible way, without any optimization of the nanowire pitch [3–5]. These are just example of the different objectives of some previous approaches. A more detailed survey of the available techniques is given in this chapter.

None of the proposed solutions targeted the fabrication of nanowires with sub-lithographic dimensions and pitch, while using only CMOS processing steps. The goal of the work reported in this chapter is to shrink both nanowire dimensions and pitch below the photolithography limit, while keeping the fabrication technique cost-efficient and CMOS-compatible, in the sense that it uses only standard CMOS processing steps. Since the constraint on the technology process is relaxed (i.e., any standard CMOS steps are suitable), then the fabrication is carried out with the available facilities at the *Center for Micro- and Nanotechnologies (CMI)* at EPFL [6]. The ambitious fabrication technique that has been developed, has the advantage of using only standard photolithography and CMOS fabrication steps, with the available photolithography limit of 0.8 μm , yet achieving sub-photolithographic device pitch down to less than 40 nm.

Parts of this chapter have been published in [7]. It is organized as follows. First the different nanowire fabrication technologies and the various integration techniques of nanowires into crossbar structures are surveyed. Then, the proposed process flow and the available fabrication facilities at the CMI are presented. Next, the encountered fabrication challenges are discussed and the accordingly optimized process is explained. Thereafter, the structural and electrical characterization results are presented. Finally, the advantages and limits of the developed fabrication technique are discussed and the chapter is concluded with the a summary of the contributions of the work at this level.

2.1 Nanowire Fabrication Techniques

Various nanowire fabrication techniques have been proposed in the last decade. They follow two main paradigms: the so-called bottom-up and top-down approaches. Bottom-up approaches are based on the growth of nanowires by generally using nanoscale metallic catalysts; they are subsequently dispersed into a solution and transferred onto the substrate to be functionalized. In contrast, top-down approaches use various types of patterning technique directly on the functional substrate, which are possibly combined with smart processing methods that will be explained in this section in order to reduce the nanowire thickness below the photolithography limit.

2.1.1 Bottom-up Techniques

2.1.1.1 Vapor-Liquid-Solid Growth

One of the widely used bottom-up techniques is the *vapor-liquid-solid* (VLS) process, in which the generally very slow adsorption of a silicon-containing gas phase onto a solid surface is accelerated by introducing a catalytic liquid alloy phase. The latter can rapidly adsorb vapor to a supersaturated level; then the crystal growth occurs from the nucleated catalytic seed at the metal-solid interface. Crystal growth with this technique was established in the 1960s [8] and silicon nanowire growth is today mastered with the same technique.

The VLS process allows for the control of the nanowire diameter and direction growth by optimizing the size and composition of the catalytic seeds and the growth conditions, including temperature, pressure and gas composition in the chamber. In [9], defect-free silicon nanowires were grown in a solvent heated and pressurized above its critical point, using alkanethiol-coated gold monocrystals. Figure 2.1 depicts the growth process and *transmission electron microscope* (TEM) images of the grown nanowires. The nanowire diameters were ranging from 40 to 50 Å, their length was about several micrometers, and their crystal orientation was controlled with the reaction pressure.

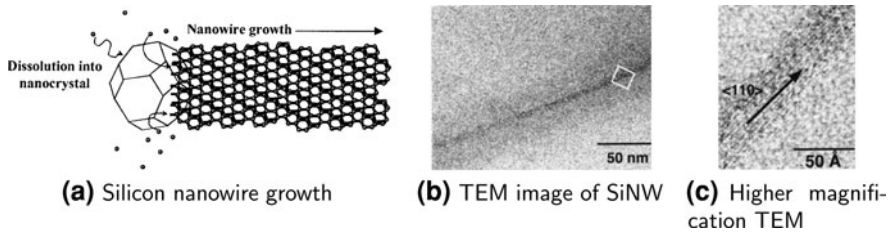


Fig. 2.1 Vapor-liquid-solid growth of a silicon nanowire [9]: **a** Free Si atoms from silane dissolve in the Au seed until reaching the Si:Au supersaturation. Then Si is expelled as nanowire. **b** TEM image of SiNW synthesized at 500°C in hexane at 200 bar. **c** TEM of a part of SiNW inside the square in **b** shows high crystalline SiNWs

2.1.1.2 Laser-Assisted Catalytic Growth

A related technique to VLS is the laser-assisted catalytic growth. High-powered, short laser pulses irradiate a substrate of the material to be used for the nanowire growth. The irradiated material either evaporates, sublimates or converts into plasma. Then, the particles are transferred onto the substrate containing the catalyst, where they can nucleate and grow into nanowires. This technique is useful for nanowire materials that have a high melting point, since the laser pulses locally heat the substrate generating the particle for the nanowire growth. It is also suitable for multi-component nanowires, including doped nanowires, and for nanowires with a high-quality crystalline structure [10].

2.1.1.3 Chemical Vapor Deposition

The *chemical vapor deposition (CVD)* method was shown to be an interesting technique used with materials that can be evaporated at moderate temperatures [11]. In a typical CVD process, the substrate is exposed to volatile precursors, which react on the substrate surface producing the desired nanowires. In [12], the CVD method was applied to fabricate nanowires based on different materials or combinations of materials, including Si, SiO₂ and Ge.

2.1.1.4 Opportunities and Challenges of Bottom-up Approaches

The bottom-up techniques offer the ability of doping the as-grown nanowires in situ, i.e., during the growth process. In [10], the laser catalytic growth was used in order to control the boron and phosphorus doping during the vapor phase growth of silicon nanowires. The nanowire could be made heavily doped in order to approach a metallic regime, while insuring a structural and electronic uniformity. Another more advanced option offered by the bottom-up approaches consists in alternating the doping regions or the grown materials along the nanowire axis, as

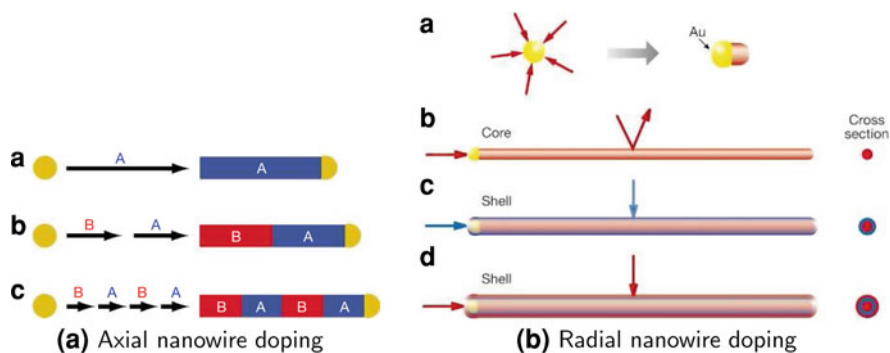


Fig. 2.2 In-situ nanowire doping: **a** Doping along the nanowire axis (axial doping) [13]. **b** Doping around the nanowire axis (radial doping) [12]

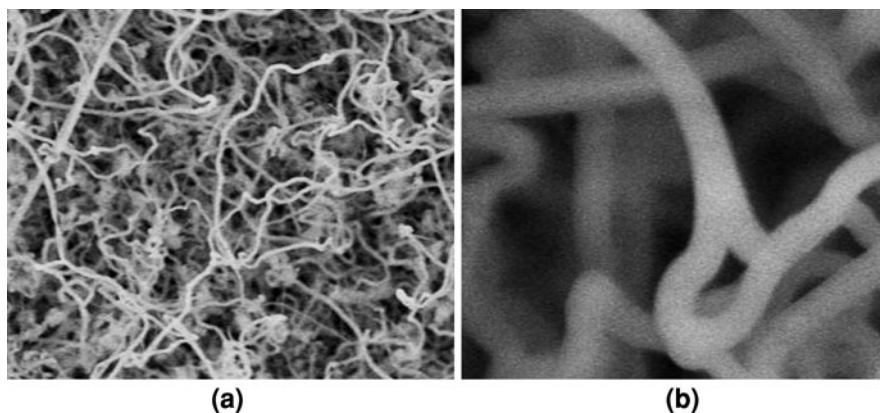


Fig. 2.3 Growth of meshed nanowires [14]: **a** SEM image of gold-catalyzed growth of SiNWs on $\text{Si}_3\text{N}_4/\text{Si}$ substrate. Image width = $7\ \mu\text{m}$. **b** High-magnification image of branched nanowires. Image width = $0.7\ \mu\text{m}$

illustrated in Fig. 2.2a [13, 15]. The growth of concentric shells with different materials around the nanowire axes was also demonstrated in [12], as illustrated in Fig. 2.2b.

The grown nanowires can either represent a random mesh laid out laterally over the substrate (Fig. 2.3) [14], or they can stand vertically aligned with respect to the substrate (Fig. 2.4) [16, 17]. The growth substrate is in general different from the functional substrate. Consequently, it is necessary to disperse the as-grown nanowires in a solution, and then to transfer them onto the functional substrate, making the process more complex. In [18], the nanowires were dispersed in ethanol; then the diluted nanowire suspension was used to flow-align the nanowires by using microfluidic channels. A similar technique was used in [19] in order to assemble arrays of nanowires through fluidic channel structures formed between

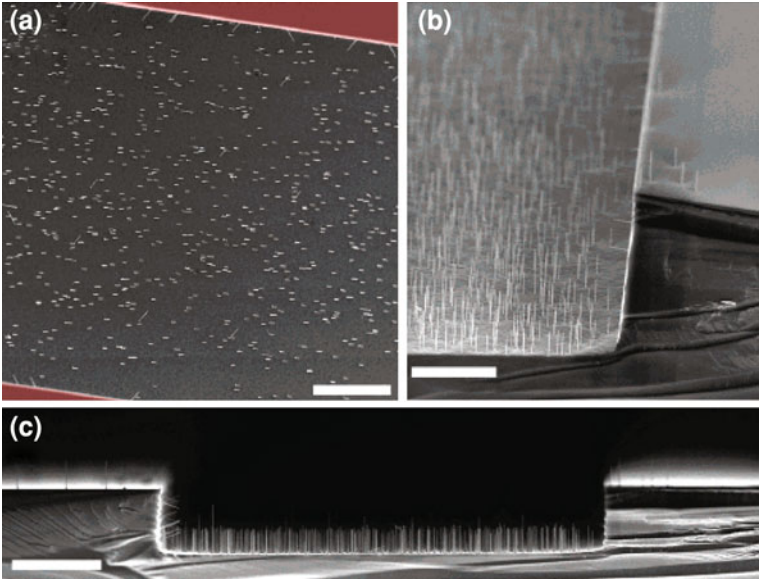


Fig. 2.4 Growth of vertical nanowires [16]: **a** Conformal growth of nanowires to the substrate. **b** Tilted SEM image and **c** a cross-sectional SEM image of the structure. *Scale bars 10 μm*

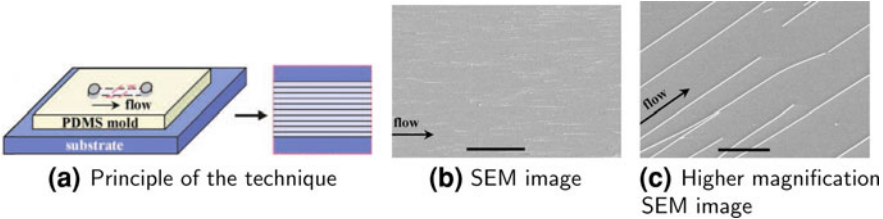


Fig. 2.5 PDMS-mold-based assembly of InP nanowires [19]: **a** Schematic representation of the technique. **b** SEM image of the aligned nanowires (*scale bar = 50 μm*). **c** Higher magnification SEM image of the aligned nanowires (*scale bar = 2 μm*)

a *polydimethylsiloxane* (PDMS) mold and a flat substrate. This technique yields parallel nanowires over long distances, as shown in Fig. 2.5.

2.1.2 Top-Down Techniques

The top-down fabrication approaches have in common the utilization of CMOS steps or hybrid steps that can be integrated into a CMOS process, while keeping the process complexity low and the yield high enough. They also have in common the ability of defining the functional structures (nanowires) directly onto the

functional substrate, with no need of dispersion and transfer of nanowires. Any top-down process uses patterning in a certain way: the patterning technique can be based on a mask, such as in standard photolithography or in other miscellaneous mask-based techniques, or it can be maskless, i.e., using a nanomold for instance.

2.1.2.1 Standard Photolithography Techniques

These techniques use standard photolithography to define the position of the nanowire. Then, by using smart processing techniques, including the accurate control of the etching, oxidation and deposition of materials, it is possible to scale the dimensions down far below the photolithographic limit.

In [20], silicon nanowires were defined on bulk substrates by using CMOS processing steps. First, a Si_3N_4 nitride rib was defined on the substrate. Then, the isotropic etch defined the nanowire underneath the rib. Well controlled self-limited oxidation and subsequent etching steps resulted in silicon nanowires with different cross-section shapes and dimensions, and with a nanowire diameter down to 5 nm.

A related fabrication approach was presented in [21], whereby the nanowire dimensions were defined by an accurate control of the silicon oxidation and etch. The authors transferred the as-fabricated nanowires onto a different substrate in order to arrange them into parallel arrays, which makes this approach partly reminiscent of the bottom-up techniques explained previously.

Another approach was presented in [22], which uses epitaxial Si and Ge layers on a bulk substrate. A thin epitaxial Si layer was sandwiched between Si_3N_4 and SiGe layers. Then, the Si_3N_4 and SiGe were selectively etched, leading to a partial etch of the sandwiched Si layer. The remaining edges of the Si layer were thinned out and lead to 10 nm nanowire diameter.

Using standard photolithography techniques, it could be demonstrated that 3-dimensional vertical stacks of nanowires can be achieved. A possible method was presented in [3, 4], which is based on the alternation of etching and passivation steps in a similar way to the *deep reactive ion etching (DRIE)* technique. This method yields scalloping edges, that can be thinned out through self-limited oxidation and controlled wet etch, resulting in vertical stacks of suspended nanowires. A fully different technique [5] uses alternating epitaxial Si and Ge layers; then, a selective etching of the Ge layers releases the thin suspended Si layers, which can be transformed into suspended Si nanowire stacks by accurately controlling their lateral etch.

2.1.2.2 Miscellaneous Mask-Based Techniques

Instead of using standard lithography and thinning out the devices by means of well controlled oxidation and selective etching, an alternative approach is to use electron-

beam lithography [23] that offers a higher resolution below 20 nm, and then eventually further reduce the nanowire diameter by stress-limited oxidation [24].

A higher resolution can be achieved by using *extreme ultraviolet interference lithography* (EUV-IL) [2]. Metallic nanowires with the width of 8–70 nm and a pitch of 50–100 nm could be achieved with this technique. However, this approach needs a highly sophisticated setup in order to provide the required EUV wave length, which is not available in state-of-the-art semiconductor fabrication lines. And it has not been proven so far how this technique may be used in order to fabricate semiconducting nanowires.

The stencil lithography is another approach, which is inherently different from the previous ones, but it shares the same feature of using a mask while avoiding the classical paradigm of CMOS processing, which consists in patterning a photoresist through the mask and then patterning the active layer through the patterned photoresist. The stencil approach [25] is based on the definition of a mask that is fully open at the patterned locations. The mask is subsequently clamped onto the substrate, and the material to be deposited is evaporated or sputtered through the mask openings onto the substrate. Nanowires with a width of 70 nm could be achieved this way. Even though only metallic nanowires have been demonstrated, the technique can be extended to semiconducting nanowires as well.

2.1.2.3 Spacer Techniques

The spacer technique is based on the idea of transforming thin lateral dimensions, in the range of 10–100 nm, into vertical dimension by means of anisotropic etch of the deposited materials. In [26], spacers with a thickness of 40 nm were demonstrated with a line-width roughness of 4 nm and a low variation across the wafer.

In [27], spacers were defined by means of *low pressure chemical vapor deposition* (LPCVD), then their number was duplicated by using the spacers themselves as sacrificial layers for the following spacer set. This technique, the *iterative spacer technique* (IST), yields silicon structures with sub-10 nm width and a narrower half-pitch than the photolithography limit.

In [28], the *multi-spacer patterning technique* (MSPT) was developed as in the previous approach, by iterating single spacer definition steps. The spacers were reminiscent to nanowires with a thickness down to 35 nm. The multi-spacer array was not used as a nanomold to define the nanowires, but it was rather used as the actual nanowire layer.

2.1.2.4 Nanomold-Based Techniques

Alternative techniques use the *nanoimprint lithography* (NIL), which is based on a mold with nanoscale features [29] that is pressed onto a resist-covered substrate in order to pattern it. The substrate surface is scanned by the nanomold in a stepper fashion. The as-patterned polymer resist is processed in a similar way to

photolithographically patterned photoresist films. The advantage of this technique is its ability to use a single densely patterned nanomold to pattern a large number of wafers. The obtained density of features on the substrate depends on the density of features in the nanomold, i.e., it mainly depend on the technology used to fabricate the nanomold.

A related technique to NIL, called the *superlattice nanowire pattern transfer technique (SNAP)*, was presented in [30], in which the nanowires are directly defined on the mold; then, they are transferred onto the polymer resist. Nanowires with a pitch of 34 nm could be achieved using the SNAP technique. The superlattice was fabricated by defining 300 successive epitaxial GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers on a GaAs wafer. Then, the wafer was cleaved, and the GaAs layers were selectively etched, so that the edge of each layer became an initial nanowire template. Then, a metal was deposited onto the exposed $\text{Al}_x\text{Ga}_{1-x}\text{As}$ ridges during a self-aligned shadow mask step. The self-aligned metal nanowires at the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ planes were subsequently transferred with the SNAP technique.

The spacer technique was used in an iterative way in [31] in order to define a nanomold yielding sub-10 nm nanowires with a 20-nm pitch. The process, *planar edge defined alternate layer (PEDAL)*, uses standard photolithography to define a sacrificial layer for the first spacer, then by iterating the spacer technique, a layer of dense spacers was defined. A shadow-mask deposited metal at the partially released spacer ridges formed thin nanowires, which were subsequently transferred onto the functional substrate. Since the spacer technique was used to define the nanomold and not the nanowires directly, this process is closer in nature to the nanomold-based techniques than to the spacer techniques.

2.1.2.5 Opportunities and Challenges of Top-Down Approaches

Top-down approaches are attractive because of their relatively easier required methods. The standard photolithography and spacer techniques can be integrated in a straightforward way into a CMOS process, whereas miscellaneous mask-based techniques may be more expensive and slower than the desired level for large production, and the maskless approaches may require the hybridization of the process with the non-conventional steps.

A promising opportunity that is offered by the spacer and nanomold-based techniques is the definition of devices with a sub-photolithographic pitch. In contrast to standard photolithography techniques, whose pitch is ultimately defined by the lithography limit, using spacer- and nanomold-based techniques represents an elegant way to circumvent the photolithographic limitations, and has a potential application field with regular architectures such as crossbar circuits as explained in Sect. 1.4.4.

The alignment of different processing steps is straightforward with standard lithography and miscellaneous mask-based techniques; while the spacer techniques are self-aligned. Nevertheless, whenever a nanomold-based step is

introduced, the alignment becomes a very challenging issue, making these techniques more likely to be used at the early processing stages.

A general drawback of all these bottom-up techniques is that the obtained semiconducting nanowires are undifferentiated, meaning that the doping profile along the nanowires is generally the same and cannot be modified at later process stages after the nanowires are defined. In order to uniquely address every nanowire, it is highly desirable to associate a different doping profile to every nanowire in order to uniquely address them.

Another challenge that is specific to the nanomold-based technique is the metallic nature of the most demonstrated nanowires. However, in order to fabricate the access devices to the nanowires, it is required to have semiconducting nanowires that can be field-effect-controlled. Fortunately, there are still many opportunities promising the fabrication with semiconducting nanowires with these techniques as well.

2.2 Crossbar Technologies

In this part of the work, the goal is to consider technologies that enable the fabrication of nanowire crossbar circuits. Even though the nanowire fabrication techniques, surveyed previously, demonstrated their ability to yield layers of parallel nanowires, only a few of them were successfully used to demonstrate the feasibility of arrays of parallel nanowires in a crossbar fashion. In the following, demonstrated fabrication techniques for nanowire crossbars are surveyed, then potential crossbar switch technologies are explored.

2.2.1 *Fluid-Directed Assembly*

Nanowires fabricated with bottom-up processes have the property of generally being grown on a different substrate from the functional one. Consequently, they need to be dispersed into a solution and transferred onto the substrate to be functionalized. The iteration of the transfer operations with different directions may lead to a crossbar structure. In [19], layers of parallel nanowires were obtained by passing suspended nanowires in an ethanol solution through a fluidic channel structure formed between a PDMS mold and the flat substrate. The obtained results show a good alignment of the nanowires, which depends on the channel dimensions defined in the mold and the flow rate and duration. By patterning the substrate with NH_2 -terminated regions, the alignment and density of nanowires could be improved. The second layer was obtained by using a crossed flow with respect to the direction of the first layer. The adhesion of the first nanowire layer to the substrate was demonstrated to be sufficiently strong that the

sequential flow step did not affect the preceding one. The obtained crossbar structure shows a separation between the nanowires of about 400 nm.

2.2.2 *Electric-Field-Assisted Assembly*

Nanowires fabricated in a bottom-up process and suspended in a solution can be assembled in parallel layers by applying an electric field that directs their adhesion to the substrate while a flow of the suspended nanowires is applied to the substrate. In [32] this technique was applied on gold nanowires in order to align them parallel to the applied electric field. The alignment was explained by the forces resulting from the polarization of the nanowire in the electric field. The approach was demonstrated in [33] to be feasible for doped semiconducting nanowires as well. The iteration of the same technique with two orthogonal directions of the electric field yields crossing nanowires in a crossbar fashion. However, the scalability of this method was evaluated in [19] to be limited by the electrostatic interference between nearby electrodes, and the requirement for an extensive lithography to fabricate the electrode for assembly of multiple nanowire arrays.

2.2.3 *Nanomold-Based Nanowire Crossbars*

Nanoimprint lithography was used in [34] in order to define two orthogonal layers of metallic nanowires. The nanomold was fabricated by electron-beam lithography and *reactive ion etching* (RIE) of a SiO₂-covered silicon substrate. The mold was then pressed onto a spin-coated *polymethylmethacrylate* (PMMA) on an oxidized Si substrate. After the system was heated, the mold was released resulting in a patterning of the PMMA, which was subsequently used as a lift-off mask to pattern a layer of parallel Ti/Pt nanowires. A layer of molecular switches, [2] rotaxane, was deposited over the entire substrate using the *Langmuir–Blodgett* (LB) method [35], in order to prepare the placement of the molecular switches at the crosspoints. Then, the fabrication of the top nanowire layer started with a thin Ti layer, which was very reactive with the top functional group of the molecules, and avoided the further penetration of the metal atom into the molecules. Then, a perpendicular top Ti/Pt nanowire layer was patterned in a similar way as explained for the low nanowire layer. The obtained functionalized crossbar had a crosspoint area of about $40 \times 40 \text{ nm}^2$. The same approach was improved in [36] yielding a nanowire width of 30 nm and a pitch of 60 nm in a 1 kbit memory, which is equivalent to a crosspoint density of 28 Gbit/cm^2 .

High-density crossbars were also demonstrated with the SNAP technique that was explained in Sect. 2.1.2 [37]. The fabricated nanowires were not only metallic but also silicon-based, with a width varying between 18 and 20 nm and a pitch between 30 and 60 nm. The iteration of the SNAP process was shown to be a flexible way to fabricate nanowire crossbars with densities up to 10^{11} cm^{-2} [30].

Such crossbars were functionalized with [2]rotaxanes and demonstrated for the first time 160-kbit molecular memories with a density of 10^{11} bit/cm² [38].

2.2.4 Crossbar Switches

While the scaling of the fabricated features below the photolithographic limit by applying the previously explained nanowire crossbar fabrication techniques has been successfully demonstrated, the interest in fabricating molecular devices, in which ultimately a small number of molecules is electrically connected to the electrodes, has continuously increased. The reason behind such an ambition, is not only the perpetuation of scaling power consumption and area per electronic device, but also the ability to understand the electrical behaviour of single molecules and to assess the physics of the zero-dimensional device in contact with a three-dimensional semiconducting or metallic bulk. In the meantime, the ability of modeling and synthesizing molecules that are potentially interesting for molecular electronics has shown many advances.

Many tries have been carried out in the last decades to design molecules comprising a donor-(σ bridge)-acceptor, which would have an asymmetric behaviour, allowing the current to flow in a preferential direction. Hereby, the electrode metal has to be carefully chosen, since the molecule-electrode interface was shown to interfere with the rectifying behavior in some cases [40–42]. Another class of switching molecules is represented by bistable molecules, such as [2] rotaxanes, pseudorotaxanes and [2] catenanes. They consist of two mechanically interlocked, or threaded, components. The molecule has two stable states (Fig. 2.6) and can be switched between these two states when the appropriate bias voltage is applied [39, 43].

Other research groups focused on phase change materials as a switching material at the nanowire crosspoints. In [44], a Ge nanowire pn-junction diode grown as a vertical nanowire with sublithographic dimensions was used as a memory cell. The cell is initially reset (to a low conductance state 0); then, it can be set by applying a current as large as a few μ A. At this point, the partially amorphous phase (in the reset state) is programmed into the poly-crystalline phase (SET state). In the SET state, the cell works as a diode. The programming from the SET to the RESET states is performed by applying pulses of large bias voltage. The cell provides an isolation of $100\times$ between the forward and reverse bias in the SET state.

2.2.5 Comparison Between Crossbar Technologies

The main goal of the crossbar architecture is to organize nanowires into very dense arrays, with a pitch below the photolithographic pitch. The two crossbar approaches suggested for nanowires grown in a bottom-up process (i.e., fluid-directed and

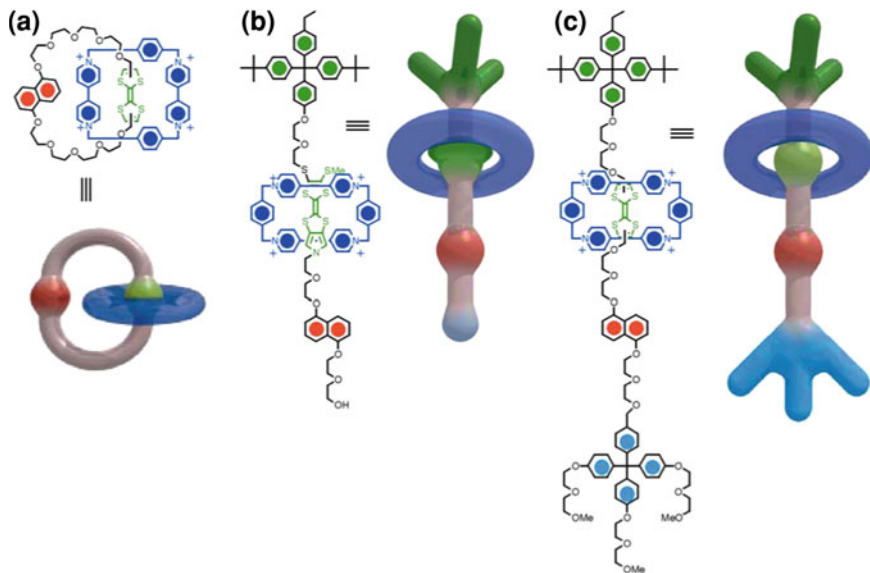


Fig. 2.6 Bistable mechanical molecular switches [39]: **a** [2] catenane, **b** pseudorotaxane and **c** [2] rotaxane

electric-field-assisted assembly) are not able to achieve this goal in general. The nanomold-based approach is the only existing technique that leverages the small dimensions of the nanowires and succeeds in arranging them into arrays with a sub-photolithographic pitch.

All these techniques showed promising results in terms of their ability to integrate nanowires into arrays, even though there is a certain discrepancy between the proposed approaches with respect to the nanowire dimensions and pitch. None of these techniques has targeted the exclusive utilization of CMOS processing steps in order to achieve crossbars with sub-photolithographic dimensions and pitches.

In the following sections, the actual work carried out with the fabrication facilities at EPFL is presented. The innovative goal of this work is to use a CMOS-compatible and cost-efficient technique, in order to arrange nanowires into arrays with a photolithography-*in* dependent pitch, while using only standard photolithography steps. The choices made with respect to the used equipments are justified in the following, before the fabrication steps and their optimization are explained.

2.3 Fabrication Facilities at EPFL

The CMI facilities were originally dedicated to the fabrication of *microelectromechanical systems (MEMS)* and to the optimization of their processing techniques. The available lithographic resolution of 0.8 μm is enough for

this purpose. MEMS processing is technologically different from microelectronics fabrication techniques in the sense that MEMS processing may require the deposition of some metallic films in early stages of the process flow, which is forbidden in microelectronics processing, since such wafers would contaminate for instance high-temperature furnaces.

However, the CMI facilities are kept in a class-100 environment. All possible sources of contamination are avoided, offering a possible environment for microelectronics applications. The high-temperature furnaces are for instance kept free of any metallic or organic contamination, by systematically separating those dedicated to poly-Si deposition or oxide growth from those dedicated to the annealing of wafers already contaminated and by applying the usual *RCA* wafer cleaning procedure.

The CMI facilities were chosen to fabricate nanowire crossbars for different reasons. On the one hand, the microelectronics-compatibility is guaranteed in the CMI. On the other hand, the lithographic limit does not represent any stopper for the suggested fabrication process, since the nanowire width and pitch are inherently independent on the lithographic limit, and they only depend on the deposition thickness and the etching properties. Moreover, the CMI offers a flexible use of the equipments, including the mask writer, and a possible customization of the process recipes upon requests and following discussions between the CMI users and staff.

2.3.1 Photolithography

2.3.1.1 Mask Writing

The input file required by the lithography system is a CIF or GDSII file that maps the design layout drawn with any layout editor, such as *L-Edit* by *Tanner EDA* or *Virtuoso* by *Cadence*. Other less conventional input formats are acceptable as well. The ladder editor was used in this work with GDSII output files. Even though *L-Edit* may offer a user-friendly interface and some easier-to-use functionalities, *Virtuoso* is already well established within standard design flows in either large industrial projects or smaller academic designs.

The masks were written using the laser lithography system *Heidelberg DWL200*. The tool uses a laser scanner and a Krypton (Kr) laser source for g- and h-line photoresist, and it is suitable for batch processing. A lithography resolution of 2 μm was sufficient in this work, because of the independency of the process critical dimensions on the lithographic resolution. Even though a direct writing on the wafers is possible with this equipment, only glass masks (5"×5" Cr-blanks) were written in this work, because this was more economical for a large number of processed wafers. Then, the masks were developed using *Süss DV 10*. The chromium and its native oxide were subsequently wet etched with the locally prepared solution $\text{HClO}_4 + \text{Ce}(\text{NH}_4)_2(\text{NO}_3)_6 + \text{H}_2\text{O}$ and the photoresist was stripped using the *Remover* by 1165 *Shipley Microposit*.

2.3.1.2 Photoresist

For non-lift-off steps, the *photoresist (PR)* that was used in this work is AZ92xx, which is a diluted version of AZ9260 by *MicroChemicals*. The thickness of 2 μm was suitable to all photolithographic steps in this work, other than lift-off. AZ92xx offers the advantage of a high profile with vertical steps. The silicon substrate was spin-coated with the photoresist using *Rite Track 88 Series*, where the wafers were previously primed in a *YES III HMDS* primer oven at 150°C. During this priming process, *hexamethyldisilazane (HMDS)*, $\text{C}_6\text{H}_{19}\text{Si}_2\text{N}$, was deposited on the wafer in order to enhance the adhesion of the photoresist to the silicon dioxide native film. The development of AZ92xx after exposure was carried out using the same *Rite Track 88 Series*.

Lift-off steps were performed with a stack of two positive photoresists: AZ1512 over *LOR*, both of them being supplied by *MicroChemicals*. For wafers with low profile topography (less than 0.7 μm), the thickness of *LOR* was set to 400 nm. The stack of both AZ1512 and *LOR* was spin-coated in two successive steps and developed after exposure with *EVG 150*. For wafers with a high profile topography (higher than 1.6 μm), a single thick layer of AZ92xx (4–5 μm) was used instead of AZ1512/*LOR*, which was spin-coated and developed with *Rite Track 88 Series*. Following the development of the resist, the lift-off procedure and the photoresist strip were carried out at the *Plade Solvent Photolithography* wet bench (Z1).

2.3.1.3 Mask Alignment and Exposure

The mask alignment to the wafer and the exposure could be performed on either *Süss MA150* or *Süss MA6/BA6*. In general, *Süss MA150* was used for first masks in a batch mode, and *Süss MA6/BA6* was used for mask alignment with individual wafers.

2.3.2 Etching

2.3.2.1 Anisotropic Plasma Etch

The cavities of both layers were defined inside silicon dioxide. The etching procedure requires the definition of vertical steps, which was performed with the plasma etcher *Alcatel AMS 200 DSE* using a fluorine chemistry (SF_6) with passivation gases for a better anisotropy. The definition of the multi-spacer had to fulfill the same requirements with respect to step anisotropy. Consequently, the oxide spacers were etched using the same equipment *Alcatel AMS 200 DSE*, while the poly-Si spacers were etched using a chlorine chemistry (Cl_2) with *STS Multiplex ICP* plasma etcher.

2.3.2.2 Isotropic Plasma Etch

The definition of the gate on a nanowire lying at the sacrificial layer needs to address the issue of a 3-dimensional (3D) gate following a step of about 0.5 μm height. The combination of anisotropic poly-Si etch to initially define the gate and a subsequent isotropic poly-Si etch in order to remove any unwanted residual poly-Si spacer at the sacrificial layer was necessary in this case, and was carried out using *Alcatel 601E* plasma etcher.

On the other hand, residual traces of photoresist needed to be completely stripped after the photoresist development, when the subsequent etch procedure is wet. This is known as a *descum* process, and the need for it is explained by the softness of the wet etching compared to the plasma etching, which may not be aggressive enough to remove the residual photoresist after development. An oxygen plasma etcher, *Oxford PRS900*, was utilized in order to isotropically etch the photoresist.

2.3.2.3 Wet Etch

In order to release the crossbar, the silicon dioxide between the two nanowire layers and in the sacrificial layer was wet-etched using a 7:1 *buffered HF (BHF)* solution in either *Coillard Etching (Z6)* or *Plade Oxide (Z2)* wet bench.

2.3.2.4 Chemical Mechanical Planarization (CMP)

In order to remove all residual films on the wafer back side, *Steag Mecapol E 460* was used to polish the back side in a fast and straightforward way. Thereby, the front side was covered by a thick photoresist for protection, because the slurry used in CMP has nanometer scale SiO_2 particles that may stick at the wafer surface. It is therefore recommended to clean the wafer in a BHF bath after CMP operations.

2.3.3 Thin Films

The *Centrotherm* furnaces were used for poly-Si LPCVD (tube 1-1), Si_3N_4 LPCVD (tube 1-2), wet oxide growth (tube 2-2), gate oxide growth (tube 2-3), LTO LPCVD (tube 3-1), LTO and poly-Si densification (tube 2-1), Si doping with POCl_3 (tube 1-4), dopant diffusion (tube 2-4), and Cr/Ni annealing (tube 3-4).

The evaporation of the contact metal (Cr and $\text{Ni}_{0.8}\text{Cr}_{0.2}$) was performed with the *Alcatel EVA600* evaporator. The equipment has *electron-beam (e-beam)* and thermal sources. For the present process flow, only e-beam sources were used. During evaporation, the vacuum level can be inside the evaporation chamber as

low as 5×10^{-7} mbar. Such a level is lower than the obtained level during metal sputtering, making the evaporation a more attractive solution. The distance between the source and the wafer is around 0.5 m, which is lower than in other evaporation equipments. The disadvantage of a low distance is the possible anisotropy of the deposited metal film, that may deteriorated the quality of the lift-off process. Since the metal film was thin (around 50–60 nm), the lift-off process could be perfectly performed using *Alcatel EVA600*.

2.3.4 Wafer Cleaning

Following the different photolithography steps, the resist was stripped using the *Remover 1165* by *Shipley Microposit*. Some plasma etching steps, namely the SiO_2 etch at 0°C with *Alcatel AMS 200 DSE*, harden the photoresist, which cannot be attacked by the *Remover 1165* anymore. In this case, two successive steps of plasma oxygen etch (*Oxford PRS900*) alternated by a wet etch with the *Remover1165* are performed.

The use of furnaces for poly-Si, Si_3N_4 and *low temperature oxide (LTO)* LPCVD necessitates a decontamination of the wafers from all organic or metallic residues. The usual and well established procedure is the RCA cleaning. It is performed at the *Plade RCA (Z3)* and consists in 3 baths. The first bath (RCA1) is $\text{H}_2\text{O} : \text{NH}_4\text{OH} : \text{H}_2\text{O}_2$ 5:1:1, used to remove organic residues; the second bath is $\text{H}_2\text{O} : \text{HF}10 : 1$, used to remove the native SiO_2 ; and the third bath (RCA2) is $\text{H}_2\text{O} : \text{HCl} : \text{H}_2\text{O}_2$ 6:1:1, used to remove the residual metal. The cleaning procedure can be transformed if the wafers have sensitive SiO_2 films or spacers, by replacing RCA1 by Piranha cleaning $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ performed at the the *UltraFab* wet bench, and skipping the HF cleaning.

2.3.5 Process Control

Besides the continuous control of the wafer with optical microscopy (*Nikon Optiphot 200/Nikon Optiphot 150*) as well as *scanning electron-microscopy (SEM)* with *Zeiss LEO1550*, a regular control of the film thickness was conducted during the front-end phases, and particularly during the definition of the multi-spacer in order to optimize the deposition and the etching times. The measurements were done with the spectro-reflectometer *Nanospec AFT-6100*. Its resolution of about 10 nm was a limiting factor in certain cases. However, it was more convenient to use the *Nanospec AFT-6100* to control film thicknesses, rather than cleaving the wafer and observing its cross-section with the SEM. An optical profiler was also utilized occasionally (*Veeco Wyko NT1100*).

Once the multi-spacer was defined, cross-sections were performed using the *FEI Nova 600 NanoLab*. The equipment has a dual beam: a SEM and a *focused ion beam (FIB)*. The FIB was used to cleave specific structures without damaging the rest of the wafer, while the SEM was used in imaging.

The electrical measurements represented an additional way to control the processed wafers in the back-end phases. A *Süss PM8* manual prober station was available inside the CMI cleanroom for device characterization. However, these measurements were performed under (artificial) ambient light.

2.4 Process Flow

The goal of this part of the work is to define a process flow for a nanowire crossbar framework using standard CMOS processing steps and the available micrometer scale lithography resolution. The proposed approach is based on the spacer patterning technique presented in [Sect. 2.1.2](#). The iteration of the spacer steps has been shown to be an attractive and cost-efficient way to fabricate arrays of parallel stripes used for the definition of nanomolds [31] or directly as nanowire arrays [28].

The approach presented in this part of the work is based on the idea of MSPT demonstrated in [28] for a single nanowire layer. In this part of the work, the efforts are concentrated on related challenges: first, the demonstration of the ability of this technology to yield a crossbar structure; then the assessment of the limits of this technology in terms of nanowire dimensions and pitch; and finally, the characterization of access devices operating as single poly-Si nanowire field effect transistors (poly-SiNWFET).

The main idea of the process is the iterative definition of thin spacers with alternating semiconducting and insulating materials, which result in semiconducting and insulating nanowires. The structures are defined inside a 1 μm high wet SiO_2 layer over the Si substrate (Fig. 2.7a). This SiO_2 layer has two functions: on the one hand, it insures the isolation between the devices; on the other hand it is used to define a 0.5 μm high sacrificial layer on which the multi-spacer is defined.

Then, a thin conformal layer of poly-Si with a thickness ranging from 40 to 90 nm is deposited by LPCVD in the *Centrotherm* tube 1-1 (Fig. 2.7b). During the LPCVD process, silane (SiH_4) flows into the chamber and silicon is deposited onto the substrate. The type of deposited silicon (amorphous or poly-crystalline) depends on the chamber temperature and pressure [45–47]. The deposition has been specifically optimized for the CMI facilities [48]. At the deposition temperature of 600°C, the LPCVD process yields poly-crystalline silicon. Thereafter, this layer is etched with the RIE etchant *STS Multiplex ICP* using a Cl_2 plasma, in order to remove the horizontal layer while keeping the sidewall as a spacer (Fig. 2.7c). As the densification of deposited silicon improves the crystalline structure [49], the poly-Si spacer is densified at 700°C for 1 hour under N_2 flow in the *Centrotherm* tube 2-1.

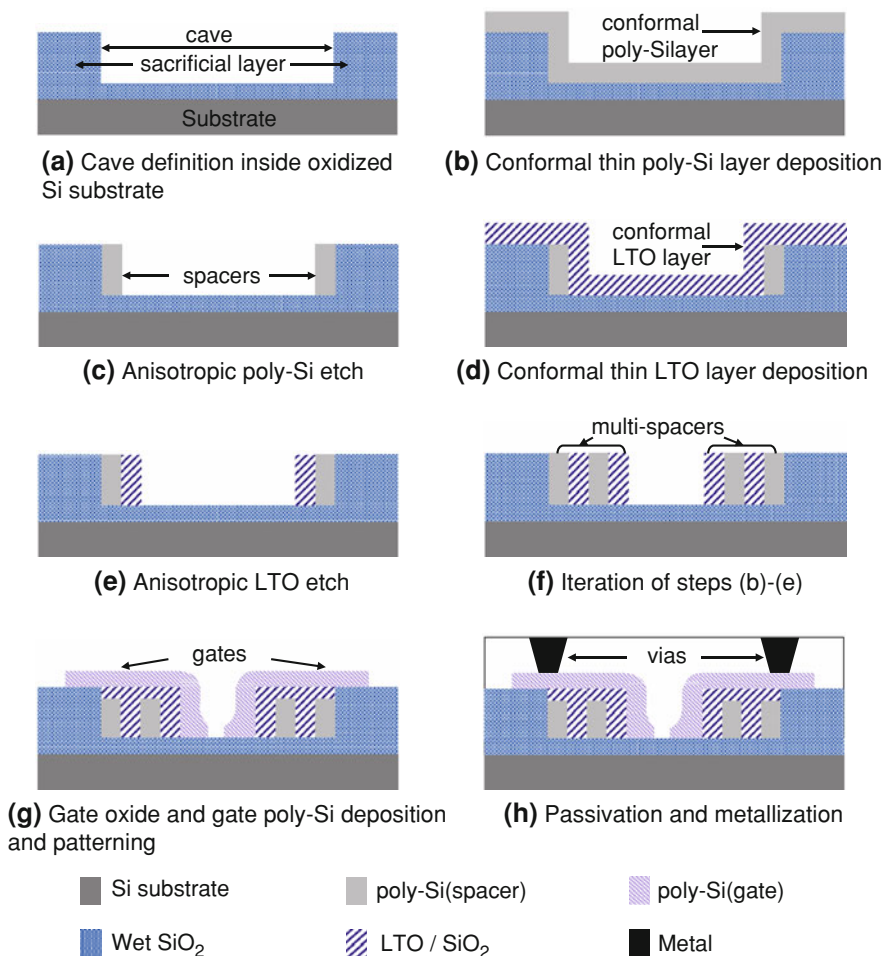


Fig. 2.7 MSPT process steps

Then, a conformal insulating layer is deposited as a 40–80 nm thin LTO layer obtained by LPCVD in the *Centrotherm* tube 3-1 following the reaction of SiH₄ with O₂ at 425°C (Fig. 2.7d). The quality of the LTO can be improved through densification [50]. Thus, the deposited LTO is densified at 700°C for 45 minutes under N₂ flow. Then it is etched in the RIE etchant *Alcatel AMS 200 DSE* using C₄F₈ plasma in order to remove the horizontal layer and just keep the vertical spacer (Fig. 2.7e). Alternatively, instead of depositing and etching the LTO, the previously defined poly-Si spacer can be partially oxidized in the *Centrotherm* tube 2-1 in order to directly form the following insulating spacer.

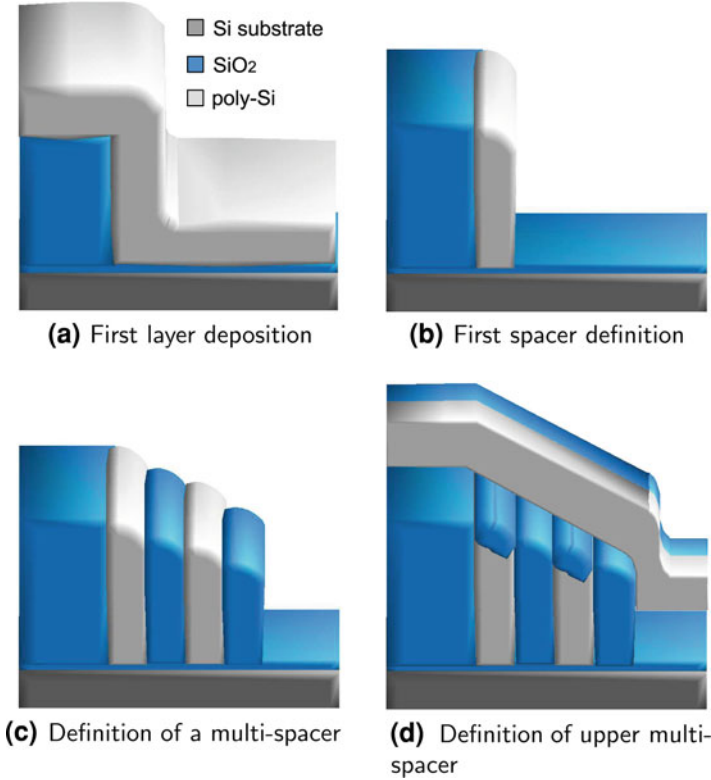


Fig. 2.8 Main process steps of crossbars with the spacer technique

These two operations (poly-Si and insulating spacer definition) are performed one to six times in order to obtain a multi-spacer with alternating poly-Si and SiO_2 nanowires (Fig. 2.7f). Then, the batch is split into two parts: some of the wafers are dedicated to the definition of a second perpendicular layer of nanowires, some others are processed further with the gate stack and the back-end steps and are dedicated to perform electrical measurements.

In order to address the issue of characterizing a single access device (poly-SiNWFET), a single nanowire layer is used, on top of which a poly-Si gate stack is defined with an oxide thickness of 20 nm, obtained by dry oxidation of the poly-SiNW, and different gate lengths (Fig. 2.7g). The drain and source regions of the undoped poly-SiNW are defined by the e-beam evaporation and lift-off of 10 nm Cr and 50 nm nichrome ($\text{Ni}_{0.8}\text{Cr}_{0.2}$) with *Alcatel EVA 600* (Fig. 2.7h). The Cr enhanced the adhesion and resistance of Ni to oxidation during the two-step annealing (including 5 minutes at 200°C , then 5 minutes at 400°C [51]) performed in the *Centrotherm* tube 3-4. Using Cr/ $\text{Ni}_{0.8}\text{Cr}_{0.2}$ is a simple way to contact undoped nanowires, since Ni is a mid-gap metal. If the nanowires are doped, then it is possible to use aluminum as contact metal, which is then

evaporated and patterned after a passivation layer is deposited and vias are opened, as depicted in Fig. 2.7h.

In order to address the issue of realizing a crossbar framework, the bottom multi-spacer is fabricated as explained previously in Fig. 2.7a–f, then a 20-nm dry oxide layer is grown as an insulator between the top and bottom nanowire layers. The top sacrificial layer is defined with LTO perpendicular to the direction of the bottom sacrificial layer. Then a poly-Si spacer is defined at the edge of the top sacrificial layer in a similar way to the bottom poly-Si spacers. Thereafter, the separation dry oxide and both sacrificial layers are removed in a BHF solution in order to visualize the crossing poly-Si spacers realizing a small poly-Si nanowire crossbar. The main process steps of a crossbar are depicted in Fig. 2.8. In this figure, the difference in height between successive spacers is shown; which effect will be explained in the following sections.

A typical runcard of the process for a single layer of nanowires is detailed in Table 2.1. When a double layer is targeted by the process (i.e., a crossbar), then additional photolithography and spacer definition steps are included between steps 4 and 5 in Table 2.1. These extra steps correspond to the upper sacrificial layer. In this typical runcard, the thickness of poly-Si and LTO layers are just given as examples. These values can be varied within the processed wafers. This runcard shows the steps for Cr/Ni_{0.8}Cr_{0.2} contacts defined with lift-off. Some wafers were contacted with Al through vias. The annealing can be done either after every spacer definition as explained above, or it can be done once all spacers are defined, as shown in Table 2.1.

2.5 Process Optimization

The development of a new technology necessitates the optimization of a large number of parameters, even though the abilities of the equipments and the goal set to use CMOS compatible steps put some boundary conditions that reduce the range of fabrication parameters to be explored. In this section, some process optimization aspects are highlighted and the adopted solutions are explained.

2.5.1 Etch of Sacrificial Layers

The process has two perpendicular sacrificial layers, corresponding to each one of the crossing nanowire layers. The first sacrificial layer is etched in a wet oxide at 0°C with a SF₆ plasma, using *Alcatel AMS 200 DSE*. It is required that the etch is highly anisotropic in order to obtain a vertical step. The shape of the step defines the shape of the conformal poly-Si thin film. A vertical step would result in a removal of only lateral parts of the poly-Si film, leaving just the narrow vertical spacer. In reality, the step has a certain obtuse angle with the horizontal line, thus

Table 2.1 Typical run card for a single nanowire array

Step	Process	Equipment	Recipe
1	<i>Wafer oxidation</i>		
1.1	RCA cleaning	Z3/RCA wetbench	Standard RCA1+HF+RCA2
1.2	Wet oxidation	Z3/Centrotherm 2-2	1 μm
1.3	Inspection	Z3/Nanospec AFT-6100	
2	<i>Photolithography: sacrificial layer mask</i>		
2.1	Wafer priming	Z1/YES III, HMDS primer oven	~ 20 min
2.2	PR coating	Z1/Rite Track 88 series	2 μm of AZ92xx
2.3	PR exposure	Z1/MA/BA6	9 s, hard contact
2.4	PR development	Z1/Rite Track 88 series	2 μm of AZ92xx
3	<i>Definition of sacrificial layer</i>		
3.1	RIE oxide etch	Z2/AMS 200 DSE	SiO ₂ _PR_5:1 2'30"
3.2	O ₂ PR strip	Z2/Oxford PRS900	1 h
3.3	PR wet strip	Z2/WB PR strip	Standard 2 \times 5 min
3.4	O ₂ PR strip	Z2/Oxford PRS900	10 min
3.5	Inspection	Z3/Nanospec AFT-6100	
4	<i>Definition of the multi-spacer</i>		
4.1	Piranha cleaning	Z2/WB Piranha	Standard 2 \times 5 min
4.2	RCA2 cleaning	Z3/WB RCA	Standard 15 min
4.3	Poly-Si LPCVD	Z3/Centrotherm 1-1	80 nm
4.4	Inspection	Z3/Nanospec AFT-6100	
4.5	Poly-Si etch	Z2/STS Multiplex ICP	Sub_Si 0'19"
4.6	Inspection	Z3/Nanospec AFT-6100	
4.7	Piranha cleaning	Z2/WB Piranha	Standard 2 \times 5 min
4.8	RCA2 cleaning	Z3/WB RCA	
4.9	LTO LPCVD	Z3/Centrotherm 3-1	90 nm
4.10	Inspection	Z3/Nanospec AFT-6100	
4.11	Oxide etch	Z2/AMS 200 DSE	SiO ₂ _PR_5:1 0'27"
4.12	Inspection	Z3/Nanospec AFT-6100	
	Iteration of steps 4.1-4.12 $n \times$		
4.(12n + 1)	Densification	Z3/Centrotherm 2-1	45' at 700°C under N ₂ flow
4.(12n + 2)	Cross-section	Z8/FEI Nova 600 NanoLab	FIB cross-section and SEM inspection
5	<i>Photolithography: cave edge mask</i>		
5.1	Wafer priming	Z1/YES III, HMDS primer oven	~ 20 min

(continued)

Table 2.1 (continued)

Step	Process	Equipment	Recipe
5.2	PR coating	Z1/Rite Track 88 series	2 μ m of AZ92xx
5.3	PR exposure	Z1/MA/BA6	9 s, hard contact
5.4	PR development	Z1/Rite Track 88 series	2 μ m of AZ92xx
6	<i>Cave edge etch</i>		
6.1	Descum	Z2/Oxford PRS900	Plasma O ₂ for 0'30"
6.2	Wet oxide etch	Z2/WB oxide etch	BHF 30"
6.3	Native oxide strip	Z2/Alcatel 601E	SiO ₂ _Soft 0'10"
6.4	Poly-Si strip	Z2/Alcatel 601E	Si_Iso_Slow 2'00"
6.5	PR wet strip	Z2/WB PR strip	Standard 2 \times 5 min
6.6	O ₂ PR strip	Z2/Oxford PRS900	30 min
6.7	Inspection	Z3/Nanospec AFT-6100	
7	<i>Gate stack deposition</i>		
7.1	Native oxide strip	Z6/WB Oxide etch	BHF 30"
7.2	Piranha cleaning	Z2/WB Piranha	Standard 2 \times 5 min
7.3	RCA2 cleaning	Z3/WB RCA	Standard 15 min
7.4	Dry oxidation	Z3/Centrotherm 2-3	20 nm gate oxide
7.5	Poly LPCVD	Z3/Centrotherm 1-1	0.5 μ m deposition of gate poly-Si
8	<i>Photolithography: gate mask</i>		
8.1	Wafer priming	Z1/YES III, HMDS primer oven	~20 min
8.2	PR coating	Z1/Rite Track 88 series	2 μ m of AZ92xx
8.3	PR exposure	Z1/MA/BA6	9 s, hard contact
8.4	PR development	Z1/Rite Track 88 series	2 μ m of AZ92xx
9	<i>Gate patterning</i>		
9.1	Anisotropic poly-Si etch	Z2/STS Multiplex ICP	Sub_Si 1'20"
9.2	Isotropic poly-Si etch	Z2/Alcatel 601E	Si_Iso_Slow 0'20"
9.3	O ₂ PR strip	Z2/Oxford PRS900	1 h
9.4	PR wet strip	Z2/WB PR strip	Standard 2 \times 5 min
9.5	O ₂ PR strip	Z2/Oxford PRS900	10 min
10	<i>Photolithography: metallization mask</i>		
10.1	Dehydration	Z6/Memmeret dry box	20 min at 150°C
10.2	PR coating	Z6/EVG150	400 nm of AZ1512 on LOR (standard recipe 5_5)
10.3	PR exposure	Z6/MA/BA6	1.5 s
10.4	PR development	Z6/EVG150	400 nm of AZ1512 on LOR (standard recipe 5_5)
11	<i>Metallization</i>		
11.1	Native oxide strip	Z6/WB Oxide etch	0'30"

(continued)

Table 2.1 (continued)

Step	Process	Equipment	Recipe
11.2	Metal evaporation	Z4/Alcatel EVA 600	10 nm Cr + 50 nm Ni _{0.8} Cr _{0.2}
12	<i>Lift-off</i>		
12.1	Lift-off	Z1/WB Photolitho	7 h
12.2	Sonication	Z1/WB Photolitho	5 min
12.3	PR strip	Z6/WB PR strip	Standard 2 × 5 min
13	<i>Thermal annealing</i>		
13.1	Annealing	Z3/Centrotherm 3-4	5' at 200°C + 5' at 400°C in N ₂ flow
14	<i>Back-side CMP</i>		
14.1	Wafer priming	Z1/YES III, HMDS primer oven	~20 min
14.2	Font-side PR coating	Z1/Rite Track 88 series	2 μm of AZ92xx
14.3	Back-side CMP	Z5/Steag Mecapol E 460	3 × 3' + SRD, slurry = Reclaim
14.4	PR strip	Z6/WB Resist strip	Standard 2 × 5 min

the conformal poly-film is partially removed in the vertical direction as well. In some cases, this can lead to a serious deformation of the poly-Si spacer shape, which is carried forwards to the next spacers as well.

The SF₆ etch process can be improved by adding a passivation gas (CH₄), which enhances the verticality of the step by passivating the areas as soon as they are etched. A comparison of the results with and without passivation gazes is demonstrated in Figs. 2.9 and 2.10 respectively with SEM of two structures processed differently.

2.5.2 Spacer Definition

The spacer etch procedures have to be anisotropic in order to keep the spacer shape as vertical as possible as explained above. This was solved for the oxide etch by using a SF₆ plasma etch including CH₄ passivation, in a similar way to the

Fig. 2.9 SEM of poly-Si spacer defined on anisotropically etched SiO₂ sacrificial layer (passivated SF₆ etch)

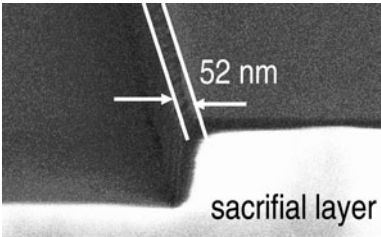


Fig. 2.10 Cross-section of poly-Si spacer defined on slightly isotropically etched SiO_2 sacrificial layer (bare SF_6 etch). Spacer thickness ~ 60 nm

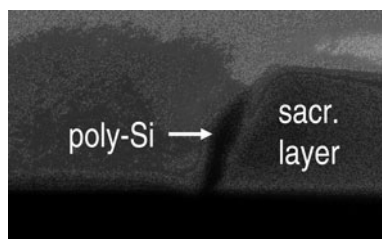
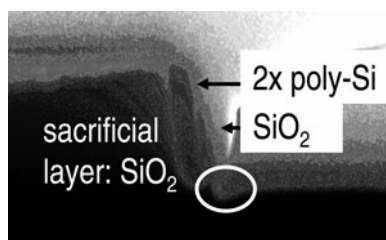


Fig. 2.11 Oxide spacer over-etch: first oxide spacer stripped, leaving 2 neighboring poly-Si spacers. Second oxide spacer over-etched, leading to etch of the cave (circle)



sacrificial layer etch. For the poly-Si etch, the used chlorine chemistry (with just Cl_2 plasma) was sufficient to insure the desired anisotropy.

An additional constraint on the spacer etch is the accuracy of etch time. As a matter of fact, an over-etch of any conformal layer (either in poly-Si or in LTO) reduces the thickness of its vertical part after the lateral part is fully consumed. In addition, the over-etch of a conformal layer attacks the uncovered layer underneath it, which is the SiO_2 sacrificial layer (Fig. 2.11). This is clearly more critical when the etched layer is LTO. Even the poly-Si layer over-etch may be of concern though, since the selectivity of the Si etchant to the SiO_2 etchant is worse than 1:20, which may result in up to 5 nm of loss of the sacrificial layer. The loss is cumulative over the whole multi-spacer definition, and becomes more visible with a larger number of spacers, resulting in an oblique multi-spacer, as demonstrated in Fig. 2.12. Even though such a shape may be processed further, it is not desirable to have an oblique gate on top of the nanowires because of possible induced stress.

On the other hand, an under-etch of the conformal layer results in the opposite effect. If a LTO is under etched, then more materials are deposited and left inside the cave of the sacrificial layer, resulting in turns in an oblique shape as well.

Fig. 2.12 Oxide and poly-Si spacers over-etch: all oxide spacers are stripped, poly-Si is over-etched. Then, cave is attacked resulting in diamond-shaped multi-spacer

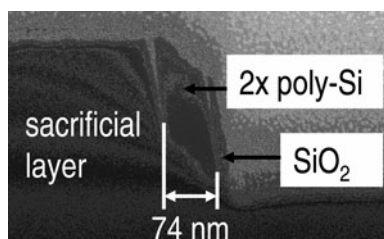


Fig. 2.13 Calibration of the poly-Si etch with Cl_2 chemistry. The offset is due to the etch of the native oxide

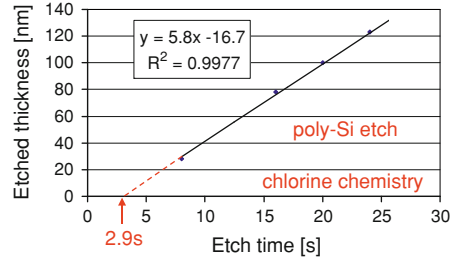
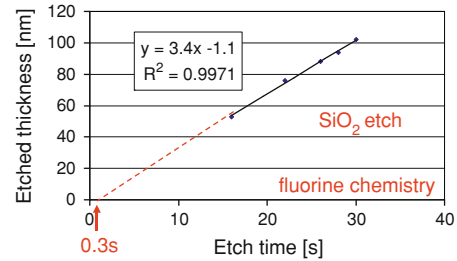


Fig. 2.14 Calibration of the SiO_2 etch with SF_6 chemistry. The etch rate is constant and there is almost no offset



The under-etch of the poly-Si conformal layer leaves some poly-Si grains inside the cave and may result in a short between the different poly-Si spacers.

In order to avoid both under- and over-etch of poly-Si and LTO, the etch rates are accurately calibrated with both fluorine and chlorine chemistries for LTO and poly-Si etch respectively. The etch procedures are calibrated by measuring the poly-Si and LTO layers before and after partial etching of thin poly-Si and densified LTO layers using the *Nanospec AFT-6100* and different etching times. The etching times are chosen such that the remaining film is thicker than the *Nanospec AFT-6100* measurement limit of 10 nm.

Figure 2.13 shows the calibration plot for the chlorine chemistry used to etch poly-Si. A linear curve with an offset of about 2.9 s is clearly seen in this plot. The offset is due to the fact that the Cl_2 plasma first physically attacks the native SiO_2 , before the poly-Si is attacked. On the contrary, Fig. 2.14, shows that the calibration plot for the fluorine chemistry used to etch LTO densified at 700°C for 45 min under N_2 flow is almost offset-free and linear with an etch rate of about 206 nm/min.

2.5.3 Gate Stack

Some samples were used in order to electrically characterize the access devices operating as poly-SiNW. In this case, a gate stack was defined on top of the poly-Si spacer following the step defined by the sacrificial layer with a height of

Table 2.2 Etch time for 3 calibration recipes. Anisotropic and isotropic etch are carried out with *STS Multiplex ICP/Sub_Si* and *Alcatel 601E/Si_Iso_Slow* respectively

Recipe	1	2	3
Anisotropic etch	1'20"	1'20"	1'20"
Isotropic etch	0'10"	0'30"	0'20"

0.4–0.5 μm . An anisotropic etch of the gate poly-Si would leave a poly-Si spacer at the sacrificial layer shorting the drain and source of the device. Thus, an additional isotropic gate poly-Si etch procedure was required in order to remove this parasitic spacer. The isotropic etch should just remove $\sim 0.4\mu\text{m}$ laterally from the gate edge. An over-etch may strip either the gate or the underlying poly-SiNW. An under-etch causes a short between drain and source. This combination of two types of etching being crucial for the device operation, several etch times were tried as summarized in Table 2.2. The impact of the double etch is illustrated with the SEM images in Fig. 2.15.

2.6 Device Characterization

The process is optimized according to the steps described above in order to carry out different types of investigation. First, a structural characterization was conducted in order to assess how small the nanowire pitch and how dense the nanowire crosspoints can be achieved. Then, an electrical characterization of single nanowires with drain, source and gate contacts was performed in order to assess the ability of a single poly-SiNWFET to act as an access transistor to the underlying nanowire.

2.6.1 Structural Characterization

In the following, the structural properties of arrays of parallel nanowires fabricated with the proposed technique are assessed. Figure 2.16 shows a SEM image of 3 double-spacers poly-Si/LTO. All the poly-SiNW have a uniform thickness of 54 nm, indicating that the NW thickness can be accurately controlled. Their height was about the height of the sacrificial layer, and decreased with increasing number of spacers, because of the increasing number of etching procedures. A NW length of hundreds of micrometers could be achieved, with no NW breakage. Besides the advantage of exclusively using standard CMOS steps, this technique has a high yield close to unity.

The insulating nanowires can be made either with LTO deposition or dry oxidation of the previously defined poly-Si nanowires. The second option was investigated by oxidizing about 40 nm of every poly-SiNW in a nanowire layer

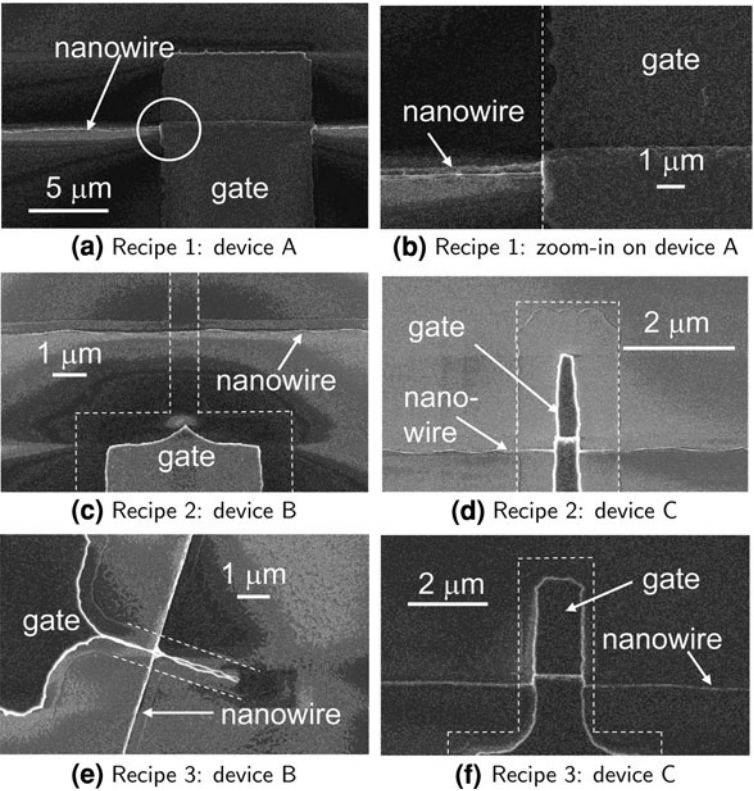
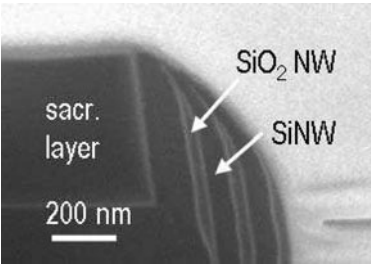


Fig. 2.15 Optimization of 3D gate etch. Dashed lines are the gate dimensions as defined by the photoresist (showed in order to guide the eyes). **a** Isotropic etch time is too short: gate edge just starts to be laterally etched. **b** Zoom-in on the circle in **a**: drawn gate edge is locally not etched. **c** Over-etch of the gate in shortest devices (1 μm). **d** Longer gates (2 μm) survive the lateral gate over-etch. **e** Shortest device (1 μm) are laterally just etched the required amount ~0.4 μm. **f** Longer gates (2 μm) suggest that the combination of anisotropic and isotropic etch is satisfactory

Fig. 2.16 SEM of a poly-Si/LTO 6×-spacer: poly-Si spacers have uniform thickness of ~54 nm



containing 6 poly-SiNW, yielding a theoretical dry oxide thickness about 90 nm. A SEM image of the cross-section of the obtained structure is illustrated in Fig. 2.17, showing an average width of the obtained poly-SiNW of about 60 nm. The surface roughness of the obtained structures is coarse because of the non-uniform oxidation rate of the poly-Si at the grain boundaries. Consequently, the deposition of LTO is found to be a better way to insulate the nanowires than the dry oxidation of poly-Si, even though it necessitates more processing steps.

The scalability of this technique was investigated by depositing thinner poly-Si layers (40 nm): Fig. 2.18 shows that the obtained poly-SiNW have a width of 20 nm. For the device in this SEM image, the multi-spacer was planarized using CMP after it was defined. This result demonstrated that it is possible to make the nanowires narrow by depositing less poly-Si. The obtained nanowire width is always less than the deposited film thickness, because of the etch procedure that attacks the vertical structures in a measurable way, but much less than it attacks the lateral structures.

The possible use of the MSPT for the fabrication of two perpendicular layers of crossing NW is illustrated in Fig. 2.19 with one poly-SiNW crossing 4 poly-SiNW underneath it. Here gain, the length of the nanowires in the crossbar could be made as large as desired without any noticeable nanowire breakage. The obtained crosspoint area is about $100 \times 100 \text{ nm}^2$, which is equivalent to a crosspoint density of 10^{10} cm^{-2} .

Fig. 2.17 SEM of poly-Si/dry SiO_2 12 \times -spacer: the spacers are repeatable with a large number of iterations

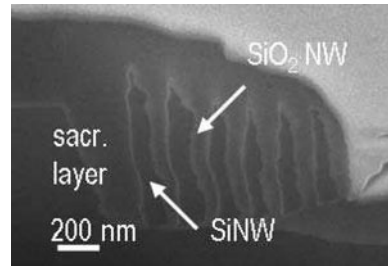


Fig. 2.18 SEM of an ultra thin multi-spacer: poly-SiNW thickness $\sim 40 \text{ nm}$

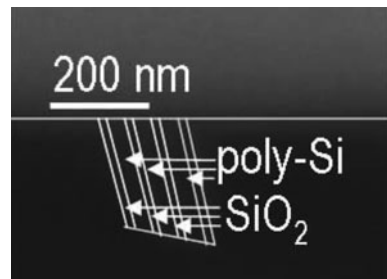


Fig. 2.19 SEM of a small 4×1 -crossbar. The upper layer is separated by 20 nm from the lower layer

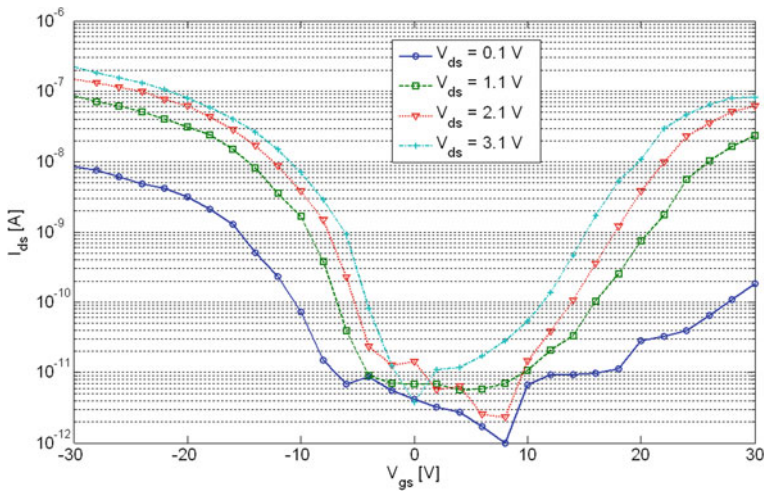
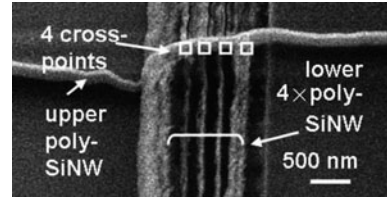


Fig. 2.20 $V_{gs} - I_{ds}$ curve of undoped poly-SiNWFET with a back gate and nickel silicide contacts

2.6.2 Electrical Characterization

The need to access the nanowires and control the current flow through them motivates for the definition of access transistors having a poly-Si spacer as a channel. Undoped poly-SiNWFET with a single poly-Si spacer as a channel are characterized. The $I_{ds} - V_{gs}$ curves for back-gated devices show an ambipolar behaviour, with a current conductance under either high positive or negative gate voltage (Fig. 2.20). The ambipolar behaviour is explained by two factors: the undoped poly-SiNWFET channel and the mid-gap drain and source nickel silicide metal, resulting in a Schottky barrier at the drain and source contacts whose thickness can be modulated using the electrical gate field (Fig. 2.21), making it more transparent for either electrons or holes. A similar behaviour in other SiNW technologies has already been reported and explained by the existence of a Schottky barrier at the drain and source contacts [52–54].

The I_{on}/I_{off} ratio was about 2×10^4 and 4×10^3 for the p- and n-branch respectively. The low $I_{on} = 0.2 \mu A$ and $0.1 \mu A$ for p- and n-branches respectively is explained by the low W/L ratio (the nanowire width $W = 67$ nm, back gate length

Fig. 2.21 Band diagram of ambipolar undoped poly-SiNW devices. *Left* positive V_{gs} makes Schottky barrier transparent for electrons. *Right* negative V_{gs} makes Schottky barrier transparent for holes

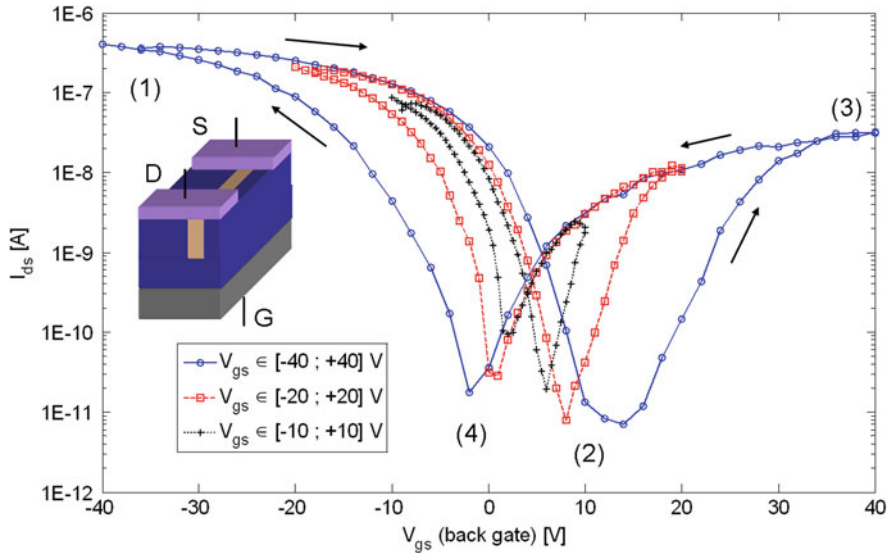
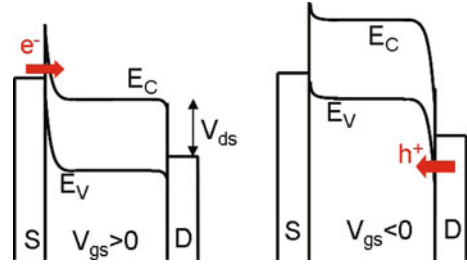


Fig. 2.22 Variation of hysteresis width of $I_{ds}-V_{gs}$ curve and I_{on}/I_{off} ratio of back-gated devices with V_{gs} range

$L = 20 \mu\text{m}$, gate oxide thickness $t_{ox} = 400 \text{ nm}$) and the low mobility in poly-Si. The Schottky barrier for holes may be slightly lower than for electrons, which explains the higher I_{on} -current in the p-branch. The curves were repeatable on the wafer scale and they do not represent a single device. The ability to control the devices in a FET fashion proves their possible use as access devices to the NW layer within a decoder. The ambipolarity is due to the intrinsic channel and the mid-gap contact metal that is electrostatically controlled by the gate field. By using implanted contact regions and metal contact, the unipolar behavior can be restored [53].

The ambipolarity of a single poly-SiNW is investigated for different sweep ranges of V_{gs} . The $I_{ds}-V_{gs}$ curve in Fig. 2.22 shows a hysteric behavior when V_{gs} is swept from $-V_{gs,max}$ to $+V_{gs,max}$ back and forth. By enlarging the V_{gs} sweep range from $V_{gs,max} = 10 \text{ V}$ to 40 V , the hysteresis became larger. Charge trapping

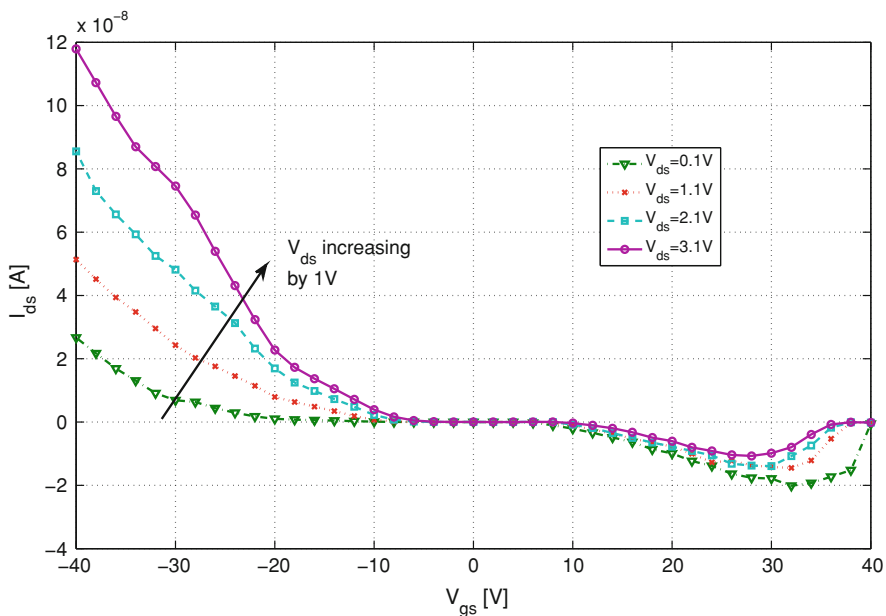


Fig. 2.23 $I_{ds}-V_{gs}$ curve of undoped poly-SiNWFET with top gate ($L_g = 4 \mu\text{m}$, $W_{NW} = 67 \text{ nm}$ and $t_{ox} = 0.450 \mu\text{m}$)

and detrapping can explain the hysteresis¹ in Fig. 2.22. From (1) to (2), trapped holes at the $\text{SiO}_2/\text{poly-Si}$ interface create positive fixed charges, and are detrapped with increasing V_{gs} . From (2) to (3), an electron channel is created. With the increasing electron density, more electrons are trapped at the $\text{SiO}_2/\text{poly-Si}$ interface, leading to a negative interface charge density. From (3) to (4), electrons are detrapped with the vanishing electron channel. Detrapping is a slower process than trapping, explaining the hysteresis (2)-(3)-(4). From (4) to (1), a hole channel is created and increases the trapping probability for holes. This is a faster process than detrapping holes; explaining again the hysteresis (4)-(1)-(2). The off-current at (2) is lower than the one at (4) because of the additional probability of having electrons trapped in SiO_2 besides the electrons trapped at the $\text{SiO}_2/\text{poly-Si}$ interface. By enlarging the sweep range (higher V_{gs}), more charge carriers are trapped. This shifts the threshold voltage in the n-branch (p-branch) to more positive (negative) values during the trapping phase. The detrapping is slow, thus all 3 curves almost coincide during the detrapping phases.

Devices with a top-gate showed a unipolar behaviour with a p-type polarity despite the intrinsic channel (Fig. 2.23). The unipolar behaviour is explained by the absence of an electrostatic control of the gate on the drain/source-to-channel

¹ This conclusion is qualitatively confirmed with Silvaco device simulations performed by Dr. Nikolaos Archontas, Democritus University of Thrace, Greece

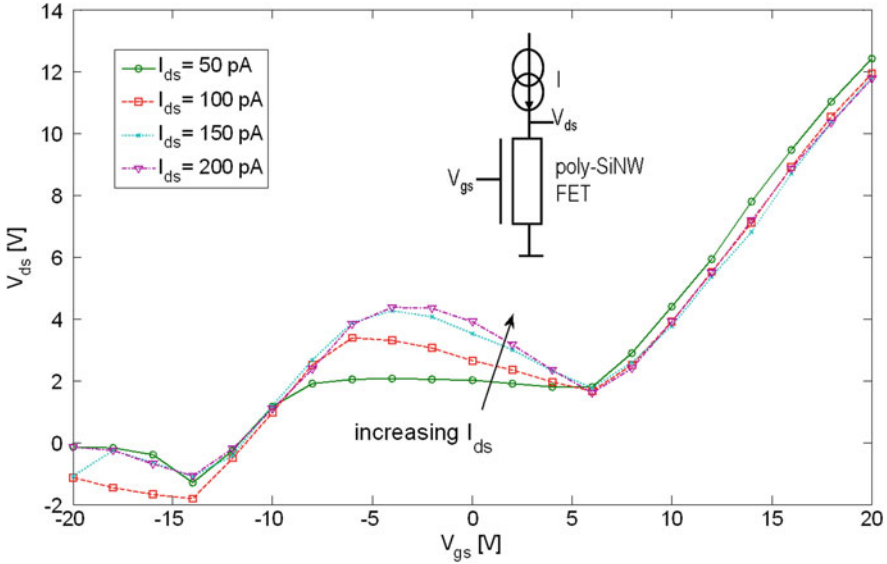


Fig. 2.24 V_{ds} versus V_{gs} curve of undoped poly-SiNWFET for fixed I_{ds} with a back gate and nickel silicide contacts

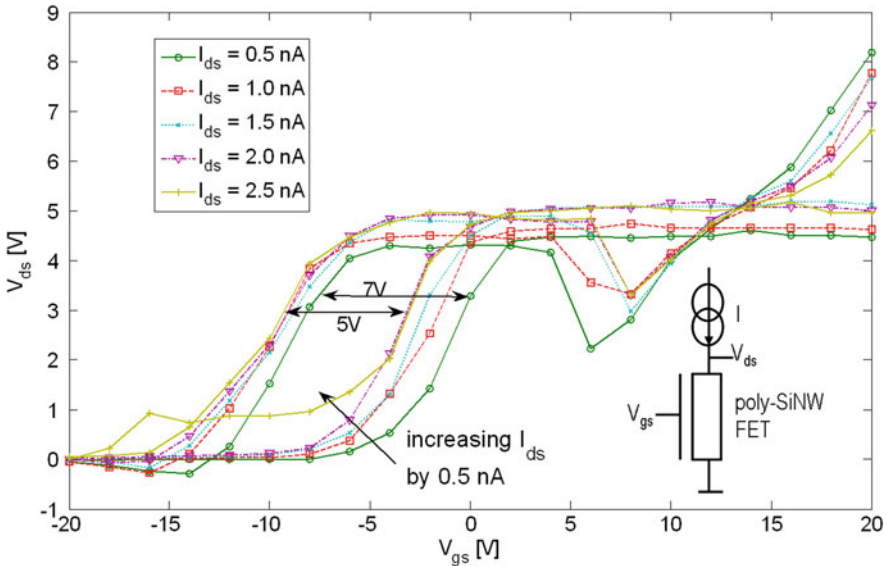


Fig. 2.25 Hysteresis of the $V_{ds} - V_{gs}$ transfer characteristics

contact area [52], which is responsible for the modulation of the Schottky barrier and the resulting hole and electron currents. The dominance of the p-type behaviour confirms the fact that nickel silicide contacts have a lower Schottky for holes than for electrons.

The transfer characteristics $V_{ds} - V_{gs}$ is shown in Fig. 2.24 for a fixed I_{ds} , and has a clear negative slope region. The same transfer characteristics have a hysteresis of 5–7 V, which decreases with increasing injected current I_{ds} (Fig. 2.25). The measured hysteresis is in agreement with the behaviour of poly-SiNW reported in literature and it can be explored in single nanowire memories [55].

2.7 Potential Applications

2.7.1 Crossbar Structures

A promising application of SiNW is the fabrication of crossbar structures. Previous approaches to build NW crossbars achieved *i*) metallic arrays, which do not have any semiconducting part that can be used as an access transistor, or *ii*) silicon-based crossbars with fluidic assembly, which have a larger pitch in average than the photolithography limit. Table 2.3 surveys the reported realized crossbars and shows that the proposed patterning technique has both advantages of yielding semi-conducting NW and a high crosspoint density $\sim 10^{10} \text{ cm}^{-2}$, as measured in the small crossbar of Fig. 2.19, while using conventional photolithographic processing steps. The use of the densest layers (Fig. 2.18) would yield a higher crosspoint density of $6.3 \times 10^{10} \text{ cm}^{-2}$.

2.7.2 Single Poly-Si Nanowire Memory

Besides the application as a crossbar array, there is another potential application as poly-SiNW memory based on the hysteresis of the $V_{ds} - V_{gs}$ transfer characteristic for a fixed I_{ds} . A poly-SiNW memory cell was already proposed in [55] and its

Table 2.3 Survey of reported nanowire crossbars. Functionalized arrays are those including molecular switches

References	[38]	[56]	[57]	This work
NW material	Si/Ti	Ti/Pt	Si	poly-Si
NW width [nm]	16	30	20	54
NW pitch [nm]	33	60	> 1000	100
Crossbar density [cm^{-2}]	10^{11}	2.7×10^{10}	N/A	10^{10}
Technique	SNAP	NIL	Self-assembly	MSPT
Functionalized?	yes	yes	no	no

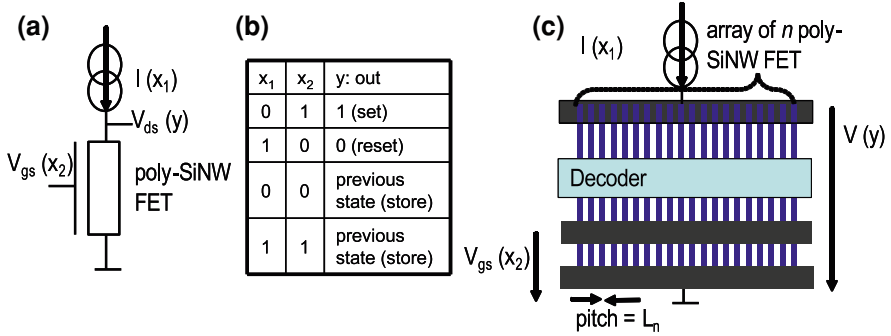


Fig. 2.26 Single poly-SiNW memory after [55]: **a** Poly-SiNW memory cell. **b** Memory operation. **c** High-density realization concept of poly-SiNW memory cells with MSPT

operation was experimentally demonstrated using I_{ds} and V_{gs} as inputs and V_{ds} as output storing the information. A single poly-SiNW memory cell after [55] and the organization of an array of similar cells in the proposed technology are illustrated in Fig. 2.26. The MSPT offers a denser pitch independent of the lithography, with a memory density scaling as L_l/L_n , where L_l and L_n represent the lithography and the MSPT pitch respectively. At the 65 nm technology node ($L_l = 2 \times 65$ nm) and with 20 nm wide nanowires ($L_n = 2 \times 20$ nm), the density with the MSPT is $3.2 \times$ higher. The density increases with decreasing L_n which scales with the thickness of the conformal layers.

2.7.3 Memristors

Memristors are the element that completes the symmetry of the equation system describing the relation between the fundamental circuit variables: current I , voltage V , charge Q and magnetic flux Φ [58]. They are the physical implementation of devices controlled by charge and magnetic flux and described by their memristance $M = d\Phi/dQ$. If the memristance is not constant, rather depending on Q , then the device $I - V$ curve shows a hysteric behavior that can be used in circuit design.

The significance of memristors arises from their natural existence in biological computational systems. For instance, ion diffusion is responsible of the time-dependant conductance of the neuron membrane in the Hodgkin-Huxley model [59], which is modeled as a memristive device. Learning mechanisms are also explained using the memristive model of synapses [60] and they were demonstrated with single devices [61]. Self-programming circuits were demonstrated by embedding memristors into logic circuits [62]. The memristor effect, seen as the hysteric behavior of the $I - V$ curve, may be obtained by using a circuitry that includes active elements and an internal power source [58, 63]. However, this solution is just an emulation of memristors and it consumes valuable chip area and

power. With the scaling of device dimensions, new phenomena have been claimed to be responsible for the memristor behavior in monolithic devices. For instance, it has been demonstrated that a memristor effect arises naturally in nanoscale systems in which solid-state electronic and ionic transport are coupled under an external bias voltage [64]. Voltage driven memristor effects were demonstrated as well in Pt/organic/Ti [65], in *polyethylene oxide (PEO)/polyaniline (PANI)* polymeric [61] and in amorphous silicon [66] devices.

Unlike basic two-terminal memristors, the fabricated devices have three terminals. The channel conductance depends on the trapped charges; thus the channel resistance may be represented as a function of the charge, in a similar way to a two-terminal memristor. The gate offers the opportunity to control the resulting $I_{ds} - V_{ds}$ hysteresis in a field-effect fashion. The device can be exploited in order to save information, in a reminiscent way to what has been explained before for single poly-SiNW memory cells.

2.7.4 Nanowire Decoders

Fabricating crossbars with a sub-photolithographic pitch raises the question of how to make every nanowire addressed by the outer CMOS circuit through a decoder. The design of crossbar decoders has attracted a lot of attention and the proposed solutions are either analog [28, 67, 68] or digital [56, 57, 69, 70]. Crossbars fabricated in the proposed approach can be addressed in either ways. In [28], it was suggested that the doping level modulation in the poly-SiNW body can differentiate the nanowires and make the implementation of an analog decoder in the MSPT technology possible. However, this approach needs more signal processing during the READ operation. In the following, a novel concept of fabricating a fully deterministic digital MSPT decoder is presented. The design aspects related to this technique are addressed in Sect. 3.4.

While a pattern can be easily defined during the growth of nanowires in a bottom-up process (Sect. 2.1.1), it is more difficult to define it with top-down processes. For instance, the MSPT, yields a regular array of undifferentiated nanowires if the bare procedure depicted in Fig. 2.7 is applied. Once the array is defined on a sub-lithographic scale, it is difficult to pattern it with standard photolithographic means, unless expensive high-resolution and time-costly methods, such as electro-beam lithography, are applied. Consequently, it is desirable to pattern the nanowires while they are defined: i.e., whenever a new spacer is defined, it has to be patterned before the next spacer is defined.

The fabrication flow that includes the decoder is illustrated in Fig. 2.27 and should be understood as an extension inserted between steps depicted in Fig. 2.7b and f. Other steps remain unchanged. The additional steps are lithography patterning and doping after every spacer definition step. Specific regions from every poly-Si nanowire are defined and doped in this way. Nanowires are fragile and thin structures, and they should be doped carefully with light doses. However, the total

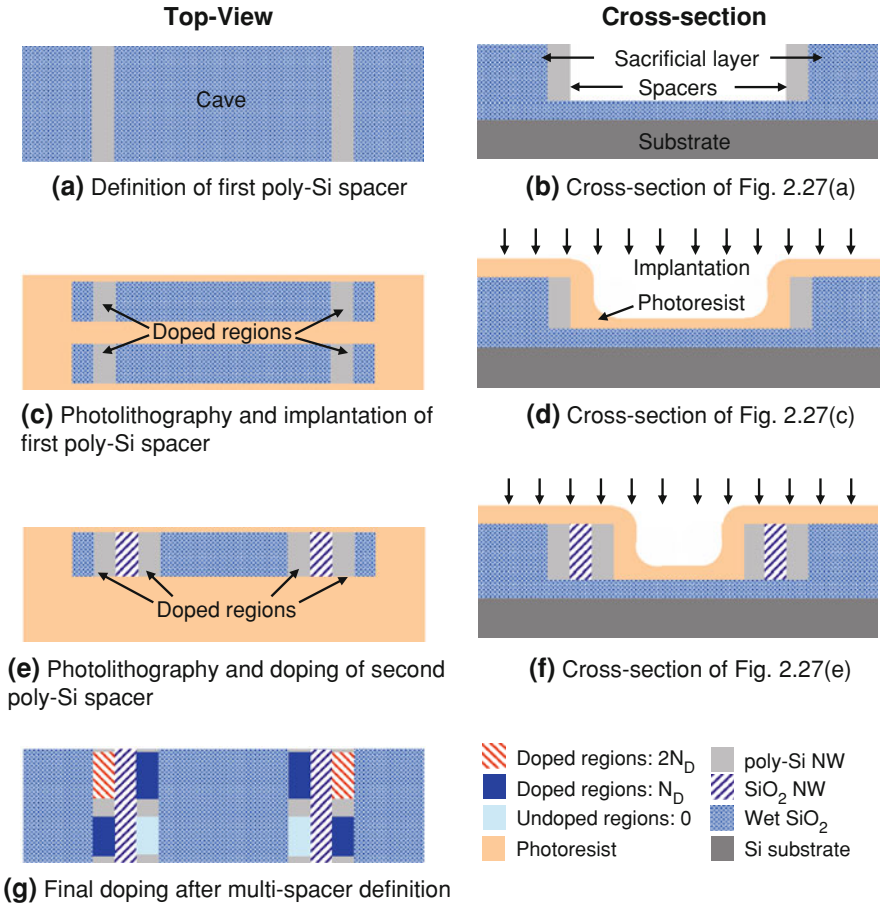


Fig. 2.27 Main process steps of MSPT decoder fabrication

doping level of a specific region is the sum of all doping levels accumulated in this region throughout the definition of the whole array, as illustrated in Fig. 2.27g. An optimized choice of the lithography/doping sequences and the doping doses may result in the desired nanowire pattern.

2.8 Discussions

One important question that may arise when it comes to the MSPT is the cost of the additional conformal deposition and RIE etch steps. The fabrication time needed for a 256×256 nanowire crossbar (8 kB memory) would be tremendous if 2×256 deposition/etch operations were required. Fortunately, the MSPT has two advantages. First, it can be parallelized within a single wafer: i.e., by using n parallel

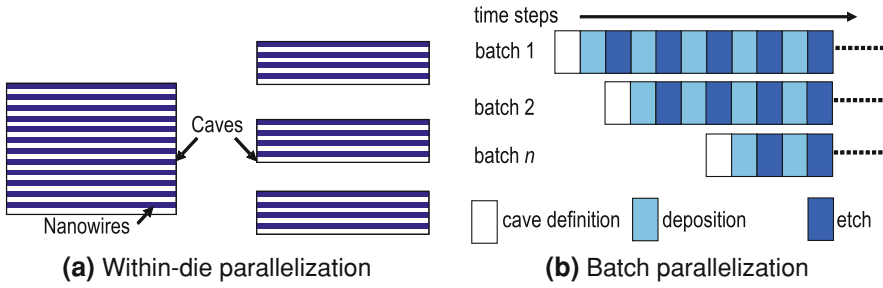


Fig. 2.28 Parallelization of the MSPT. **a** Using many small caves instead of a few large ones minimizes the number of steps, but has a cost in terms of area. **b** Any two batches can be processed together during the spacer definition steps, as long as the spacer parameters are identical

sacrificial layers instead of one, the number of deposition/etch steps is divided by n (Fig. 2.28a). Second, the technique allows for parallel batch processing, i.e., any two different batches can be processed together during the deposition/etch steps as long as the thickness of the conformal layers is the same (Fig. 2.28b).

Another important question about the proposed technique is related to the lower mobility of current carriers in the poly-Si used to define the structure, compared to crystalline Si. The question was generalized previously for any crossbar type: whatever the used NW material, the structure length and small cross-section will induce a slower signal propagation and higher resistance. To address this fact, it is generally believed [71] that the benefit of crossbars is to parallelize memory and computation in a grid with a large number of small crossbars, rather than using a limited number of large crossbars.

Considering the different potential applications presented in this chapter, it may be interesting to think of the advantages of using this process in order to fabricate single poly-SiNW memories or memristors, given the wide range of technologies that can be deployed to fabricate these devices. Clearly, the benefit in terms of area and integration density is the dominant advantage, since the considered technique easily yields structures with a pitch below the photo-lithographic limit. However, it is questionable to separately access these devices from the rest of the circuit defined on the lithography scale. This access requires the use of a decoder that addresses every nanowire separately. The benefits of this technology cannot be explored unless a decoder is available. The design aspects and the fabrication complexity of the proposed decoder concept will be therefore the core of the following chapter.

2.9 Chapter Contributions and Summary

This chapter has presented a first-time demonstration of the opportunity to use the multi-spacer patterning technique in order to fabricate the framework for crossbar circuits by integrating two layers of poly-Si spacers on top of each other.

The technique is cost-efficient and CMOS-compatible, in the sense that it does not require any additional steps other than those used in a standard CMOS process. It is also the only technique that uses only photolithography steps, while it is able to define structures with dimensions and pitch well below the photolithography pitch.

It has been demonstrated that the benefits of this technology go beyond the limit of crossbars circuits. In principle, the sub-photolithographic half pitch can be beneficial in any other application of the fabricated poly-SiNWs in terms of integration density. The hysteresis of the fabricated structures suggests their use as single poly-SiNW memories or memristors.

In this chapter a novel concept of fabricating nanowire decoders with the multi-spacer patterning technique has been introduced. It is the first time that a decoder for this nanowire technology is proposed. It has the advantage of being digital and deterministic. It is expected to have a minimal cost in terms of size. The technological costs have been addressed in this chapter. A more detailed investigation of the design aspects to this decoder will be given in the next chapter.

This chapter concludes the technology part of the book. The following parts are dealing with logic design aspects. Given the importance of the decoder for every crossbar circuit, the next chapter focuses on the decoder logic design methodologies. The first goal is to optimize the encoding scheme. The optimized codes are then used with the MSPT-decoder, as well as other decoder types, in order to assess the trade-offs between circuit area, yield and fabrication complexity.

References

1. Moselund KE, Bouvet D, Ben Jamaa HH, Atienza D, Leblebici Y, De Micheli G, Ionescu AM (2008) Prospects for logic-on-a-wire. *Microelectron Eng* 85:1406–1409
2. Auzelyte V, Solak HH, Ekinci Y, MacKenzie R, Vrs J, Olliges S, Spolenak R (2008) Large area arrays of metal nanowires. *Microelectron Eng* 85(5–6):1131–1134
3. Doherty L, Liu H, Milanovic V (2003) Application of MEMS technologies to nanodevices. In: *ISCAS'03. Proceedings of the 2003 International Symposium on Circuits and systems*, vol 3, pp III-934–III-937
4. Doherty L, Liu H, Milanovic V (2003) Application of MEMS technologies to nanodevices 3(5):III-934–III-937
5. Ng RMY, Wang T, Chan M (2007) A new approach to fabricate vertically stacked single-crystalline silicon nanowires. pp 133–136
6. Center for Micro- and Nanotechnologies (CMI) at EPFL. Available at: <http://cmi.epfl.ch>
7. Ben Jamaa MH, Cerofolini G, Leblebici Y, De Micheli G (2009) Nanowire Crossbar Framework Optimized for the Multi-Spacer Patterning Technique. In: *Proceedings of CASES, Grenoble, France*
8. Wagner RS, Ellis WC (1964) Vapor-liquid-solid mechanism for single crystal growth. *Appl Phys Lett* 4(5):89–90
9. Holmes JD, Johnston KP, Doty RC, Korgel BA (2000) Control of thickness and orientation of solution-grown silicon nanowires. *Science* 287(5457):1471–1473
10. Cui Y, Duan X, Hu J, Lieber CM (2000) Doping and electrical transport in silicon nanowires. *J Phys Chem B* 4(22):5213–5216
11. He R, Yang P (2006) Giant piezoresistance effect in silicon nanowires. *Nat Nanotechnol* 1(1):42–46

12. Lauhon LJ, Gudiksen MS, Wang D, Lieber CM (2002) Epitaxial core-shell and core-multishell nanowire heterostructures. *Nature* 420:57–61
13. Gudiksen MS, Lauhon LJ, Wang J, Smith DC, Lieber CM (2002) Growth of nanowire superlattice structures for nanoscale photonics and electronics. *Nature* 415:617–620
14. Hsu J-F, Huang B-R, Huang C-S (2005) The growth of silicon nanowires using a parallel plate structure. In: *The 5th IEEE Conference on Nanotechnology*, vol 2, pp 605–608
15. Yang C, Zhong Z, Lieber CM (2005) Encoding electronic properties by synthesis of axial modulation-doped silicon nanowires. *Science* 310(5752):1304–1307
16. Hochbaum AI, Fan R, He R, Yang P (2005) Controlled growth of Si nanowire arrays for device integration. *Nano Lett* 5(3):457–460
17. Schmidt V, Riel H, Senz S, Karg S, Riess W, Gösele U (2006) Realization of a silicon nanowire vertical surround-gate field-effect transistor. *Small* 2(1):85–88
18. Hayden O, Björk M, Schmid H, Riel H, Drechsler U, Karg S, Lörtscher E, Riess W (2007) Fully depleted nanowire field-effect transistor in inversion mode. *Small* 3(2):230–234
19. Huang Y, Duan X, Wei Q, Lieber CM (2001) Directed assembly of one-dimensional nanostructures into functional networks. *Science* 291(5504):630–633
20. Moselund KE, Bouvet D, Tschuur L, Pot V, Dainesi P, Eggimann C, Thomas NL, Houdré R, Ionescu AM (2007) Cointegration of gate-all-around MOSFETs and local silicon-on-insulator optical waveguides on bulk silicon. *IEEE Trans Nanotechnol* 6(1):118–125
21. Lee K-N, Jung S-W, Kim W-H, Lee M-H, Shin K-S, Seong W-K (2007) Well controlled assembly of silicon nanowires by nanowire transfer method. *Nanotechnology* 18(44):445302 (7pp)
22. Suk SD, Lee S-Y, Kim S-M, Yoon EJ, Kim M-S, Li M, Oh CW, Yeo KH, Kim SH, Shin D-S, Lee K-H, Park HS, Han JN, Park C, Park J-B, Kim D-W, Park D, Ryu B-I (2005) High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): fabrication on bulk Si wafer, characteristics, and reliability. In: *IEEE Transactions on Nanotechnology*, pp 717–720
23. Koo S-M, Fujiwara A, Han J-P, Vogel EM, Richter CA, Bonevich JE (2004) High inversion current in silicon nanowire field effect transistors. *Nano Lett* 4(11):2197–2201
24. Kedzierski J, Bokor J (1997) Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation. *J Vac Sci Technol B* 15(6):2825–2828
25. Vazquez-Mena O, Villanueva G, Savu V, Sidler K, van den Boogaart MAF, Brugger J (2008) Metallic nanowires by full wafer stencil lithography. *Nano Lett* 8(11):3675–3682
26. Hållstedt J, Hellström PE, Zhang Z, Malm B, Edholm J, Lu J, Zhang SL, Radamson H, Östling M (2006) A robust spacer gate process for deca-nanometer high-frequency MOSFETs. *Microelectron Eng* 83(3):434–439
27. Choi Y-K, Lee JS, Zhu J, Somorjai GA, Lee LP, Bokor J (2003) Sublithographic nanofabrication technology for nanocatalysts and DNA chips. *J Vac Sci Technol B: Microelectron Nanometer Struct* 21:2951–2955
28. Cerofolini G (2007) Realistic limits to computation. II. The technological side. *Appl Phys A* 86(1):31–42
29. Wu W, Jung G-Y, Olynick DL, Straznicki J, Li Z, Li X, Ohlberg DAA, Chen Y, Wang S-Y, Little JA, Tong WM, Williams RS (2005) One-kilobit cross-bar molecular memory circuits at 30-nm half-pitch fabricated by nanoimprint lithography. *Appl Phys A: Mater Sci Process* 80(6):1173–1178
30. Jung GY, Johnston-Halperin E, Wu W, Yu Z, Wang SY, Tong WM, Li Z, Green JE, Sheriff BA, Boukai A, Bunimovich Y, Heath JR, Williams RS (2006) Circuit fabrication at 17 nm half-pitch by nanoimprint lithography. *Nano Lett* 6(3):351–354
31. Sonkusale SR, Amsinck CJ, Nackashi DP, Spigna NHD, Barlage D, Johnson M, Franzon PD (2005) Fabrication of wafer scale, aligned sub-25nm nanowire and nanowire templates using planar edge defined alternate layer process. *Phys E: Low-dimensional Syst Nanostruct* 28(2):107–114

32. Smith PA, Nordquist CD, Jackson TN, Mayer TS, Martin BR, Mbindyo J, Mallouk TE (2000) Electric-field assisted assembly and alignment of metallic nanowires. *Appl Phys Lett* 77:1399–1401
33. Duan X, Huang Y, Cui Y, Wang J, Lieber CM (2001) Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices. *Nature* 409:66–69
34. Chen Y, Ohlberg DAA, Li X, Stewart DR, Stanley Williams R, Jeppesen JO, Nielsen KA, Stoddart JF, Olynick DL, Anderson E (2003) Nanoscale molecular-switch devices fabricated by imprint lithography. *Appl Phys Lett* 82:1610–1612
35. Zasadzinski JA, Viswanathan R, Madsen L, Garnea J, Schwartz DK (1994) Langmuir-Blodgett films. *Science* 263(5154):1726–1733
36. Wu W, Jung G-Y, Olynick DL, Straznicki J, Li Z, Li X, Ohlberg DAA, Chen Y, Wang S-Y, Liddle JA, Tong WM, Williams RS (2005) One-kilobit cross-bar molecular memory circuits at 30-nm half-pitch fabricated by nanoimprint lithography. *Appl Phys A: Mater Sci Process* 80(6):1173–1178
37. Melosh NA, Boukai A, Diana F, Gerardot B, Badolato A, Petroff PM, Heath JR (2003) Ultrahigh-density nanowire lattices and circuits. *Science* 300(5616):112–115
38. Green JE, Wook Choi J, Boukai A, Bunimovich Y, Johnston-Halperin E, Deionno E, Luo Y, Sheriff BA, Xu K, Shik Shin Y, Tseng HR, Stoddart JF, Heath JR (2007) A 160-kilobit molecular electronic memory patterned at 10^{11} bits per square centimetre. *Nature* 445: 414–417
39. Luo Y, Collier CP, Jeppesen JO, Nielsen KA, DeIonno E, Ho G, Perkins J, Tseng H-R, Yamamoto T, Stoddart JF, Heath JR (2002) Two-dimensional molecular electronics circuits. *J Chem Phys Phys Chem* 3:519–525
40. Ho G, Heath JR, Kondratenko M, Perepichka DF, Arseneault K, Pézolet M, Bryce MR (2005) The first studies of a tetrathiafulvalenesigma- acceptor molecular rectifier. *Chem—A Eur J* 11(10):2914–2922
41. McCreery RL (2004) Molecular electronic junctions. *Chem Mater* 16(23):4477–4496
42. Ashwell GJ, Urasinska B, Tyrrell WD (2006) Molecules that mimic Schottky diodes. *Phys Chem Chem Phys (Incorporating Faraday Transactions)* 8:3314–3319
43. Collier CP, Matternsteig G, Wong EW, Luo Y, Beverly K, Sampaio J, Raymo FM, Stoddart JF, Heath JR (2000) A [2]catenanebased solid state electronically reconfigurable switch. *Science* 289:1172–1175
44. Zhang Y, Kim S, McVittie J, Jagannathan H, Ratchford J, Chidsey C, Nishi Y, Wong H-S (2007) An integrated phase change memory cell with ge nanowire diode for cross-point memory. In: *IEEE Symposium on VLSI Technology*, pp 98–99
45. Voutsas AT, Hatalis MK (1992) Structure of as-deposited LPCVD silicon films at low deposition temperatures and pressures. *J Electrochem Soc* 139(9):2659–2665
46. Voutsas AT, Hatalis MK (1993) Surface treatment effect on the grain size and surface roughness of as-deposited LPCVD polysilicon films. *J Electrochem Soc* 140(1):282–288
47. Voutsas AT, Hatalis MK (1993) Deposition and crystallization of a-Si low pressure chemically vapor deposited films obtained by low-temperature pyrolysis of disilane. *J Electrochem Soc* 140(3):871–877
48. Pott V (2008) Gate-all-around silicon nanowires for hybrid single electron transistor/CMOS applications. Ph.D. dissertation, Lausanne, 2008. Available at: <http://library.ep.ch/theses/?nr=3983>
49. Nakazawa K (1991) Recrystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition from Si_2H_6 gas. *J Appl Phys* 69(3):1703–1706
50. Bergamini F, Bianconi M, Cristiani S, Gallerani L, Nubile A, Petrini S, Sugliani S (2008) Ion track formation in low temperature silicon dioxide. *Nucl Instrum Methods Phys Res Sect B: Beam Interact Mater Atoms* 266(10):2475–2478
51. Byon K, Tham D, Fischer JE, Johnson AT (2007) Systematic study of contact annealing: ambipolar silicon nanowire transistor with improved performance. *Appl Phys Lett* 90(14):143513

52. Appenzeller J, Knoch J, Tutuc E, Reuter M, Guha S (2006) Dualgate silicon nanowire transistors with nickel silicide contacts. In: International Electron Devices Meeting, pp 1–4
53. Weber WM, Geelhaar L, Graham AP, Unger E, Duesberg GS, Liebau M, Pamler W, Cheze C, Riechert H, Lugli P, Kreupl F (2006) Silicon-nanowire transistors with intruded nickel-silicide contacts. *Nano Lett* 6(12):2660–2666
54. Koo S-M, Edelstein MD, Li Q, Richter CA, Vogel EM (2005) Silicon nanowires as enhancement-mode Schottky barrier field-effect transistors. *Nanotechnology* 16(9):1482–1485
55. Ecoffey S, Mazza M, Pott V, Bouvet D, Schmid A, Leblebici Y, Declercq M, Ionescu A (2005) A new logic family based on hybrid MOSFET-polysilicon nanowires. pp 269–272
56. Hogg T, Chen Y, Kuekes P (2006) Assembling nanoscale circuits with randomized connections. *IEEE Trans Nanotechnol* 5(2):110–122
57. Beckman R, Johnston-Halperin E, Luo Y, Green JE, Heath JR (2005) Bridging dimensions: demultiplexing ultrahigh density nanowire circuits. *Science* 310(5747):465–468
58. Chua L (1971) Memristor—the missing circuit element. *IEEE Trans Circuit Theory* 18(5):507–519
59. Hodgkin AL, Huxley AF (1952) A quantitative description of membrane current and its application to conduction and excitation in nerve. *J Physiol* 117:500–544
60. Linares-Barranco B, Serrano-Gotarredona T (2009) Memristance can explain spike-time-dependent plasticity in neural synapses. In: *Nature Precedings*, pp 1–4
61. Smerieri A, Berzina T, Erokhin V, Fontana MP (2008) A functional polymeric material based on hybrid electrochemically controlled junctions. *Mater Sci Eng: C* 28(1):18–22
62. Borghetti J, Li Z, Straznicky J, Li X, Ohlberg DAA, Wu W, Stewart DR, Williams RS (2009) A hybrid nanomemristor/transistor logic circuit capable of self-programming. *Proc Natl Acad Sci* 106:1699–1703
63. Toumazou C, Georgiou J, Drakakis E (1998) Current-mode analogue circuit representation of Hodgkin and Huxley neuron equations. *Electron Lett* 34(14):1376–1377
64. Strukov DB, Snider GS, Stewart DR, Williams RS (2008) The missing memristor found. *Nature* 453:80–83
65. Stewart DR, Ohlberg DAA, Beck PA, Chen Y, Williams RS, Jeppesen JO, Nielsen KA, Stoddart JF (2004) Molecule independent electrical switching in Pt/organic monolayer/Ti devices. *Nano Lett* 4(1):133–136
66. Jo SH, Kim K-H, Lu W (2009) High-density crossbar arrays based on a Si memristive system. *Nano Lett* 9(2):870–874
67. Shenoy R, Gopalakrishnan K, Rettner C, Bozano L, King R, Kurdi B, Wickramasinghe H (2006) A new route to ultra-high density memory using the micro to nano addressing block (MNAB). In: *VLSI Technol.*, pp 140–141
68. Gopalakrishnan K, Shenoy RS, Rettner C, King R, Zhang Y, Kurdi B, Bozano LD, Weslser JJ, Rothwell MB, Jurich M, Sanchez MI, Hernandez M, Rice PM, Risk WP, Wickramasinghe HK (2005) The micro to nano addressing block. In: *IEEE Electron Devices Meeting*, p 19.4
69. DeHon A, Lincoln P, Savage J (2003) Stochastic assembly of sublithographic nanoscale interfaces. *IEEE Trans Nanotechnol* 2(3):165–174
70. Ben Jamaa MH, Leblebici Y, De Micheli G (2009) Decoding nanowire arrays fabricated with the multi-spacer patterning technique. In: *Design Automation Conference (DAC)*, San Francisco, California, USA
71. International technology roadmap for semiconductors (ITRS) (2007) <http://www.itrs.net/reports.html>. Tech. Rep., 2007

Regular Nanofabrics in Emerging Technologies
Design and Fabrication Methods for Nanoscale Digital
Circuits

Ben Jamaa, M.H.

2011, XX, 192 p., Hardcover

ISBN: 978-94-007-0649-1