

Chapter 2

Basic DC-DC Converter Theory

Several methods exist to achieve DC-DC voltage conversion. Each of these methods has its specific benefits and disadvantages, depending on a number of operating conditions and specifications. Examples of such specifications are the voltage conversion ratio range, the maximal output power, power conversion efficiency, number of components, power density, galvanic separation of in- and output, etc. When designing fully-integrated DC-DC converters these specifications generally remain relevant, nevertheless some of them will gain weight, as more restrictions emerge. For instance the used IC technology, the IC technology options and the available chip area will be dominant for the production cost, limiting the value and quality factor of the passive components. These limited values will in-turn have a significant impact upon the choice of the conversion method.

In order for the designer to obtain a clear view of the DC-DC voltage conversion methods and their individual advantages and disadvantages, with respect to monolithic integration, the three fundamental methods are discussed in this chapter. The first and oldest method of performing DC-DC voltage conversion is by means of linear voltage converters (resistive dividers), which are explained in Sect. 2.1. The second method, which also has an interesting potential for the purpose of monolithic voltage conversion, is by means of capacitor charge-pumps, as explained in Sect. 2.2. The latter two methods are explained more briefly as this work will mainly concentrate on inductive type DC-DC converters, which are discussed in Sect. 2.3.

Power conversion efficiency is in most cases a primary specification for any given energy converter. Therefore, a formal method for the fair comparison of DC-DC step-down voltage converters, in terms of power conversion efficiency, is introduced in Sect. 2.4. This method is referred to as the Efficiency Enhancement Factor (EEF). The chapter is concluded with the conclusions in Sect. 2.5.

2.1 Linear Voltage Converters

The most elementary DC-DC converters are linear voltage converters. They achieve DC-DC voltage conversion by dissipating the excess power into a resistor, making

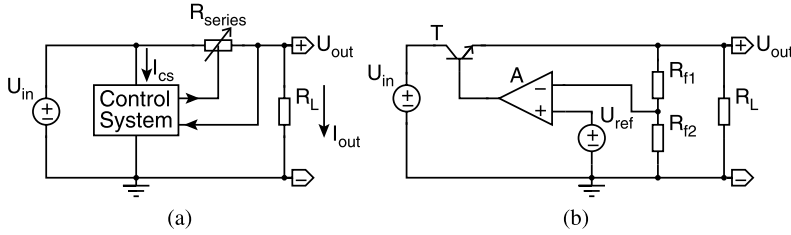


Fig. 2.1 (a) The principle of a linear series voltage converter and (b) a simple practical implementation

them resistive dividers. Clearly, this is not quite ideal for the power conversion efficiency η_{lin} . Another implication of their operating principle is the fact that they can only convert a certain input voltage U_{in} into a lower output voltage U_{out} , having the same polarity. In other words, the value of their voltage conversion ratio k_{lin} , given by (1.1), is always between zero and one.

The advantage of linear voltage converters is that they are fairly simple to implement. Moreover, they generally do not need large, and space consuming, inductors or capacitors, making them an attractive option for monolithic integration [Rin98]. Therefore, the two types of linear voltage converters, namely the series and the shunt regulator, are discussed in Sects. 2.1.1 and 2.1.2.

2.1.1 Series Converter

The operating principle of a linear series voltage converter is shown in Fig. 2.1(a). A variable resistor R_{series} is placed in series with the load R_L , lowering U_{in} to U_{out} . The resistance of R_{series} is controlled by the control system, which keeps U_{out} constant under varying values of U_{in} and R_L , by measuring U_{out} . The control system also consumes power, which is illustrated by its supply current I_{cs} . In this case the control system uses U_{in} as supply voltage, which can also be provided by U_{out} . However, the latter case will require a start-up circuit, as U_{out} is initially zero.

A practical implementation example for a linear series voltage converter is shown in Fig. 2.1(b). In this example R_{series} is implemented as an NPN BJT and the control system as an OPERational AMPlifier (OPAMP), which performs the task of an error amplifier. By doing so, U_{out} is determined by (2.1).

$$U_{out} = U_{ref} \frac{R_{f1} + R_{f2}}{R_{f2}} \quad (2.1)$$

By examining the operating principle of Fig. 2.1(a), η_{lin} can be calculated through (2.2). When I_{cs} is neglected and assumed to be zero, η_{lin} is equal to k_{lin} and thus independent of R_L . This is graphically illustrated by the black curve in Fig. 2.2(a). The gray curve illustrates the more realistic situation, where I_{cs} has a finite positive value. It can be seen that η_{lin} will tend to decrease when P_{out} decreases.

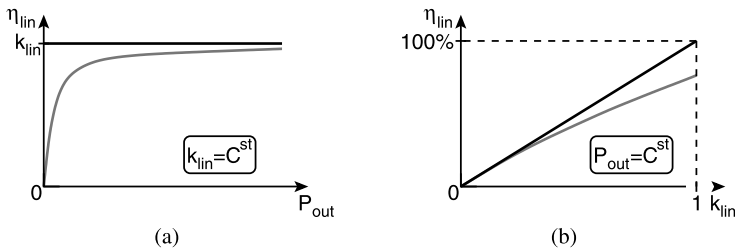


Fig. 2.2 (a) The power conversion efficiency η_{lin} as a function of the output power P_{out} for a linear series voltage converter, at a constant voltage conversion ratio k_{lin} . The black curve is valid for a zero control system supply current I_{cs} and the gray curve is valid for a non-zero I_{cs} . (b) The power conversion efficiency η_{lin} as a function of the voltage conversion ratio k_{lin} for a linear series voltage converter, at a constant output power P_{out} . The black curve is valid for a zero control system supply current I_{cs} and the gray curve is valid for a non-zero I_{cs}

Clearly, linear series voltage converters have an intrinsic advantage, in terms of power conversion efficiency, at high voltage conversion ratios.¹ This is illustrated by Fig. 2.2(b), where the black curve is valid for $I_{cs} = 0$ and the gray curve for a finite, non-zero I_{cs} . The gray curve shows that the impact of the power consumption of the control system on η_{lin} becomes more dominant when k_{lin} approaches unity.

$$\eta_{lin} = \frac{P_{out}}{P_{in}} = \frac{U_{out}I_{out}}{U_{in}(I_{out} + I_{cs})} \Big|_{I_{cs}=0} = \frac{U_{out}}{U_{in}} = k_{lin} \quad (2.2)$$

It is already mentioned that this type of converter is well suited for monolithic integration, due to its simple nature and lack of large passives. However, as the excess power is dissipated as a Joule-loss in R_{series} , the maximal P_{out} is limited by the allowed on-chip power dissipation. This limitation becomes more dominant for low values of k_{lin} .

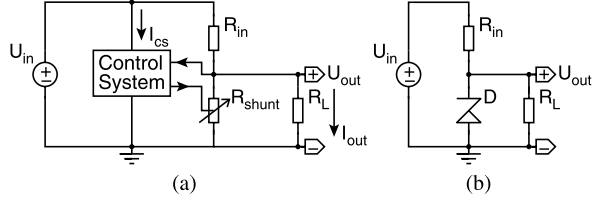
Note that variants of this type of voltage converter are used in several designs in this work for start-up and rail-shifting. More details can be found in Chap. 6.

2.1.2 Shunt Converter

The alternative for a linear series voltage converter is a linear shunt voltage converter. The principle of operation for this type of DC-DC converter is shown in Fig. 2.3(a). U_{in} is lowered to U_{out} by means of the resistive division between the fixed input resistor R_{in} and both the load R_L and the variable shunt resistor R_{shunt} , where U_{out} is calculated through (2.3). R_{in} can either be the intrinsic output resistance of U_{in} , an added resistor or the combination of both. U_{out} is kept constant

¹Linear series voltage converters are often used in applications which require a small voltage difference $U_{in} - U_{out}$, as they achieve a high η_{lin} in such cases. Therefore, they are commonly denoted as Low Drop-Out (LDO) regulators, which is not necessarily the case.

Fig. 2.3 (a) The principle of a linear shunt voltage converter and (b) a simple practical implementation



under varying R_L and U_{in} conditions by adapting the value of R_{shunt} . This operation can be performed by a control system, providing feedback from U_{out} . The control system consumes a certain amount of power by drawing a current I_{cs} from U_{in} or U_{out} . The fact that U_{out} can also be directly used to supply the control systems is due to the self-starting nature of this circuit, as opposed to the linear series voltage converter. The voltage used for supplying the control system will depend on whether U_{out} has a sufficiently large value. In the following analysis it is assumed that U_{in} is used for this purpose, for which the results merely differ little from the other possibility.

$$U_{out} = U_{in} \frac{R_L // R_{shunt}}{R_{in} + R_L // R_{shunt}} \quad (2.3)$$

Feedback of U_{out} is however not always required, as illustrated by the simple practical implementation of Fig. 2.3(b). For this implementation the shunt resistor is replaced by a reverse-biased zener diode D . In this way a quasi constant U_{out} can be achieved, if the current through D is kept large enough for it to operate in the zener-region.

For a shunt converter η_{lin} is calculated through (1.3), yielding (2.4).

$$\eta_{lin} = \frac{P_{out}}{P_{in}} = \frac{\frac{U_{out}^2}{R_L}}{\frac{U_{in}^2}{R_{in} + R_L // R_{shunt}} + U_{in} I_{cs}} \quad (2.4)$$

The explicit notation of R_{shunt} from (2.3) substituted into (2.4), yields (2.5). This expression for η_{lin} is not dependent on R_{shunt} .

$$\eta_{lin} = \frac{U_{out}^2}{R_L} \frac{R_{in}}{I_{cs} R_{in} U_{in} + U_{in}^2 - U_{in} U_{out}} \Big|_{I_{cs}=0} = \frac{U_{out}^2}{R_L} \frac{R_{in}}{U_{in}^2 - U_{in} U_{out}} \quad (2.5)$$

Figure 2.4(a) graphically illustrates η_{lin} as a function of the output power P_{out} , for a constant voltage conversion ratio k_{lin} . The black curve is valid for the ideal case where I_{cs} is zero and the gray curve is valid for a finite non-zero I_{cs} . As opposed to a linear series converter, η_{lin} is intrinsically linear dependent on P_{out} . It can be seen that η_{lin} is zero for $P_{out} = 0$ and that it has a maximal value equal to k_{lin} , occurring at the maximal output power P_{out_max} which is given by (2.6). For a given U_{in} and U_{out} , P_{out_max} is determined by the inverse of the value of R_{in} .

$$P_{out_max} = \frac{U_{out}(U_{in} - U_{out})}{R_{in}} \quad (2.6)$$

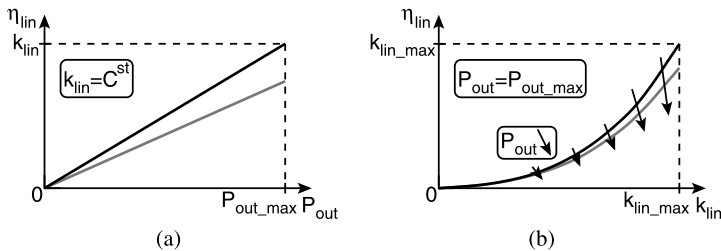


Fig. 2.4 (a) The power conversion efficiency η_{lin} as a function of the output power P_{out} for a linear shunt voltage converter, at a constant voltage conversion ratio k_{lin} . The black curve is valid for a zero control system supply current I_{cs} and the gray curve is valid for a non-zero I_{cs} . (b) The power conversion efficiency η_{lin} as a function of the voltage conversion ratio k_{lin} for a linear shunt voltage converter, for a constant value of $P_{out} = P_{out_max}$. The black curve is valid for a zero control system supply current I_{cs} and the gray curve is valid for a non-zero I_{cs}

The dependency of η_{lin} on k_{lin} is illustrated in Fig. 2.4(b), for a constant $P_{out} = P_{out_max}$. The black curve is valid when I_{cs} is zero and the gray curve is valid for a finite, non-zero value of I_{cs} . As explained for Fig. 2.4(a), η_{lin} is maximal for P_{out_max} . Therefore, the curves will become lower upon decreasing P_{out} , eventually congregating with the X-axis. The maximal achievable voltage conversion ratio k_{lin_max} is calculated by (2.7) and is for a given U_{out} inversely proportional to P_{out} and R_{in} .

$$k_{lin_max} = \frac{U_{out}^2}{U_{out}^2 + P_{out_max} R_{in}} \quad (2.7)$$

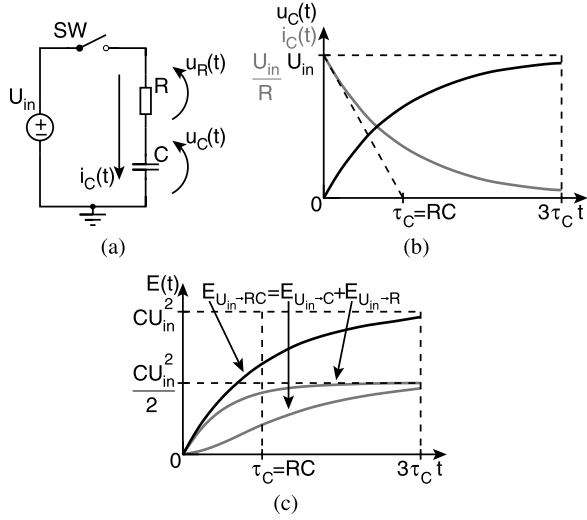
Unlike a linear series converter, where η_{lin} is ideally independent of P_{out} , a linear shunt converter only achieves its maximal η_{lin} at P_{out_max} . This behavior makes a linear shunt converter inferior compared to a series converter, in terms of η_{lin} . However, its simple practical implementation makes it suitable for applications that require a small and quasi constant P_{out} . Furthermore, a linear shunt converter can prove to be more practical than a linear series converter in applications that have a low value for k_{lin} and P_{out} . In such a case the voltage difference $U_{in} - U_{out}$ will only be present over the passive resistor R_{in} rather than over an active device, of which the maximal voltage is limited. The simple nature of a linear shunt voltage converter, and its lack of large passives, makes it suitable for monolithic integration in non-critical applications. Obviously, the problem of on-chip power dissipation remains and becomes more limiting than for linear series voltage converters.

Note that this type of voltage converter is also used in several designs in this work, for the purpose of start-up. More details can be found in Chap. 6.

2.2 Charge-Pump DC-DC Converters

Rather than linear converter methods to perform DC-DC voltage conversion, which are described in Sect. 2.1, switched-mode DC-DC converters acquire energy-storing

Fig. 2.5 (a) The circuit for charging a capacitor C with a series resistor R by means of a voltage source U_{in} . (b) The voltage $u_C(t)$ over C and the current $i_C(t)$ through C , as a function of time. (c) The energy $E_{U_{in} \rightarrow RC}(t)$ delivered by U_{in} , the energy $E_{U_{in} \rightarrow C}(t)$ stored in C and the energy $E_{U_{in} \rightarrow R}(t)$ dissipated in R , as a function of time



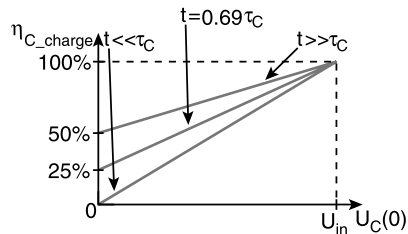
passives and switches to alter the connections between them. Ideally, this switching can be performed lossless, as explained in Sect. 1.1.1, which is preliminary assumed in this section. The losses associated with switching in inductive DC-DC converters are discussed in Chap. 4, of which the main principles remain valid for other types of converters. This section discusses the basics of switched-mode charge-pump DC-DC converters, which only use capacitors as energy-storing elements.

In Sect. 2.2.1 the principles for using capacitors as energy reservoirs is explained and some basic calculations are conducted. These calculations will be used to investigate two ideal charge-pump DC-DC converters. In Sect. 2.2.2 a series-parallel step-down DC-DC converter is discussed, followed by a series-parallel step-up DC-DC converter in Sect. 2.2.3.

2.2.1 On Capacitors

The charging of capacitors is a process that is intrinsically lossy, even when all the components in the charge-circuit are considered to be ideal and lossless. This is explained by means of the circuit for the charging of a capacitor C , with a series resistor R and out of a voltage source U_{in} . This circuit is shown in Fig. 2.5(a). The voltage $u_C(t)$ over C and the current $i_C(t)$ through C , as a function of time, are shown in Fig. 2.5(b), where it is assumed that the initial voltage $U_C(0)$ over C is zero. $u_C(t)$ and $i_C(t)$ are calculated by means of (2.8) and (2.9) respectively. At the time equal to the time constant $t = \tau_C$ the values of $u_C(t)$ and $i_C(t)$ are 63% of the steady-state values, where $t = \infty$, and at $t = 3\tau_C$ their values are 95% of the steady-state values.

Fig. 2.6 The energy charging efficiency η_{C_charge} of a capacitor charged by means of a voltage source U_{in} as a function of the initial voltage $U_C(0)$ over the capacitor, for three different charge times t



$$u_C(t) = U_{in} + (U_C(0) - U_{in})e^{-\frac{t}{RC}} \quad (2.8)$$

$$i_C(t) = \frac{U_{in} - U_C(0)}{R} e^{-\frac{t}{RC}} \quad (2.9)$$

The corresponding energy $E_{U_{in} \rightarrow RC}(t)$ that is delivered by U_{in} , the energy $E_{U_{in} \rightarrow R}(t)$ that is dissipated in R and the energy $E_{U_{in} \rightarrow C}(t)$ that is stored in C , as a function of time, are calculated through (2.10), (2.11) and (2.12), respectively. These energies are plotted as a function of time in Fig. 2.5(c). Analogue to Fig. 2.5(b), $U_C(0)$ is assumed to be zero. It can be seen that for this case the steady-state values of $E_{U_{in} \rightarrow R}(t)$ and $E_{U_{in} \rightarrow C}(t)$ are equal. However, in the transient region $E_{U_{in} \rightarrow R}(t)$ is higher than $E_{U_{in} \rightarrow C}(t)$, making this region undesired for the charging of C . Therefore, it is understood that, from a energy efficiency point of view, when charging a capacitor by means of a voltage source, the steady-state region should be approached sufficiently close. It is noted that it this conclusion can also be proven for the charging of a capacitor by means of another capacitor, which is omitted here.

$$E_{U_{in} \rightarrow RC}(t) = \int_0^t U_{in} i_C(t) dt = C U_{in} (U_C(0) + U_{in}) (1 - e^{-\frac{t}{RC}}) \quad (2.10)$$

$$E_{U_{in} \rightarrow R}(t) = \int_0^t u_R(t) i_C(t) dt = \frac{C(U_C(0) - U_{in})^2}{2} (1 - e^{-\frac{2t}{RC}}) \quad (2.11)$$

$$E_{U_{in} \rightarrow C}(t) = E_{U_{in} \rightarrow RC} - E_{U_{in} \rightarrow R} \quad (2.12)$$

In the case of Fig. 2.5(c), where the value of $U_C(0)$ is assumed zero, half of the energy in steady-state is dissipated in R . This is obviously not the case when $U_C(0) > 0$, as otherwise a charge-pump would never reach a power conversion efficiency higher than $50\% \cdot 50\% = 25\%$. In order to comprehend the relation between the charging time t , $U_C(0)$ and the energy charging efficiency $\eta_{C_charge}(t)$ of a capacitor by means of a voltage source, $\eta_{C_charge}(t)$ is calculated accordingly to (2.13).

$$\eta_{C_charge}(t) = \frac{E_{U_{in} \rightarrow C}(t)}{E_{U_{in} \rightarrow RC}(t)} = \frac{(2.12)}{(2.10)} = \frac{U_C(0) + U_{in} + (U_C(0) - U_{in})e^{-\frac{t}{RC}}}{2U_{in}} \quad (2.13)$$

This relation is graphically represented in Fig. 2.6, where η_{C_charge} is plotted as a function of $U_C(0)$, for three different values of t : $t \ll \tau_C$, $t = 0.69 \cdot \tau_C$ and $t \gg \tau_C$. It is observed that $\eta_{C_charge}(t)$ increases upon an increasing t , for a certain constant value of $U_C(0)$, meaning that steady-state is approached more closely. This

is already concluded earlier in this section, for the case where $U_C(0) = 0$. It can also be seen that $\eta_{C_charge}(t)$ increases when $U_C(0)$ increases, for a certain constant t . Moreover, $\eta_{C_charge}(t)$ approaches 100% for the case when $U_C(0) = U_{in}$. Using this knowledge allows for the following conclusions to be made, for maximizing $\eta_{C_charge}(t)$:

- Sufficient settling time $t \gg \tau_C$ is to be provided, however the effect of settling on $\eta_{C_charge}(t)$ becomes less dominant if $U_C(0)$ approaches U_{in} .
- The value of $U_C(0)$ should be as close as possible to U_{in} . However, the more $U_C(0)$ approaches to U_{in} , the less energy is transferred to C , which becomes zero for the following condition: $U_C(0) = U_{in}$.
- These conclusions are also valid for the charging of capacitors with one another.

Because of the fact that switching can be ideally lossless and because the charging of capacitors can be performed with $\eta_{C_charge}(t)$ approaching a value of 100%, charge-pump DC-DC converters have a promising prospect on the achievable conversion efficiency. Indeed, they could theoretically achieve higher power conversion efficiencies than do linear voltage converters, which are explained in Sect. 2.1.

2.2.2 Series-Parallel Step-Down Converter

The circuit topology of an ideal series-parallel charge-pump step-down DC-DC converter is shown in Fig. 2.8(a). Its basic operation consists of two phases:

1. *The flying capacitor charge phase Φ_1* : During Φ_1 both the flying-capacitor C_1 and the output capacitor C_2 are charged, in series with each other, through the voltage source U_{in} . This is done by closing the switches SW_1 – SW_4 and opening SW_2 – SW_3 , yielding the equivalent charge circuit shown in Fig. 2.8(b). In Φ_1 a part of the charge current through C_1 also flows through the load R_L .
2. *The flying capacitor discharge phase Φ_2* : During Φ_2 C_2 is charged by C_1 , by placing C_1 parallel with C_2 . This is achieved by opening SW_1 – SW_4 and closing SW_2 – SW_3 , yielding the equivalent discharge circuit shown in Fig. 2.8(c). Similar as in Φ_1 a part of the charge current from C_1 also flows through R_L . After this second phase the first phase is started again. The frequency at which this is done is denoted as the switching frequency f_{sw} .

From this operation principle it follows that U_{out} can never exceed $U_{in}/2$, as this would cause reversing of the energy flow from the output to the input. Obviously, this is physically not possible. By means of these principles a simple expression for U_{out} can be formulated, given by (2.23). In this equation I_{out} is the current through the load, ΔQ_{SW} is the amount of charge being transferred to the output in each switching cycle and ΔU_{C_1} is the voltage difference over C_1 , between Φ_1 and Φ_2 . The equation readily shows that, for an ideal converter, U_{out} is proportional to R_L , f_{sw} and C_1 and that U_{out} will asymptotically reach the value of $U_{in}/2$.

⊗ CHARGED CAPACITORS IN EQUILIBRIUM

The circuit for charging a capacitor C_b with another capacitor C_a is shown in Fig. 2.7(a). It is proved that for $t \gg \tau_C$ the energy transfer is independent of the value of the series resistor R . This is done by calculating the limit, where $t/\tau_C \rightarrow \infty$, for the energy equations $E_{C_a \rightarrow RC_b}$ and $E_{C_a \rightarrow R}$, yielding (2.14) and (2.15). $E_{C_a \rightarrow C_b}$ is subsequently calculated by (2.16).

$$E_{C_a \rightarrow RC_b} = \lim_{\frac{t(C_a+C_b)}{C_a C_b R} \rightarrow \infty} \left[\int_0^t U_{C_a}(t) I(t) dt \right] \\ = -\frac{C_a C_b^2}{2(C_a + C_b)^2} \Delta U^2 + \frac{U_{C_a}(0) C_a C_b}{C_a + C_b} \Delta U \quad (2.14)$$

$$E_{C_a \rightarrow R} = \lim_{\frac{t(C_a+C_b)}{C_a C_b R} \rightarrow \infty} \left[\int_0^t U_R(t) I(t) dt \right] = \frac{C_a C_b}{2(C_a + C_b)} \Delta U^2 \quad (2.15)$$

$$E_{C_a \rightarrow C_b} = E_{C_a \rightarrow RC_b} - E_{C_a \rightarrow R} \\ = -\frac{C_a C_b (C_a + 2C_b)}{2(C_a + C_b)^2} \Delta U^2 + \frac{U_{C_a}(0) C_a C_b}{C_a + C_b} \Delta U \quad (2.16)$$

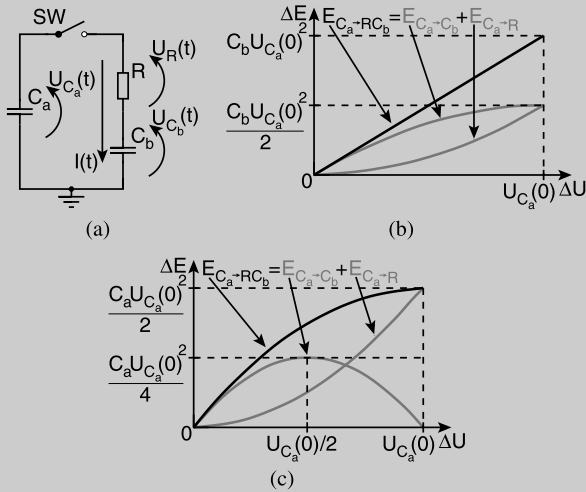


Fig. 2.7 (a) The circuit for charging C_b with C_a . (b) The $E_{C_a \rightarrow RC_b}$, $E_{C_a \rightarrow C_b}$ and $E_{C_a \rightarrow R}$ as a function of $\Delta U = U_{C_a}(0) - U_{C_b}(0)$, for $C_a \gg C_b$ and (c) for $C_b \gg C_a$

The obtained expressions for the energy transfers can be subdivided for two special cases. The first case, where $C_a \gg C_b$, results in (2.17), (2.18) and (2.19). This is illustrated in Fig. 2.7(b), where $E_{C_a \rightarrow RC_b}$, $E_{C_a \rightarrow C_b}$ and $E_{C_a \rightarrow R}$ are plotted normalized as a function of time. The second case, where $C_b \gg C_a$, results in (2.20), (2.21) and (2.22). This is illustrated in Fig. 2.7(c), similar as in Fig. 2.7(b).

⊕CHARGED CAPACITORS IN EQUILIBRIUM (CONTINUED)

$$C_a \gg C_b \implies E_{C_a \rightarrow RC_b} \simeq C_b U_{C_a}(0) \Delta U \quad (2.17)$$

$$\implies E_{C_a \rightarrow R} \simeq \frac{C_b}{2} \Delta U^2 \quad (2.18)$$

$$\implies E_{C_a \rightarrow C_b} \simeq -\frac{C_b}{2} \Delta U^2 + C_b U_{C_a}(0) \Delta U \quad (2.19)$$

$$C_b \gg C_a \implies E_{C_a \rightarrow RC_b} \simeq -\frac{C_a}{2} \Delta U^2 + C_a U_{C_a}(0) \Delta U \quad (2.20)$$

$$\implies E_{C_a \rightarrow R} \simeq \frac{C_a}{2} \Delta U^2 \quad (2.21)$$

$$\implies E_{C_a \rightarrow C_b} \simeq -C_a \Delta U^2 + C_a U_{C_a}(0) \Delta U \quad (2.22)$$

Please note that for the case where $C_a \gg C_b$ the obtained results are also valid for the circuit of Fig. 2.5(a), with $U_C(0) = U_{in}$.

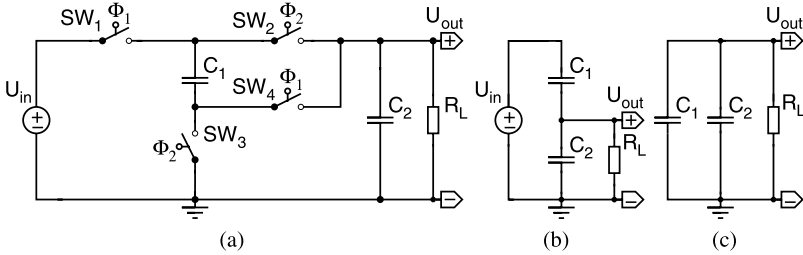


Fig. 2.8 (a) The circuit of an ideal series-parallel charge-pump step-down DC-DC converter, together with (b) its equivalent charge circuit and (c) its equivalent discharge circuit

$$U_{out} = R_L I_{out} = R_L f_{SW} \Delta Q_{SW} = R_L f_{SW} C_1 \Delta U_{C_1} = R_L f_{SW} C_1 (U_{in} - 2U_{out})$$

$$\implies U_{out} = \frac{R_L f_{SW} C_1 U_{in}}{1 + 2R_L f_{SW} C_1} \blacksquare \quad (2.23)$$

The process of charging capacitors by means of voltage sources, as well as other capacitors, is intrinsically prone to losses, as discussed earlier in this section. Hence, by making the assumption that the series-parallel charge-pump consists of ideal and lossless components, the ideal power conversion efficiency η_{sp_down} as a function of the voltage ratio $k_{SW} = U_{in}/U_{out}$ can be calculated. For this ideal converter it is assumed that the output voltage ripple ΔU_{out} is infinitesimal, implying that f_{SW} is infinitely large and that there is no dependency on R_L , which follows from (2.23). Furthermore, as the switches are assumed ideal there are no switch losses, therefore η_{sp_down} is independent of f_{SW} . The calculation of η_{sp_down} is performed in three steps. In the first step the energy conversion efficiency η_{Φ_1} of the charge phase is determined. The circuit of this phase, where C_1 and C_2 are charged through U_{in} , is similar to that of Fig. 2.7(a), for the case where $C_a \gg C_b$. As a result, η_{Φ_1} is given by (2.24).

$$\frac{E_{C_a \rightarrow C_b}}{E_{C_a \rightarrow RC_b}} = \frac{(2.19)}{(2.17)} \quad \text{with} \quad \begin{cases} \Delta U = U_{in} - 2U_{out} \\ C_b = \frac{C_1 C_2}{C_1 + C_2} \\ U_{C_a}(0) = U_{in} \end{cases}$$

$$\Rightarrow \eta_{\Phi_1} = \frac{E_{C_1 C_2}}{E_{U_{in} \rightarrow C_1 C_2}} = \frac{U_{in} + 2U_{out}}{2U_{in}} \quad (2.24)$$

In the second step the energy conversion efficiency η_{Φ_2} of the discharge phase is determined. In this phase C_1 is discharged through C_2 , as illustrated by Fig. 2.7(a). Accordingly, η_{Φ_2} can be calculated analogue to (2.24). However, for this phase C_1 and C_2 are assumed to obtain arbitrary values, yielding (2.25).

$$\frac{E_{C_a \rightarrow C_b}}{E_{C_a \rightarrow RC_b}} = \frac{(2.16)}{(2.14)} \quad \text{with} \quad \begin{cases} \Delta U = U_{in} - 2U_{out} \\ U_{C_a}(0) = U_{in} - U_{out} \end{cases}$$

$$\Rightarrow \eta_{\Phi_2} = \frac{E_{C_2}}{E_{C_1 \rightarrow C_2}} = \frac{C_1 U_{in} + 2C_2 U_{out}}{U_{in}(2C_1 + C_2) - 2C_1 U_{out}} \quad (2.25)$$

Finally, for the third step η_{sp_down} can be calculated, resulting in (2.26).

$$\eta_{sp_down} = \eta_{\Phi_1} \eta_{\Phi_2} = \frac{(C_1 U_{in} + 2C_2 U_{out}) \left(\frac{U_{in} + 2U_{out}}{2U_{in}} \right)}{C_2 U_{in} + 2C_1 (U_{in} - U_{out})} \blacksquare \quad (2.26)$$

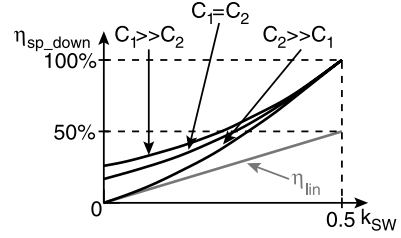
In addition, for the purpose of graphically representing this information, two special cases of (2.26) are considered: The case where the flying capacitor C_1 is significantly larger than the output capacitor C_2 and vice versa. The first case is given by (2.27) and the second case by (2.28).

$$C_1 \gg C_2 \quad \Rightarrow \quad \eta_{sp_down} = \frac{U_{in} + 2U_{out}}{4U_{in} - 4U_{out}} \quad (2.27)$$

$$C_2 \gg C_1 \quad \Rightarrow \quad \eta_{sp_down} = \frac{U_{in} U_{out} + 2U_{out}^2}{U_{in}^2} \quad (2.28)$$

The graphical representation of (2.26), (2.27) and (2.28), illustrated in Fig. 2.9 by the black curves, shows η_{sp_down} as a function of k_{SW} . For the case of (2.26) the value of C_1 and C_2 are assumed to be equal. The gray curve shows η_{lin} of an ideal linear series converter, for comparison (refer to Sect. 2.1.1). It is observed that for all three cases of the values of C_1 and C_2 , a higher power conversion efficiency than achievable with a linear series converter is obtained. Also, for all three cases η_{sp_down} reaches its maximum value of 100% at $k_{SW} = 0.5$ and decreases upon decreasing values of k_{SW} . This can be understood by reconsidering Fig. 2.6, where it can be seen that η_{C_charge} decreases when $U_{in} - U_C(0)$ increases. Similar behavior can be observed when k_{SW} decreases. For the charge phase this implies that $U_{in} - (U_{C_1}(0) + U_{C_2}(0))$ increases and for the discharge phase $U_{C_1}(0) - U_{C_2}(0)$ increases. Finally, it can be seen that the highest overall η_{sp_down} is obtained for the case where $C_1 \gg C_2$. This follows from the fact that the charging of capacitors with one another is more efficient if the charging capacitor is larger than the capacitor being charged, as can be seen by comparing the graphical representations from Fig. 2.7(a) and Fig. 2.7(b).

Fig. 2.9 The black curves show the power conversion efficiency η_{sp_down} of an ideal series-parallel charge-pump step-down DC-DC converter, as a function of the voltage conversion ratio k_{SW} , for three different cases of the values of C_1 and C_2 . The gray curve shows the power conversion efficiency of a linear series converter, as a function of k_{SW}



This kind of converter topologies is quite promising, seen from the perspective towards monolithic integration. The advantage over linear voltage converters, which are explained in Sect. 2.1, in terms of η_{sp_down} , is clearly illustrated in Fig. 2.9. Practical monolithic realizations in standard CMOS technologies of charge-pump step-down converters show that high values for η_{sp_down} are realistic [Ram10]. However, care must be taken when comparing η_{sp_down} , as it should be normalized conform to k_{SW} . This is elaborated upon in Sect. 2.4. There are also a few potential drawbacks. First, this topology is limited in a sense that the maximal k_{SW} can never exceed the value of 0.5. Obviously, this can be overcome by using a different topology, which is however beyond the scope of this work. Secondly, two capacitors for storing the energy are necessary. Therefore, this type of switched converter will inevitably require more chip area, compared to a linear converter with a similar maximal output power. Thirdly, although η_{sp_down} can theoretically reach a value of 100%, this case for which $k_{SW} = 0.5$ will not always prove to be practical in a real-world application. This can also be partially solved by using different, more complex, gear-box topologies [Mak95], of which a discussion is also omitted in this work. Finally, four switches are required, where other switched converter topologies can provide similar functionality with only two switches, as explained in Sect. 3.1.

2.2.3 Series-Parallel Step-Up Converter

Unlike linear voltage converters switched-mode voltage converters are capable of converting a given input voltage to a higher output voltage. Such converters are commonly denoted as step-up converters. A straightforward example of a charge-pump step-up converter is the series-parallel converter, of which the circuit topology with ideal components is shown in Fig. 2.10. The basic operation of this converter consists of two phases:

1. *The flying capacitor charge phase Φ_1* : During Φ_1 the flying-capacitor C_1 is charged through the voltage source U_{in} . This is done by closing the switches SW_1 – SW_3 and opening SW_2 – SW_4 , yielding the equivalent charge circuit shown

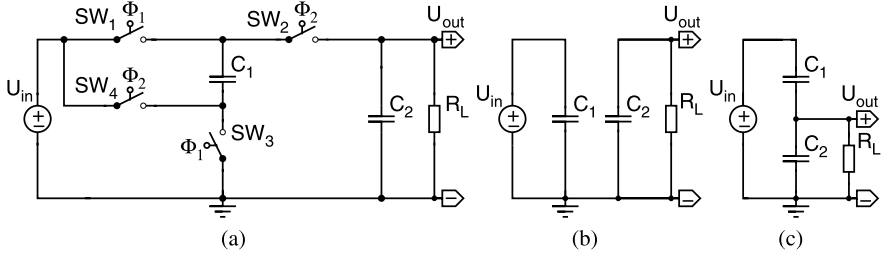


Fig. 2.10 (a) The circuit of an ideal series-parallel charge-pump step-up DC-DC converter, together with (b) its equivalent charge circuit and (c) its equivalent discharge circuit

in Fig. 2.10(b). Also, in this phase the output capacitor C_2 is discharged through the load R_L .

2. *The flying capacitor discharge phase Φ_2* : During Φ_2 C_2 is charged by C_1 and U_{in} , by placing C_1 in series with U_{in} . This is achieved by opening SW_1 – SW_3 and closing SW_2 – SW_4 , yielding the equivalent charge circuit shown in Fig. 2.10(c). A part of the charge current from C_1 and U_{in} also flows through R_L . After this second phase the first phase is started again. The frequency at which this is done is denoted as the switching frequency f_{SW} .

The conclusions and calculations made in the following discussion are similar to those of the series-parallel step-down charge-pump of Sect. 2.2.2, hence the following explanation will be more briefly. U_{out} of the series-parallel step-up converter is limited to $2U_{in}$ and is calculated by means of (2.29). This leads to the conclusion that $0 < U_{out} < 2U_{in}$, where the value of $2U_{in}$ is asymptotically reached.

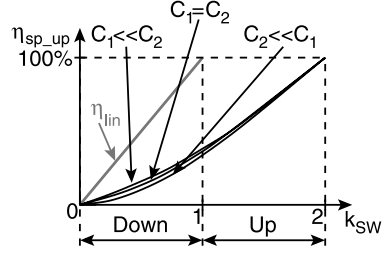
$$\begin{aligned}
 U_{out} &= R_L I_{out} = R_L f_{SW} \Delta Q_{SW} = R_L f_{SW} C_1 \Delta U_{C_1} = R_L f_{SW} C_1 (2U_{in} - U_{out}) \\
 \Rightarrow U_{out} &= \frac{2R_L f_{SW} C_1 U_{in}}{1 + R_L f_{SW} C_1} \blacksquare
 \end{aligned} \tag{2.29}$$

For this converter topology the ideal power conversion efficiency η_{sp_up} will also depend on k_{SW} . In order to calculate this dependency, ΔU_{out} is assumed to be zero, implying that f_{SW} is infinitely large. Thus, it follows from (2.29) that there is no dependency on R_L . The calculation itself is performed in three steps. First, the energy conversion efficiency η_{Φ_1} of the charge phase is determined, which is done analogue to the calculation of (2.24). In this case only C_1 is charged, yielding (2.30).

$$\begin{aligned}
 \frac{E_{C_a \rightarrow C_b}}{E_{C_a \rightarrow RC_b}} &= \frac{(2.19)}{(2.17)} \quad \text{with} \quad \begin{cases} \Delta U = 2U_{in} - U_{out} \\ C_b = C_1 \\ U_{C_a}(0) = U_{in} \end{cases} \\
 \Rightarrow \eta_{\Phi_1} &= \frac{E_{C_1}}{E_{U_{in} \rightarrow C_1}} = \frac{U_{out}}{2U_{in}}
 \end{aligned} \tag{2.30}$$

Secondly, the energy conversion efficiency η_{Φ_1} of the discharge phase is calculated. The calculation method is analogue to (2.25), resulting in (2.31).

Fig. 2.11 The *black curves* show the power conversion efficiency η_{sp_up} of an ideal series-parallel charge-pump step-up DC-DC converter, as a function of the voltage conversion ratio k_{SW} , for three different cases of the values of C_1 and C_2 . The *gray curve* shows the power conversion efficiency η_{lin} of a linear series converter, as a function of k_{SW}



$$\frac{E_{C_a \rightarrow C_b}}{E_{C_a \rightarrow RC_b}} = \frac{(2.16)}{(2.14)} \quad \text{with} \quad \begin{cases} \Delta U = 2U_{in} - U_{out} \\ U_{C_a}(0) = 2U_{in} \end{cases}$$

$$\Rightarrow \eta_{\Phi_2} = \frac{E_{C_2}}{E_{U_{in}C_1 \rightarrow C_2}} = \frac{2C_1U_{in} + C_1U_{out} + 2C_2U_{out}}{4C_1U_{in} + 2C_2U_{in} + C_2U_{out}} \quad (2.31)$$

Thirdly, the resulting η_{sp_up} is calculated by means of (2.32).

$$\eta_{sp_up} = \eta_{\Phi_1}\eta_{\Phi_2} = \frac{U_{out}(2C_2U_{out} + C_1(2U_{in} + U_{out}))}{2U_{in}(4C_1U_{in} + C_2(2U_{in} + U_{out}))} \blacksquare \quad (2.32)$$

Two special cases for (2.32): 1) the flying capacitor C_1 is significantly larger than the output capacitor C_2 and 2) vice versa, are also considered. The results for these two cases are respectively given by (2.33) and (2.34).

$$C_1 \gg C_2 \quad \Rightarrow \quad \eta_{sp_up} = \frac{2U_{in}U_{out} + U_{out}^2}{8U_{in}^2} \quad (2.33)$$

$$C_2 \gg C_1 \quad \Rightarrow \quad \eta_{sp_up} = \frac{U_{out}^2}{2U_{in}^2 + U_{in}U_{out}} \quad (2.34)$$

The graphical representation of (2.32), (2.33) and (2.34) is illustrated in Fig. 2.11, where the black curves show η_{sp_up} as a function of k_{SW} . For (2.32), the values of C_1 and C_2 are chosen equally large. The gray curve shows η_{lin} of an ideal linear series converter, for comparison (refer to Sect. 2.1.1). Although this converter is designated for step-up voltage conversion, it is also capable to perform a step-down function. This is indicated on the X-axis. For the step-down operation region, the achievable η_{sp_up} is however significantly lower than for a series-parallel step-down converter, as can be seen in Fig. 2.9, and it is also significantly lower than for a linear series regulator. Thus, the step-down operation region of this converter has no practical use. The step-up operation region yields theoretical values for η_{sp_up} ranging from about 35%, for $k_{SW} = 1$, to 100%, for $k_{SW} = 2$. The reason for η_{sp_up} to decrease upon decreasing values for k_{SW} is due to the fact that the charging of capacitors becomes less efficient when $U_{in} - U_{C_i}(0)$ increases, as is illustrated in Fig. 2.6. Translated for this converter, this means that upon decreasing values for k_{SW} , $2U_{in} - U_{C_1}(0)$ increases for the charge phase and $(U_{in} + U_{C_1}(0)) - U_{C_2}(0)$ increases for the discharge phase. Finally, it is observed that the dependency of

η_{sp_up} upon the difference in values for C_1 and C_2 is far less significant than for the step-down variant of this converter. This follows from the fact that C_2 is charged by means of C_1 in series with U_{in} , in the discharge phase. This process is less lossy than charging a capacitor merely with another capacitor, as is done in the discharge phase of a series-parallel step-down converter.

Monolithic integration of the series-parallel step-up charge pump converter topology is, similar to its step-down variant, feasible. The common limitation for any given charge-pump is the fact that η_{SW} reaches its maximum at only in particular value of k_{SW} , which is 2 for this topology. In practical applications, where k_{SW} often needs to be variable, this might prove to be a limitation. Nevertheless, this could be overcome by using a gear-box topology. An overview of other charge-pump step-up topologies and a comparison, with respect to their required area for monolithic integration, is given in [Bre08]. These and other topologies will not be discussed in this work. Charge-pump step-up converters are proven to be feasible, for the purpose of monolithic integration [Bre09a, Bre09b]. Moreover, individual converter stages can achieve high values of η_{SW} , in the order of 80% and more. This is beneficial for converters that have a moderately low value (< 2) of k_{SW} [Bre09a]. However, when higher values (> 2) of η_{SW} are required different converters need to be cascaded, having a negative impact on the overall η_{SW} [Bre09b]. Finally, a potential drawback of this step-up topology is that it requires four switches, whereas some other topologies discussed in Sect. 3.2 require only two switches.

2.3 Inductive Type DC-DC Converters

The third way to achieve DC-DC voltage conversion is by means of inductive type DC-DC converters. This type of DC-DC converters belongs, together with the charge-pump DC-DC converters discussed in Sect. 2.2, to the group of switched-mode DC-DC converters. Inductive DC-DC converters consist of one or more inductor(s) and capacitor(s) and at least two switches.² In the galvanically separated variant of inductive DC-DC converters the inductor is replaced by a transformer, which can be seen as two, or more, mutually magnetically coupled inductors. A selection of inductive type DC-DC converter topologies is provided in Chap. 3.

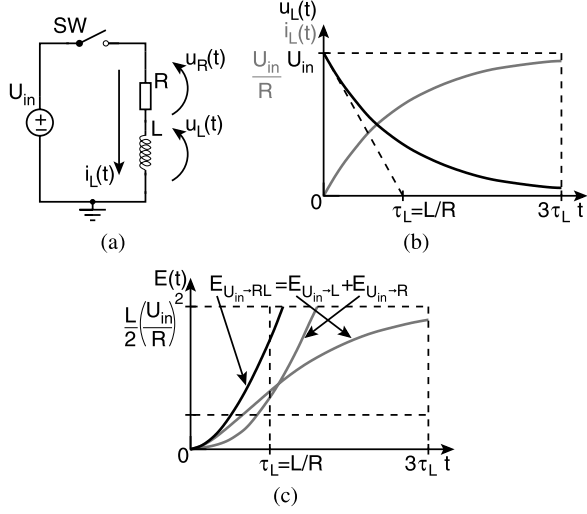
The basic theory for understanding the processes of storing energy by means of inductor and inductor-capacitor circuits is explained in the respective Sects. 2.3.1 and 2.3.2. The traditional calculation methods for the steady-state behavior of inductive type DC-DC converters are discussed in Sect. 2.3.3.

2.3.1 On Inductors

Unlike the charging of capacitors, discussed in Sect. 2.2.1, the process of charging inductors is not intrinsically lossy. In other words, the charging of an ideal induc-

²For DC-DC converters with off-chip components, one or more of the switches is often implemented as a diode. In doing so, the functionality of the converter is not altered.

Fig. 2.12 (a) The circuit for charging an inductor L in series with a resistor R by means of a voltage source U_{in} . (b) The voltage $u_L(t)$ over and the current $i_L(t)$ through L , as a function of time. (c) The energy $E_{U_{in} \rightarrow RL}(t)$ delivered by U_{in} , the energy $E_{U_{in} \rightarrow L}(t)$ stored in L and the energy $E_{U_{in} \rightarrow R}(t)$ dissipated in R , as a function of time



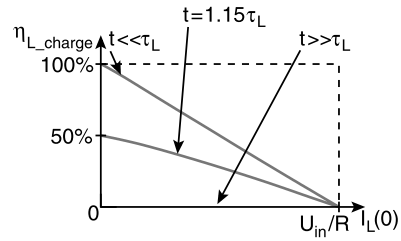
tor involves no energy loss. In order to understand the energy loss mechanism of charging non-ideal inductors, the circuit for charging an inductor L in series with a resistor R by means of a voltage source U_{in} is considered in Fig. 2.12(a). The voltage $u_L(t)$ and the current $i_L(t)$ through the inductor are plotted as a function of time t in Fig. 2.12(b). For these plots it is assumed that the initial current $i_L(0)$ through L is zero. $u_L(t)$ and $i_L(t)$ are calculated by means of (2.35) and (2.36), respectively. The time constant τ_L denotes the time where $u_L(t)$ and $i_L(t)$ reach 63% of their steady-state value. When a time equal to $3\tau_L$ is elapsed, $u_L(t)$ and $i_L(t)$ reach 95% of their steady-state value.

$$u_L(t) = (U_{in} - RI_L(0))e^{-\frac{t}{\tau_L}} \quad (2.35)$$

$$i_L(t) = \frac{U_{in}}{R} + \left(I_L(0) - \frac{U_{in}}{R} \right) e^{-\frac{t}{\tau_L}} \quad (2.36)$$

Figure 2.12(c) shows the energy $E_{U_{in} \rightarrow RL}(t)$ that is delivered by U_{in} , the energy $E_{U_{in} \rightarrow R}(t)$ that is dissipated in R and the energy $E_{U_{in} \rightarrow L}(t)$ that is stored in L as a function of time and for $I_L(0) = 0$. These energies are calculated by (2.37), (2.38) and (2.39), respectively, of which the results are not shown due to their complexity. It is observed that $E_{U_{in} \rightarrow R}(t)$ and $E_{U_{in} \rightarrow L}(t)$ are equal at a charging time t of about $1.15 \cdot \tau_L$. When $t < 1.15 \cdot \tau_L$, $E_{U_{in} \rightarrow L}(t)$ is larger than $E_{U_{in} \rightarrow R}(t)$, which is beneficial for the energy charging efficiency $\eta_{L_charge}(t)$ of the charging of an inductor. For a charging time $t > 1.15 \cdot \tau_L$, $E_{U_{in} \rightarrow R}$ becomes larger than $E_{U_{in} \rightarrow L}(t)$. The value of $E_{U_{in} \rightarrow R}(t)$ can be infinitely large, as $i_L(t)$ keeps flowing in steady-state, causing continuous Joule-losses in R . The value of $E_{U_{in} \rightarrow L}(t)$, on the other hand, saturates to a finite value in steady-state for a non-ideal inductor, where $0 < R < \infty$. The steady-state value of $E_{U_{in} \rightarrow L}(t)$ is calculated by applying the limit where $t/\tau_L \rightarrow \infty$, yielding (2.40). This equals (1.6), for $I_L(0) = 0$.

Fig. 2.13 The energy charging efficiency η_{L_charge} of an inductor with a series resistance charged by a voltage source U_{in} , as a function of the initial current $I_L(0)$ through the inductor, for three different charge time t



$$E_{U_{in} \rightarrow RL}(t) = \int_0^t U_{in} i_L(t) dt \quad (2.37)$$

$$E_{U_{in} \rightarrow R}(t) = \int_0^t u_R(t) i_L(t) dt \quad (2.38)$$

$$E_{U_{in} \rightarrow L}(t) = E_{U_{in} \rightarrow RL}(t) - E_{U_{in} \rightarrow R}(t) \quad (2.39)$$

$$\lim_{\frac{tR}{L} \rightarrow \infty} (E_{U_{in} \rightarrow L}(t)) = \frac{L}{2} \left(\left(\frac{U_{in}}{R} \right)^2 - I_L(0)^2 \right) \quad (2.40)$$

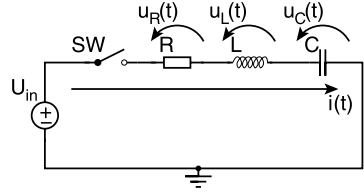
Obviously, the maximal energy that can additionally be stored in an inductor, given by (2.40), is not a practical value since it is associated with high losses in the (parasitic) series resistance. In order to gain a better idea of the relation between the stored and the dissipated energy, the energy charging efficiency $\eta_{L_charge}(t)$ is calculated by means of (2.41). The result of this calculation is not shown in its mathematical form, due to its rather complex nature. Therefore, (2.41) is graphically represented in Fig. 2.13, where $\eta_{L_charge}(t)$ is plotted as a function of $I_L(0)$, for three different cases of t : $t \ll \tau_L$, $t = 1.15 \cdot \tau_L$ and $t \gg \tau_L$.

$$\eta_{L_charge}(t) = \frac{E_{U_{in} \rightarrow L}(t)}{E_{U_{in} \rightarrow RL}(t)} = \frac{(2.39)}{(2.37)} \quad (2.41)$$

In Fig. 2.13 it is observed that, for equal values of $I_L(0)$, $\eta_{L_charge}(t)$ decreases upon increasing values of t . This was already concluded for the case where $I_L(0) = 0$, in Fig. 2.12(c). Furthermore, it can be seen that $\eta_{L_charge}(t)$ decreases as $I_L(0)$ increases, for a fixed value of t . This knowledge leads to the following conclusions for the charging of an inductor with a series resistance by means of a voltage source:

- The highest values $\eta_{L_charge}(t)$ are obtained at $t \ll \tau_L$, meaning that the charge time t of inductors should be minimized, thereby minimizing the resistive losses. However, as the value of t becomes smaller, for a certain constant value of τ_L , the energy $E_{U_{in} \rightarrow L}(t)$ stored in L becomes smaller as well, ultimately becoming infinitesimal.
- The value of $I_L(0)$ should be minimized and ideally be zero, in order to obtain the highest values for $\eta_{L_charge}(t)$.
- The charging of an ideal inductor, which has an infinitesimal series resistance, by means of a voltage source is lossless, regardless of the value of $I_L(0)$. The formal prove of this statement is omitted, but it can be intuitively understood by considering Fig. 2.13. If $R = 0$ then $\tau_L = \infty$ and as a consequence $t \ll \tau_L$, which

Fig. 2.14 The circuit for charging a series inductor L and a series capacitor C with a series resistor R , by means of a voltage source U_{in}



is illustrated by the upper curve. Moreover, the intersection with the X-axis U_{in}/R will be at infinity, implying that curve for $t \ll \tau_L$ will be parallel to the X-axis, intersecting the Y-axis at the value $\eta_{L_charge}(t) = 100\%$.

It is clear that inductors have an intrinsic advantage over capacitors for the purpose of storing energy out of a voltage source. Indeed, the process of charging capacitors can only reach a high value of $\eta_{C_charge}(t)$ if $U_{in} - U_C(0)$ is kept significantly smaller than U_{in} , regardless of the value of the parasitic series resistance. This is in contrast to the process of charging inductors, which can reach a high value of $\eta_{L_charge}(t)$ for any given value of U_{in} and $I_C(0)$, as long as the parasitic series resistance is kept small. Therefore, inductors are theoretically well suited for the purpose of DC-DC converters, as they allow for high power conversion efficiencies over a broad range of voltage conversion levels.

2.3.2 Inductors and Capacitors: The Combination

Any given switched-mode (inductive) DC-DC converter topology has an output capacitor to smooth out the current/voltage transients, generated by the switching part of the converter, and also to act as an energy reservoir for the load when the converter is not delivering power to the output. However, as the direct charging of a capacitor through a voltage source is intrinsically lossy (see Sect. 2.2.1), an inductor needs to be added to avoid these losses. This process of charging a capacitor C with a series inductor L through a voltage source U_{in} is illustrated in Fig. 2.14, where the series resistor R represents the sum of the parasitic series resistances of the voltage source U_{in} , the inductor L and the capacitor C . This circuit is described by its differential equation, which is omitted in this discussion. Its time-domain solution can be either aperiodically damped, critically damped or periodically damped. Only the latter case, for which (2.42) is valid, is considered in this discussion as the total parasitic series resistance in practical inductive DC-DC converters is always kept small enough to fulfill this requirement.

$$R \ll 2\sqrt{\frac{L}{C}} \quad (2.42)$$

For the periodically damped RLC -circuit, the current $i(t)$, the voltage $u_L(t)$ over L , the voltage $u_R(t)$ over R and the voltage $u_C(t)$ over C are given by (2.43),

(2.44),³ (2.45) and (2.46), respectively. In (2.43), $I_L(0)$ denotes the initial current, $U_C(0)$ is the initial voltage over C , ω_{LC} is the angular frequency and τ_{LC} is the time constant.

$$i(t) = (I_L(0)Q \cos(\omega_{LC}t) + (I_L(0)(R - 2LR) + 2(U_{in} - U_C(0))) \sin(\omega_{LC}t)) \cdot \frac{e^{-\frac{t}{\tau_{LC}}}}{Q} \quad (2.43)$$

$$\text{with } \begin{cases} Q = \sqrt{\frac{4L}{C} - R^2} \\ \tau_{LC} = \frac{2L}{R} \\ \omega_{LC} = \frac{Q}{2L} \end{cases}$$

$$u_L(t) = L \frac{di(t)}{dt} \quad (2.44)$$

$$u_R(t) = Ri(t) \quad (2.45)$$

$$u_C(t) = U_{in} - u_L(t) - u_R(t) \quad (2.46)$$

The current and the voltages of an ideal series RLC -circuit as a function of time are plotted in Fig. 2.15(a). In this figure it is assumed that the resistance of R is infinitesimal, $I_L(0) = 0$ and $U_C(0) = 0$. The most important observations in this plot are that the ideal series RLC -circuit oscillates undamped at an angular frequency $\omega_{LC} = 2\pi f = 2\pi/T$ and that the maximal voltage U_{C_max} over C is $2U_{in}$. For the non-ideal, periodically damped RLC -circuit, where R is non-zero and complies with (2.42), the current and voltages are plotted in Fig. 2.15(b), where it is also assumed that $I_L(0) = 0$ and $U_C(0) = 0$. This circuit oscillates at the same angular frequency ω_{LC} as its ideal counterpart, it is however damped with a time-constant τ_{LC} . In steady-state $i_L(t)$, $u_L(t)$ and $u_R(t)$ become zero and $u_C(t)$ becomes equal to U_{in} .

The energy $E_{U_{in} \rightarrow RLC}(t)$ delivered by U_{in} , the energies $E_L(t)$ stored in L , $E_R(t)$ dissipated in R and $E_C(t)$ stored in C are given by (2.47), (2.48), (2.49) and (2.50).

$$E_{U_{in} \rightarrow RLC}(t) = \int_0^t U_{in} i(t) dt \quad (2.47)$$

$$E_L(t) = \int_0^t u_L(t) i(t) dt \quad (2.48)$$

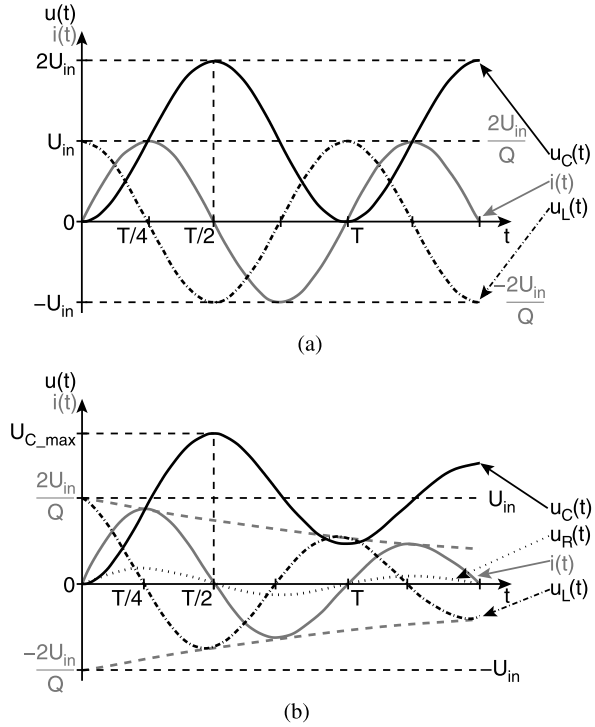
$$E_R(t) = \int_0^t u_R(t) i(t) dt \quad (2.49)$$

$$E_C(t) = \int_0^t u_C(t) i(t) dt \quad (2.50)$$

These energies are plotted in Fig. 2.16(a) for an ideal series RLC -circuit, where it is assumed that the resistance of R , $I_L(0)$ and $U_C(0)$ are zero. During the first

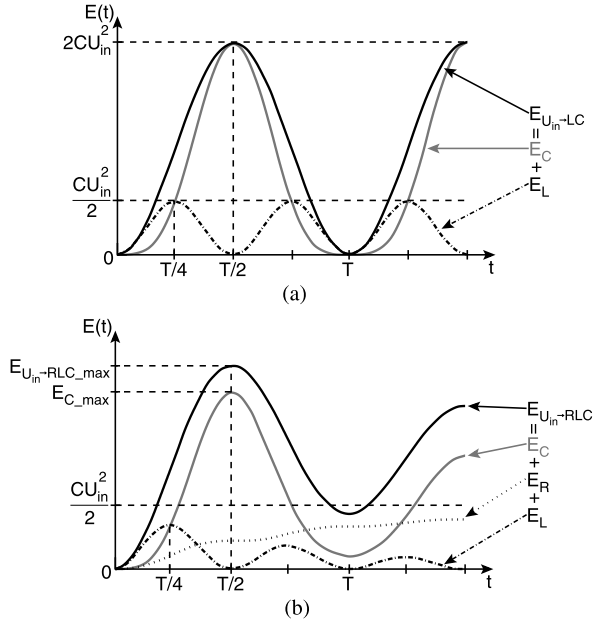
³This equation is known as Lenz's law.

Fig. 2.15 (a) The current $i(t)$, the voltage $u_L(t)$ over L , the voltage $u_R(t)$ over R and the voltage $u_C(t)$ over C as a function of time, for in ideal ($R = 0$) and (b) a non-ideal ($R \neq 0$) series RLC -circuit



one-fourth part of the period T energy from U_{in} is stored in L and C . Afterwards, during the following one-fourth part of T energy from both U_{in} and L are stored in C . Finally, during the last half part of T this process is repeated in reversed order and the cycle recommences. It can be seen that at exactly the half of T , $E_C(t)$ is maximal and equal to $E_{U_{in} \rightarrow RLC}(t)$, implying that the energy charging efficiency $\eta_{RLC_charge}(t)$, for charging a capacitor in an ideal series RLC -circuit by means of a voltage source, is equal to 100%. This is in contrast with the case where a capacitor is charged directly by a voltage source, where for the same case of a zero initial voltage ($U_C(0) = 0$) $\eta_{C_charge}(t) = 50\%$, as can be seen in Fig. 2.5(c). Moreover, in the latter case C is only charged to a voltage equal to U_{in} in steady-state, whereas for the ideal RLC -circuit C is charged to $2 \cdot U_{in}$ at $T/2$ and therefore contains four times more energy. Figure 2.16(b) shows the plotted energies of a periodically damped series RLC -circuit, where it is assumed that R complies to (2.42) and both $I_L(0)$ and $U_C(0)$ are zero. Similar to the current and voltages of this system, which are shown in Fig. 2.15(b), the oscillation of these energies is damped with the time-constant τ_{LC} . To gain insight into this circuit the steady-state region, where $t \gg \tau_{LC}$, is examined first. It can be intuitively seen that in steady-state $i(t)$ is zero, thus $E_L(t)$ will also be zero. The steady-state values of $E_{U_{in} \rightarrow RLC}(t)$, $E_C(t)$ and $E_R(t)$ are positive finite values given by (2.51), (2.52) and (2.53), respectively. For the specific cases where $I_L(0)$ and $U_C(0)$ are zero these energies are equal to those of a capacitor that is charged directly by means of a voltage source.

Fig. 2.16 (a) The energy $E_{U_{in} \rightarrow RLC}(t)$ delivered by U_{in} , the energy $E_L(t)$ stored in L , the energy $E_R(t)$ dissipated in R and the energy $E_C(t)$ stored in C as a function of time, for an ideal ($R = 0$) and (b) a non-ideal ($R \neq 0$) series RLC -circuit



$$\lim_{\frac{t}{T_{LC}} \rightarrow \infty} (E_{U_{in} \rightarrow RLC}(t)) = CU_{in}(I_L(0)R(1-L) - U_C(0) + U_{in})|_{I_C(0)=U_C(0)=0} \\ = CU_{in}^2 \quad (2.51)$$

$$\lim_{\frac{t}{T_{LC}} \rightarrow \infty} (E_C(t)) = \frac{C}{2}((I_L(0)R(1-L) - U_C(0))^2 + U_{in}^2)|_{I_C(0)=U_C(0)=0} \\ = \frac{CU_{in}^2}{2} \quad (2.52)$$

$$\lim_{\frac{t}{T_{LC}} \rightarrow \infty} (E_R(t)) = \frac{1}{2}(2RCI_L(0)(L-1)(U_C(0) - U_{in}) + C(U_C(0) - U_{in})^2 \\ + I_L(0)^2(L + R^2C(L-1)^2))|_{I_C(0)=U_C(0)=0} \\ = \frac{CU_{in}^2}{2} \quad (2.53)$$

The periodically-damped series RLC -circuit shows no advantage for charging a capacitor, in terms of $\eta_{RLC_charge}(t)$, in steady-state. Nevertheless, this advantage exists during specific moments of the transient region. When considering Fig. 2.16(b), it shows that the maximal $\eta_{RLC_charge}(t)$ will occur after the first half period $T/2$ has elapsed. This $\eta_{RLC_charge}(t)$ is calculated through (2.54), where the initial energy $E_L(0)$ stored in L is added to $E_{U_{in} \rightarrow RLC}(t)$ because $E_L(0)$ is added in a previous step that is not considered here. Only the solution for the special case where $I_L(0)$ and $U_C(0)$ are zero is shown, as the general solution of this calcula-

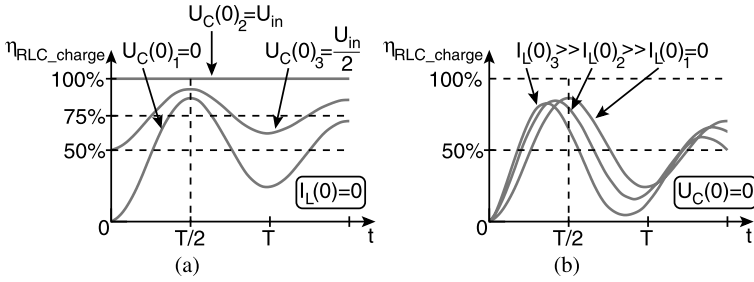


Fig. 2.17 (a) The energy charging efficiency $\eta_{RLC_charge}(t)$ of a capacitor in a periodically-damped series RLC -circuit as a function of time, for different values of the initial voltages $U_C(0)$ over C and (b) for different initial currents $I_L(0)$ through L

tion is too complex. When the resistance of R is infinitesimal, $\eta_{RLC_charge}(t)$ will be 100%.

$$\begin{aligned}
 \eta_{RLC_charge}\left(\frac{T}{2}\right) &= \eta_{RLC_charge}\left(\frac{2\pi L}{Q}\right) = \frac{E_C\left(\frac{2\pi L}{Q}\right)}{E_{U_{in} \rightarrow RLC}\left(\frac{2\pi L}{Q}\right) - E_L(0)} \\
 &= \frac{E_C\left(\frac{2\pi L}{Q}\right)}{E_{U_{in} \rightarrow RLC}\left(\frac{2\pi L}{Q}\right) + \frac{LI_L(0)^2}{2}} \Big|_{I_C(0)=U_C(0)=0} \\
 &= \frac{1 + e^{-\frac{\pi R}{Q}}}{2} \blacksquare
 \end{aligned} \tag{2.54}$$

The influence of the values of $U_C(0)$ and $I_L(0)$ on $\eta_{RLC_charge}(t)$ is graphically represented in Fig. 2.17(a) and (b). First, Fig. 2.17(a) is considered, where $\eta_{RLC_charge}(t)$ is plotted as a function of time. Also, the value of $I_C(0)$ is assumed to be zero and three different values of $U_C(0)$ are considered: $U_C(0)_1 = 0$, $U_C(0)_2 = U_{in}/2$ and $U_C(0)_3 = U_{in}$. It is observed that at time $T/2$ the maximum values of $\eta_{RLC_charge}(t)$ are reached and that these values increase upon increasing values of $U_C(0)$. For the case where $U_C(0) = U_{in}$, $\eta_{RLC_charge}(t)$ reaches the value of 100%. Obviously, no energy is added to C in this case. Please note that the maximum value of $\eta_{RLC_charge}(t)$ is also dependent on the resistance of R . This dependency is not shown for sake of simplicity. However, it can be proven that the maximum value of $\eta_{RLC_charge}(t)$ is inversely proportional to R . In order to gain more insight into the dependency of $\eta_{RLC_charge}(t)$ on $I_L(0)$, Fig. 2.17(b) is explained. In this figure $\eta_{RLC_charge}(t)$ is plotted as a function of time. The value of $U_C(0)$ is assumed to be zero and three different cases for $I_L(0)$ are considered: $I_L(0)_1 = 0 \gg I_L(0)_2 \gg I_L(0)_3$. In this figure is observed that the maximum value of $\eta_{RLC_charge}(t)$ is only reached at $T/2$ for the case where $I_L(0) = 0$. When $I_L(0) > 0$, the maximum value for $\eta_{RLC_charge}(t)$ is reached faster than $T/2$. It can also be seen that this maximum value tends to decrease upon increasing values of $I_L(0)$, which is associated with increasing Joule-losses in R . Finally, it is noted that, similar to Fig. 2.17(a), the maximum value of $\eta_{RLC_charge}(t)$ is inversely proportional to R .

To conclude this dissertation on the charging of capacitors in a periodically-damped RLC -circuit by means of a voltage source, the most important observations and their consequences are listed:

- The maximum value of $\eta_{RLC_charge}(t)$ is reached at a charge time t exactly equal to $T/2$, assuming that $I_L(0)$ is zero.
- The total parasitic series resistance R is inversely proportional to $\eta_{RLC_charge}(t)$ and $\eta_{RLC_charge}(t)$ reaches the value of 100% for $R = 0$, independent of the values of $U_C(0)$ and $I_L(0)$. This implies that the charging of a capacitor in an ideal RLC -circuit ($R = 0$) is lossless, as opposed to the charging of a capacitor by means of a voltage source.
- The maximal $E_C(t)$ is ideally four times larger than for a capacitor charged by means of a voltage source, implying that $u_C(t)$ can reach the maximum value of $2 \cdot U_{in}$.
- The smaller the difference between the values of U_{in} and $U_C(0)$, the larger the maximum value of $\eta_{RLC_charge}(t)$, reaching 100% for the case where $U_C(0) = U_{in}$. Obviously for the latter case $E_C(t)$ is zero.
- A smaller value of $I_L(0)$ yields a larger maximum value for $\eta_{RLC_charge}(t)$.

As both the charging of inductors by means of a voltage source and the charging of capacitors in periodically-damped series RLC -circuits by means of a voltage source can ideally be lossless, their combination is promising for the realization of inductive DC-DC voltage converters. The result of this is that ideal inductive DC-DC converters are able to achieve power conversion efficiencies η_{SW} of 100% for their entire voltage conversion ratio k_{SW} range, which is in contrast to ideal charge-pump DC-DC converters, which is explained in Sect. 2.2.

2.3.3 Reflections on Steady-State Calculation Methods

The behavior of ideal inductive DC-DC converters in terms of the voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ and the conduction mode (CM) is discussed in this section. For this purpose the general small-ripple approximation method is provided here [Eri04]. The method is explained by means of an ideal boost DC-DC converter, which is shown in Fig. 2.18(a), but can be used for any given inductive DC-DC converter topology. As this method is only useful for calculations of ideal converters, it will prove to be of limited value in the design of monolithic inductive DC-DC converters. An accurate model for this purpose is provided in Sect. 4.

Continuous Conduction Mode

First, the basic steady-state operation of an ideal boost converter, shown in Fig. 2.18, is explained. In continuous conduction mode (CCM) the current through the inductor $i_L(t)$ has a finite, positive value which is not zero and the operation mode consists of two phases:

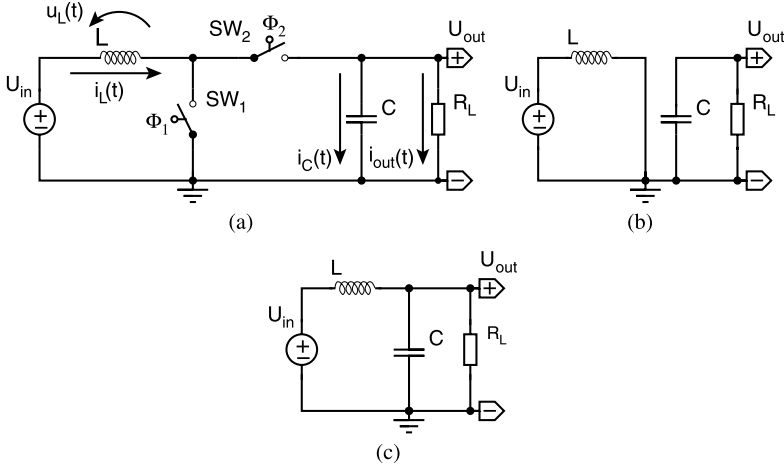


Fig. 2.18 (a) The circuit of an ideal boost DC-DC converter. (b) The equivalent circuit of the inductor charge phase and (c) the inductor discharge phase

1. *The inductor charge phase Φ_1* : The equivalent circuit for Φ_1 is shown in Fig. 2.18(b), which is achieved by closing SW_1 and opening SW_2 for a certain on-time t_{on} . During Φ_1 the inductor L is charged by the voltage source U_{in} , causing the inductor current $i_L(t)$ to increase from its minimal value I_{L_min} to its maximal value I_{L_max} , as illustrated in Fig. 2.20. Simultaneously the output capacitor C is discharged through the load R_L .
2. *The inductor discharge phase Φ_2* : The equivalent circuit for Φ_2 is shown in Fig. 2.18(c), which is achieved by opening SW_1 and closing SW_2 for a certain off-time t_{off} . During Φ_2 L is discharged into C and R_L , causing $i_L(t)$ to decrease from I_{L_max} to I_{L_min} , as can be seen in Fig. 2.20. As a result $i_L(t)$ is divided over C and R_L , thereby charging C and providing power to R_L .

Because L is discharged in series with U_{in} it can be intuitively seen that the output voltage U_{out} will always be higher than U_{in} . This will be formally proven by means of the small-ripple approximation method. For this method it is assumed that:

- All the converter components are ideal and lossless.
- The output voltage ripple $U_{out_max} - U_{out_min} = \Delta U_{out}$ is infinitesimal, which implies that U_{out} is equal to its mean value \bar{U}_{out} .
- The inductor current ripple $\Delta I_L = I_{L_max} - I_{L_min}$ is infinitesimal.
- All the currents and voltages are linearized, according to Fig. 2.20.
- The converter operates in steady-state.

First, the voltage $u_L(t)$ over L is considered. In Fig. 2.20 it can be seen that, for Φ_1 and Φ_2 , $u_L(t)$ is given by (2.61).

$$\begin{cases} \Phi_1 : 0 \rightarrow t_{on} & \Rightarrow & u_L(t) = U_{in} \\ \Phi_2 : t_{on} \rightarrow t_{off} & \Rightarrow & u_L(t) = U_{in} - U_{out} \end{cases} \quad (2.61)$$

⊗ CAPACITOR CHARGE BALANCE & INDUCTOR VOLT-SECOND BALANCE

For a capacitor C in a DC-DC converter, operating in steady-state, the energy E_{C_in} stored in it is equal to the energy E_{C_out} delivered by it, as stated by (2.55). Because the capacitance of C is constant, the net voltage change, during one period T , over C is zero. This is translated into (2.56), where $U_C(0)$ and $U_C(T)$ are the respective voltages over C at the beginning and end of T . For the example of Fig. 2.19(b), where the current $i_C(t)$ through C as a function of time is shown, this yields (2.56). This implies that the stored Q_{in} and the delivered charge Q_{out} in C are equal, hence the capacitor charge is in balance. Graphically, the positive area A_C^+ of Fig. 2.19(b) is equal to the negative area A_C^- .

$$E_{C_in} - E_{C_out} = \frac{CU_C(T)^2}{2} - \frac{CU_C(0)^2}{2} = 0 \quad (2.55)$$

$$\Rightarrow U_C(T) - U_C(0) = 0 = \frac{1}{C} \int_0^T i_C(t) dt \quad (2.56)$$

$$\Rightarrow \int_0^T i_C(t) dt = I_{C1}t_1 + I_{C2}t_2 = Q_{in} - Q_{out} = A_C^+ - A_C^- \blacksquare \quad (2.57)$$

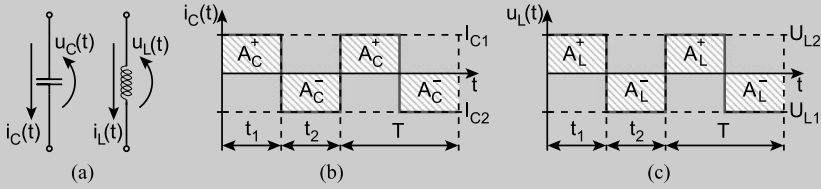


Fig. 2.19 (a) The convention of the voltage over and the current through a capacitor C and an inductor L . (b) The current $i_C(t)$ through C and (c) the voltage $u_L(t)$ over L , both in energetic equilibrium

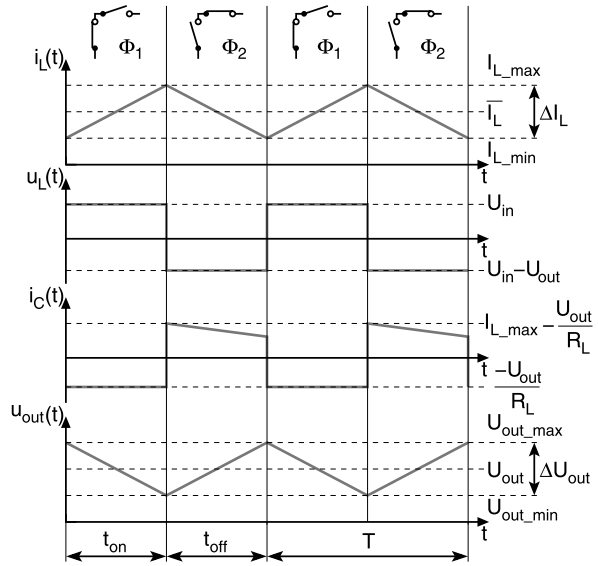
For an inductor L in a DC-DC converter, operating in steady-state, the energy E_{L_in} stored in it is equal to the energy E_{L_out} delivered by it, as stated by (2.58). Because the inductance of L is constant, the net current change, during one period T , through L is zero. This is translated into (2.59), where $I_L(0)$ and $I_L(T)$ are the respective currents through L at the beginning and end of T . For the example of Fig. 2.19(c), where the voltage $u_L(t)$ over L as a function of time is shown, this yields (2.60). This implies that the inductor's volt-second product is in balance. Graphically, the positive area A_L^+ of Fig. 2.19(c) is equal to the negative area A_L^- .

$$E_{L_in} - E_{L_out} = \frac{LI_L(T)^2}{2} - \frac{LI_L(0)^2}{2} = 0 \quad (2.58)$$

$$\Rightarrow I_L(T) - I_L(0) = 0 = \frac{1}{L} \int_0^T u_L(t) dt \quad (2.59)$$

$$\Rightarrow \int_0^T u_L(t) dt = U_{L1}t_1 + U_{L2}t_2 = A_L^+ - A_L^- \blacksquare \quad (2.60)$$

Fig. 2.20 The linearized current $i_L(t)$ through L , the linearized voltage $u_L(t)$ over L , the linearized current $i_C(t)$ through C and the linearized output voltage $u_{out}(t)$ as a function of time, for an ideal boost converter in CCM



In steady-state operation the net energy change in the inductor over one switching period T is zero, thus the volt-second balance of the inductor is also zero. This yields (2.62), giving the voltage conversion ratio $k(\delta)$ as a function of the duty cycle δ . It is observed that $k(\delta)$ only depends on δ and not on the load R_L or the switching frequency f_{SW} . This follows from the fact that the converter components are assumed to be ideal. Another implication of this assumed ideality is that the power conversion efficiency η_{SW} will always be 100%, independent of the converter's operation parameters. Therefore, (2.62) will prove little value in the design process, it can however be used to understand the operation principle. A more accurate design model for a boost converter will be deduced in Chap. 4.

$$\int_0^T u_L(t) dt = U_{in}t_{on} + (U_{in} - U_{out})t_{off} = 0$$

$$\Rightarrow k(\delta) = \frac{U_{out}}{U_{in}} = \frac{t_{on} + t_{off}}{t_{off}} = \frac{1}{1 - \delta} \quad \blacksquare \quad (2.62)$$

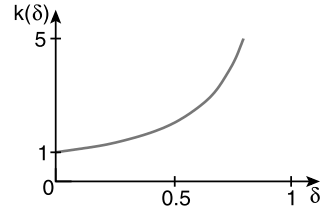
The duty-cycle δ is defined by (2.63).

$$\delta = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} \quad \text{with} \quad 0 \leq \delta \leq 1 \quad (2.63)$$

The relation between δ and $k(\delta)$, given by (2.62), is graphically represented in Fig. 2.21. It can be seen that U_{out} is always higher than U_{in} , as explained earlier. Also, U_{out} can be infinitely high, as δ approaches to 1. In practical implementations the maximum value of U_{out} will naturally be limited by losses.

The small-ripple approximation, used to calculate $k(\delta)$, assumes that the output ripple voltage ΔU_{out} is infinitesimal. This is obviously not the case when the values of L , C and f_{SW} are not infinitely large, even when the converter components are

Fig. 2.21 The voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ , for an ideal boost converter in CCM



assumed ideal. Therefore, the calculation of ΔU_{out} is also performed. In Fig. 2.20 it can be seen that during Φ_1 C is discharged through R_L . If $t_{on} \ll \tau_C = CR_L$ the discharge current $i_C(t)$ of C can be approximated to have a constant value, which is formally described by (2.64).

$$\Phi_1 : 0 \rightarrow t_{on} \implies i_C(t) = C \frac{du_{out}(t)}{dt} = -\frac{\overline{U_{out}}}{R_L} \quad (2.64)$$

Thus, the net change of $u_{out}(t)$ follows from the integration of $i_C(t)$. The result of this calculation yields ΔU_{out} , which is given by (2.65).

$$\Delta U_{out} = -\frac{1}{C} \int_0^{t_{on}} i_C(t) dt = \frac{\overline{U_{out}}}{CR_L} t_{on} = \frac{\overline{I_{out}}}{C} t_{on} \blacksquare \quad (2.65)$$

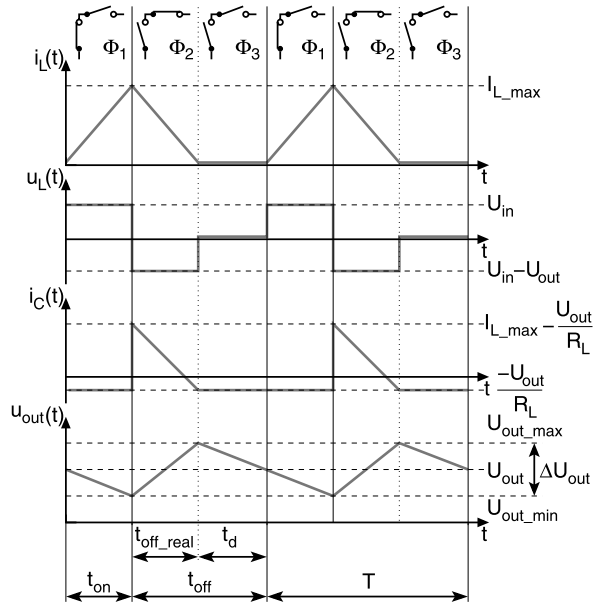
From (2.65) it follows that ΔU_{out} will increase upon decreasing R_L , which is equal to an increasing mean output current $\overline{I_{out}}$, because C is discharged faster during Φ_1 . ΔU_{out} will also increase upon increasing values of t_{on} , as this is equal to the discharge time of C . Furthermore, it is observed that ΔU_{out} is inversely proportional to the capacitance of C and independent of the inductance of L . The fact that there is no dependency on L can be intuitively understood because it is not a part of the output filter. For DC-DC converters where both L and C are a part of the output filter, this method for calculating ΔU_{out} will not be applicable. The alternative method, which is based on the charge balance of C , is explained for the DC-DC buck converter in Sect. 3.1.

Discontinuous Conduction Mode

In discontinuous conduction mode (DCM) $i_L(t)$ varies between zero and a finite positive value. In other words, $i_L(t)$ does not flow continuously. The small-ripple approximation method, for analyzing the voltage conversion ratio k_{SW} of a DC/DC converter, is somewhat more complex for DCM. Before elaborating upon this method for the ideal boost DC-DC converter example, of which the circuit is shown in Fig. 2.18(a), the three phases of this converter in DCM are explained:

1. *The inductor charge phase Φ_1* : The equivalent circuit for Φ_1 is shown in Fig. 2.18(b), which is achieved by closing SW_1 and opening SW_2 for a certain on-time t_{on} . During Φ_1 L is charged by U_{in} , causing $i_L(t)$ to increase from zero to I_{L_max} , as illustrated in Fig. 2.22. Simultaneously C is discharged through R_L .

Fig. 2.22 The linearized current $i_L(t)$ through L , the linearized voltage $u_L(t)$ over L , the linearized current $i_C(t)$ through C and the linearized output voltage $u_{out}(t)$ as a function of time, for an ideal boost converter in DCM



2. *The inductor discharge phase Φ_2* : The equivalent circuit for Φ_2 is shown in Fig. 2.18(c), which is achieved by opening SW_1 and closing SW_2 for a certain real off-time t_{off_real} . This t_{off_real} is the exact duration for $i_L(t)$ to reach the value zero, which is shown in Fig. 2.22. Thus, during t_{off_real} L is discharged into C and R_L , thereby charging C and providing power to R_L .
3. *The dead-time phase Φ_3* : The equivalent circuit for Φ_3 is illustrated by the right-hand part of Fig. 2.18(b), which is achieved by both opening SW_1 and SW_2 for a certain dead-time t_d . This prevents $i_L(t)$ to become negative, discharging C into U_{in} . Thus, during Φ_3 C is discharged through R_L . Finally, it is noted that the sum of t_{off_real} and t_d equals t_{off} .

Due to the fact that, in DCM, $i_L(t)$ is zero during t_d , it cannot be approximated as an infinitesimal small-ripple. For this reason the calculation method for $k(\delta)$ in CCM, which was described earlier, will not suffice for DCM. Therefore, the calculation method for the latter mode, by means of the small-ripple approximation, method is explained. The same assumptions as for CCM are made for this calculation, except for the inductor current ripple $\Delta I_L = I_{L_max} - I_{L_min} = I_{L_max}$, which cannot be considered infinitesimal.

First, the voltage $u_L(t)$, which is plotted in Fig. 2.22, is considered. For Φ_1 , Φ_2 and Φ_3 this yields (2.66).

$$\begin{cases} \Phi_1 : 0 \rightarrow t_{on} & \Rightarrow & u_L(t) = U_{in} \\ \Phi_2 : t_{on} \rightarrow t_{off_real} & \Rightarrow & u_L(t) = U_{in} - U_{out} \\ \Phi_3 : t_{off_real} \rightarrow t_{off} & \Rightarrow & u_L(t) = 0 \end{cases} \quad (2.66)$$

In order to determine the current $i_C(t)$, an expression for $i_L(t)$ is needed. Both these currents are plotted for DCM in Fig. 2.22. By means of Lenz's law (2.44) the tangents of $i_L(t)$ during Φ_1 and Φ_2 are calculated, as stated in (2.67).

$$\begin{cases} \Phi_1 : 0 \rightarrow t_{on} & \Rightarrow \frac{di_L(t)}{dt} = \frac{U_{in}}{L} \\ \Phi_2 : t_{off_real} \rightarrow t_{off} & \Rightarrow \frac{di_L(t)}{dt} = \frac{U_{in} - U_{out}}{L} \end{cases} \quad (2.67)$$

The linear approximation of $i_L(t)$ during Φ_2 is calculated by (2.67), yielding (2.68).

$$\begin{aligned} \Phi_2 : t_{off_real} \rightarrow t_{off} & \Rightarrow i_L(t) = I_{L_max} + \frac{U_{in} - U_{out}}{L} t \\ & = \frac{U_{in}}{L} t_{on} + \frac{U_{in} - U_{out}}{L} t \end{aligned} \quad (2.68)$$

By means of Fig. 2.22 and (2.68), $i_C(t)$ is calculated by (2.69), for Φ_1 , Φ_2 and Φ_3 .

$$\begin{cases} \Phi_1 : 0 \rightarrow t_{on} & \Rightarrow i_C(t) = -\frac{U_{out}}{R_L} \\ \Phi_2 : t_{on} \rightarrow t_{off_real} & \Rightarrow i_C(t) = i_L(t) - \frac{U_{out}}{R_L} \\ & = \frac{U_{in}}{L} t_{on} + \frac{U_{in} - U_{out}}{L} t - \frac{U_{out}}{R_L} \\ \Phi_3 : t_{off_real} \rightarrow t_{off} & \Rightarrow i_C(t) = -\frac{U_{out}}{R_L} \end{cases} \quad (2.69)$$

Analogue to CCM, the volt-second balance of L in DCM is zero when the converter operates in steady-state. This volt-second balance, in combination with (2.66) for $i_L(t)$, is used to calculate $k(\delta)$, yielding (2.70).

$$\begin{aligned} \int_0^T u_L(t) dt &= U_{in} t_{on} + (U_{in} - U_{out}) t_{off_real} = 0 \\ \Rightarrow k(\delta) &= \frac{U_{out}}{U_{in}} = \frac{t_{on} + t_{off} - t_d}{t_{off} - t_d} \end{aligned} \quad (2.70)$$

The dead-time t_d in (2.70) is an unknown output parameter and therefore an additional equation is needed to substitute it with known input parameters. For this purpose the charge balance of C is calculated, which is zero when the converter operates in its steady-state region. This is achieved by using (2.69) for $i_C(t)$, yielding (2.71) which is a quadratic equation of t_d . Solving t_d out of this quadratic equation results in two solutions, of which only the positive solution has a physical meaning.

$$\begin{aligned} \int_0^T i_C(t) dt &= 0 \\ &= -\frac{U_{out}}{R_L} t_{on} + \left(\left(\frac{U_{in}}{L} t_{on} - \frac{U_{out}}{R_L} \right) (t_{off} - t_d) \right. \\ &\quad \left. + \frac{U_{in} - U_{out}}{2L} (t_{off} - t_d)^2 \right) - \frac{U_{out}}{R_L} t_d \end{aligned} \quad (2.71)$$

In the last step $k(\delta)$ is calculated by substituting the positive solution for t_d of (2.71) into (2.70). This results in a quadratic equation of U_{out} . The positive, physical relevant, solution of this equation yields $k(\delta)$, given by (2.72).

$$k(\delta) = \frac{U_{out}}{U_{in}} = \frac{1 + \sqrt{1 + \frac{2R_L}{L(t_{on} + t_{off})} t_{on}^2}}{2} = \frac{1 + \sqrt{1 + \frac{4\delta^2}{\frac{2L}{R_L T}}}}{2} \quad \blacksquare \quad (2.72)$$

It is observed that $k(\delta)$ is not independent of the value of R_L , L and T in DCM. This stands in contrast to CCM where $k(\delta)$, given by (2.62), is only dependent on δ . However, both equations do not provide any information on whether the converter operates continuous or DCM and therefore it is not yet clear when to use which equation. The formal method to determine the CM for an ideal converter and a graphic representation of (2.72) is provided in the following section.

The output voltage ripple ΔU_{out} for DCM is calculated analogue to CCM. This ripple is assumed to be infinitesimal for the small-ripple approximation method, which is not the case when the values of L , C and f have a finite value. For this purpose $i_C(t)$ is considered during Φ_3 and Φ_1 , as illustrated in Fig. 2.22. During Φ_3 and Φ_1 C is discharged through R_L . Thus, for the case where $t_{on} + t_d \ll \tau_C = CR_L$ the discharge current $i_C(t)$ of C can be approximated to be constant, as described by (2.73).

$$\Phi_3 \text{ \& \; } \Phi_1 : 0 \rightarrow t_{on} + t_d \implies i_C(t) = C \frac{du_{out}(t)}{dt} = -\frac{\overline{U_{out}}}{R_L} \quad (2.73)$$

Analogue to (2.65), for CCM, ΔU_{out} is calculated by integrating $i_C(t)$ over $t_{on} + t_d$, yielding (2.73). The dead-time t_d is calculated by solving the quadratic equation (2.71).

$$\begin{aligned} \Delta U_{out} &= -\frac{1}{C} \int_0^{t_{on} + t_d} i_C(t) dt \\ &= \frac{\overline{U_{out}}}{CR_L} (t_{on} + t_d) = \frac{\overline{I_{out}}}{C} (t_{on} + t_d) \\ &= \left(t_{on} + \frac{R_L T U_{in} - R_L t_{off} \overline{U_{out}} + \sqrt{R_L (R_L t_{on}^2 U_{in}^2 + 2LT (U_{in} - \overline{U_{out}}) \overline{U_{out}})}}{R_L (U_{in} - \overline{U_{out}})} \right) \cdot \frac{\overline{I_{out}}}{C} \quad \blacksquare \end{aligned} \quad (2.74)$$

As can be seen, in DCM ΔU_{out} is dependent on the same parameters as for CCM, which is described by (2.65), in addition of t_d . As a consequence ΔU_{out} is also dependent on the inductance of L , which is not the case for CCM. This dependency of L is not expected because L is not a part of the output filter, however the dependency follows from the fact that t_d is dependent on L . This dependency is quite complex and it is more interesting to understand that the inductance of L influences the duration of t_d . An increasing value of t_d , meaning that the converter is driven

deeper into DCM, will increase the discharge time of C and as a result the value of ΔU_{out} will increase. An insight into the boundary between the two conduction modes is required to clarify this, which is provided in the next section. Finally, it is noticed that, similar to CCM, this calculation method will not be applicable for DC-DC converters where L is also a part of the output filter. For this type of converters the charge balance method, explained in Sect. 3.1 for a DC-DC buck converter, will be required.

Continuous-Discontinuous Boundary

The calculation of $k(\delta)$ and ΔU_{out} for both CMs of an ideal boost converter, shown in Fig. 2.18(a), is already performed in the previous sections, by using the small-ripple approximation method. This same method is used in this section to determine the conduction boundary (CB) between CCM and DCM, for the ideal boost converter example. The conditions for the converter to work in either of the two modes are found by means of Fig. 2.20 and are given by (2.75), where $\overline{I_L}$ is the mean value of $i_L(t)$.

$$\begin{cases} \overline{I_L} > \frac{I_{L_max} - I_{L_min}}{2} = \frac{\Delta I_L}{2} & \implies \text{CCM} \\ \overline{I_L} < \frac{I_{L_max} - I_{L_min}}{2} = \frac{\Delta I_L}{2} & \implies \text{DCM} \end{cases} \quad (2.75)$$

In order to find an expression for $\overline{I_L}$, the charge balance for C in CCM is to be solved. For this purpose, $i_C(t)$ for Φ_1 and Φ_2 is determined by means of the graph in Fig. 2.20, yielding (2.76).

$$\begin{cases} \Phi_1 : 0 \rightarrow t_{on} & \implies i_C(t) = -\frac{U_{out}}{R_L} \\ \Phi_2 : t_{on} \rightarrow t_{off} & \implies i_C(t) = i_L(t) - \frac{U_{out}}{R_L} \end{cases} \quad (2.76)$$

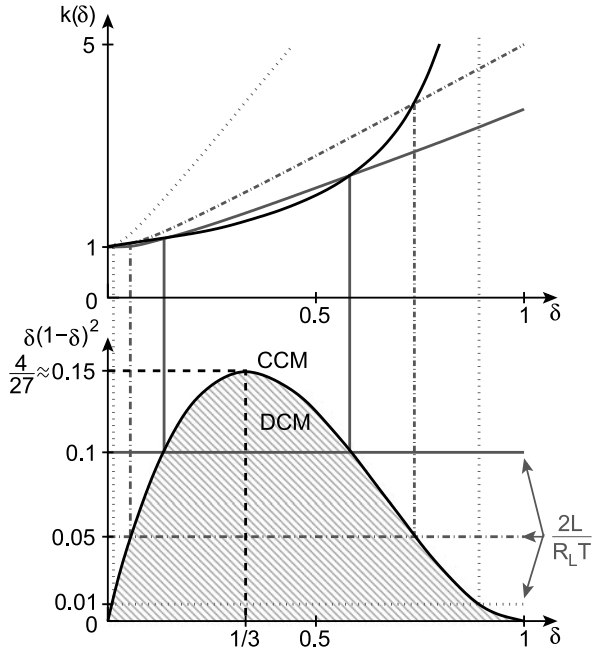
When assuming that ΔI_L is infinitesimal, which is the case for the small-ripple approximation, it can be seen that $i_L(t)$ equals $\overline{I_L}$. Thus, solving the charge balance of C and substituting $\overline{I_L}$, yields (2.77).

$$\begin{aligned} \int_0^T i_C(t) dt &= -\frac{U_{out}}{R_L} t_{on} + \left(\overline{I_L} - \frac{U_{out}}{R_L} \right) t_{off} = 0 \\ \implies \overline{I_L} &= \frac{U_{out}}{R_L} \cdot \frac{t_{on} + t_{off}}{t_{off}} = \frac{U_{out}}{R_L(1 - \delta)} \end{aligned} \quad (2.77)$$

Substituting the unknown output parameter U_{out} out of (2.62) and replacing it in (2.77) results in (2.78), which is only dependent on known input parameters.

$$\overline{I_L} = \frac{U_{in}}{R_L(1 - \delta)^2} \quad (2.78)$$

Fig. 2.23 The upper graph shows the voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ , where the black curve is valid for CCM and the gray curves for DCM. In the lower graph the black curve shows the boundary between the two CMs and the gray curves illustrate three numerical examples. These graphs are valid for an ideal DC-DC boost converter



The inductor current-ripple ΔI_L is equal to the current increase of $i_L(t)$ during Φ_1 . By using (2.67), this results in (2.79).

$$\Phi_1 : 0 \rightarrow t_{on} \implies \frac{di_L(t)}{dt} = \frac{U_{in}}{L} \implies \Delta I_L = \frac{U_{in}}{L} t_{on} = \frac{U_{in}}{L} T \delta \quad (2.79)$$

Finally, the condition for CCM of (2.75) can be reformulated into (2.80), by means of (2.78) and (2.79).

$$\begin{aligned} \overline{I_L} > \frac{\Delta I_L}{2} &\iff \frac{U_{in}}{R_L(1-\delta)^2} > \frac{U_{in}}{2L} T \delta \\ &\iff \frac{2L}{R_L T} > \delta(1-\delta)^2 \blacksquare \end{aligned} \quad (2.80)$$

It can be seen that the CM of an ideal DC-DC boost converter depends on the duty-cycle δ , the switching period T , the inductance of L and the load R_L . The boost converter will tend to operate in DCM for low inductances L , high values of the load resistance R_L (low loads) or longer switching periods T (lower frequencies f). Furthermore, the CM does not depend on the capacitance of C .

To get more insight into this matter, the CB is plotted in Fig. 2.23. The upper graph shows $k(\delta)$ as a function of δ , where the black curve is valid for CCM (2.62) and the gray curves for DCM (2.72). The curves for discontinuous mode are plotted for three different values of $(2L)/(R_L T)$: 0.01, 0.05 and 0.1. The CM valid for the upper graph is determined by the lower graph. In this graph the CB (2.80) is plotted by the black curve. The gray horizontal lines are the values for $(2L)/(R_L T)$, used in the upper graph. For the values of δ , at a certain value of $(2L)/(R_L T)$, which are

underneath the black CB curve, the converter will operate in DCM and vice versa. From these graphs it can also be concluded that the converter will tend to operate towards CCM for values of δ approaching zero or one. Finally, it is noted that in DCM $k(\delta)$ is quasi linear dependent on δ . This is due to the fact that the $i_L(t)$ will rise in a linear fashion during Φ_1 , according to (2.67), and therefore the amount of energy $E_L(t)$ stored in L will increase quadratically with δ , as determined by (1.6). The amount of energy delivered to R_L also increases quadratically with U_{out} and because this energy is equal to $E_L(t)$, U_{out} increases linear with δ .

The mathematical expressions obtained for the characterization of an ideal DC-DC boost converter will be validated with SPICE simulations in Sect. 3.2.1. A more sophisticated and accurate model, that takes all the significant losses of a monolithic DC-DC boost converter into account, is derived in Chap. 4.

2.4 INTERMEZZO: The Efficiency Enhancement Factor

Virtually any given energy converter has the purpose of performing its task with minimal energy losses.⁴ For DC-DC converters this is translated into maximizing the overall power conversion efficiency η , as stated by (1.3). The advantages of attaining the highest possible η are obvious:

- Less energy consumption leads to longer battery autonomies and lower energy costs, hence greener applications.
- Less heat dissipation leads to smaller required contact surfaces and/or heatsinks, in turn resulting into smaller and more cost efficient applications.
- Less heat dissipations leads to reduced conduction losses in metals and (MOS) transistors, due to Positive Temperature Coefficient (PTC) resistive behavior.

This section describes the formal method for comparing switched DC-DC step-down converters with each other, with respect to their power conversion efficiency η_{SW} . In order to achieve this, a new figure of merit is introduced [Wen08a]: The Efficiency Enhancement Factor (*EEF*). The method takes the voltage conversion ratio k_{SW} into account, which is a crucial parameter for the comparison.

The basic idea behind the *EEF* is explained in Sect. 2.4.1 and the possible interpretations and variations of this figure of merit are described in Sect. 2.4.2.

2.4.1 The Concept

Consider two switched-mode DC-DC step-down converters DC-DC₁ and DC-DC₂, having both the same P_{out} , a different k_{SW} and η_{SW} . The value of these parameters

⁴By referring to energy losses the energy converter is implicitly regarded as an open system, where the energy losses are in the form of waste/dissipated heat (Joule-losses).

Table 2.1 A comparison to clarify the concept of the *EEF* figure of merit for step-down DC-DC converters. Each comparison is made between a linear series voltage converter and a switched DC-DC step-down voltage converter, having the same voltage conversion ratio $k_{lin} = k_{SW}$

DC-DC ₁		DC-DC ₂	
$P_{out} = 1 \text{ W}$	$k_{lin} = k_{SW} = 0.8$	$P_{out} = 1 \text{ W}$	$k_{lin} = k_{SW} = 0.5$
$\eta_{lin} = 80\%$	$\eta_{SW} = 85\%$	$\eta_{lin} = 50\%$	$\eta_{SW} = 55\%$
$\Rightarrow \Delta\eta = \eta_{SW} - \eta_{lin} = 5\%$		$\Rightarrow \Delta\eta = \eta_{SW} - \eta_{lin} = 5\%$	
$P_{in_lin} = 1.25 \text{ W}$	$P_{in_SW} = 1.18 \text{ W}$	$P_{in_lin} = 2 \text{ W}$	$P_{in_SW} = 1.82 \text{ W}$
$\Rightarrow \Delta P_{in} = P_{in_lin} - P_{in_SW} = 0.07 \text{ W}$		$\Rightarrow \Delta P_{in} = P_{in_lin} - P_{in_SW} = 0.18 \text{ W}$	
$EEF = \frac{\Delta P_{in}}{P_{in_lin}} \Big _{k_{lin}=k_{SW}} = 5.6\%$		$EEF = \frac{\Delta P_{in}}{P_{in_lin}} \Big _{k_{lin}=k_{SW}} = 9\%$	

is listed in Table 2.1. At first glance DC-DC₁ is superior to DC-DC₂, in terms of η_{SW} .

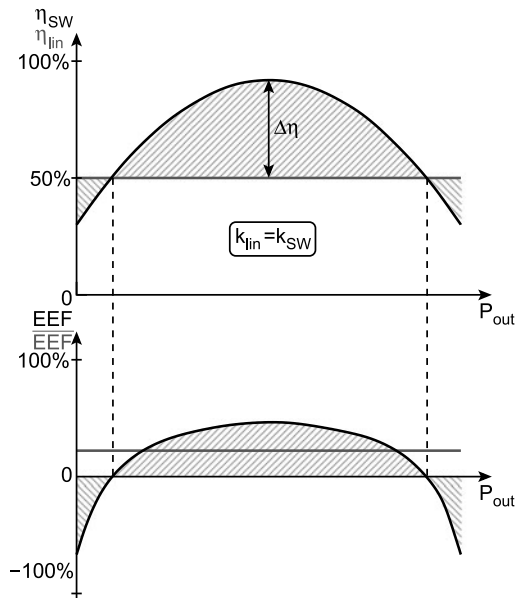
In order to examine this more closely, both converters are compared to their ideal series linear voltage converter equivalents, having the same voltage conversion ratios $k_{lin} = k_{SW}$ and P_{out} . The power conversion efficiency η_{lin} of these ideal linear series voltage converters is equal to k_{lin} and independent of P_{out} , which is proven by (2.2). For both examples this yields the same difference $\Delta\eta$ of power conversion efficiencies. From this point of view it is already clear that DC-DC₁ is not better than DC-DC₂, with regard to η_{SW} .

The main question still to be answered is how the improvement of the switched-mode DC-DC converters, compared to their linear series voltage converter equivalents, can be measured. In essence, it all comes down to P_{in} , which is larger than P_{out} due to the losses in a real converter. Thus, the input power P_{in_SW} of DC-DC₁ and DC-DC₂ is to be compared to the input power P_{in_lin} of their respective linear series converter equivalents, which is done by means of their difference ΔP_{in} . When comparing ΔP_{in} for both examples, it can be seen that this difference is smaller for DC-DC₁ than for DC-DC₂. This indicates that the net gain over a linear series voltage converter, in terms of P_{in} , has the highest value for DC-DC₂, despite its lower overall η_{SW} .

It is clear that the comparison of ΔP_{in} can only be made for equal P_{out} , which is the case in this example. In order to be able to perform this comparison independently of P_{out} , ΔP_{in} is normalized over P_{in_lin} , yielding the *EEF* for switched-mode DC-DC step-down converters. This figure of merit allows for comparing different DC-DC step-down converters in terms of their η_{SW} , independent of P_{out} and k_{SW} . A more convenient form of the *EEF*, which is equivalent to the one of Table 2.1, is given by (2.81).

$$\begin{aligned}
 EEF &= \frac{\Delta P_{in}}{P_{in_lin}} \Big|_{k_{lin}=k_{SW}} = 1 - \frac{P_{in_lin} - P_{in_SW}}{P_{in_lin}} \Big|_{k_{lin}=k_{SW}} = 1 - \frac{\frac{P_{out_SW}}{\eta_{SW}}}{\frac{P_{out_lin}}{\eta_{lin}}} \Big|_{k_{lin}=k_{SW}} \\
 \Rightarrow EEF &= 1 - \frac{\eta_{lin}}{\eta_{SW}} \Big|_{k_{lin}=k_{SW}} \blacksquare
 \end{aligned} \tag{2.81}$$

Fig. 2.24 The upper graph shows the power conversion efficiencies η_{SW} and η_{lin} of a switched-mode DC-DC converter and a linear series voltage converter having the same voltage conversion ratio $k_{lin} = k_{SW}$, as a function of the output power P_{out} . The lower graph shows the corresponding EEF and \overline{EEF} , as a function of P_{out}



In the last step of for obtaining (2.81) it is assumed that $P_{out_lin} = P_{out_SW}$. The premise for this assumption is the fact that η_{lin} is not dependent on P_{out_lin} .

2.4.2 Interpretations

From the definition of the EEF , given by (2.81), it follows that the EEF will have a positive value for $\eta_{SW} > \eta_{lin}$ (wanted) and vice versa (unwanted). This is graphically illustrated in Fig. 2.24. The upper graph shows η_{SW} and η_{lin} for both a switched and a linear series DC-DC converter, for $k_{lin} = k_{SW}$, as a function of P_{out} . The lower graph shows both the EEF and its mean value \overline{EEF} as a function of P_{out} .

Calculating the EEF can essentially be performed in two alternative ways, leading to different interpretations. The first method is to calculate the EEF for a single value of η_{SW} , usually the highest/lowest one. This yields either the best or worst case scenario.⁵

The second way to perform the calculation of the EEF is by calculating it for multiple values η_{SW} , each at different values of P_{out} , and applying a power activity probability distribution $\alpha(P_{out})$. This $\alpha(P_{out})$ may follow from the targeted load application or it can also be a user-defined function. An example of such a function is (linear) ramp, indicating the weight of the EEF , and thus η_{SW} , becomes more

⁵Not to be confused with the album of dEUS.

important at higher values of P_{out} . Eventually this yields the weighted Efficiency Enhancement Factor \widetilde{EEF} , which is given by (2.82).

$$\widetilde{EEF} = \sum_{i=1}^n \frac{EEF(P_{out_i})\alpha(P_{out_i})}{i} \quad (2.82)$$

The \widetilde{EEF} gives a more realistic view on the performance of a switched-mode DC-DC step-down converter, with regard to η_{SW} , as it provides information on the overall performance over a certain load region. Obviously, when $\alpha(P_{out}) = 1$ (2.82) yields the mean Efficiency Enhancement Factor \overline{EEF} , as shown in the lower graph of Fig. 2.24.

Note that the main purpose of switched-mode DC-DC step-down converters is to provide a higher value for η_{SW} than achievable with a linear series DC-DC converter, which in essence is a resistive divider. If this constraint is not fulfilled, the additional complexity and cost of a switched-mode DC-DC converter, whether it is off- or on-chip, converter cannot be justified.

2.5 Conclusions

This chapter discusses the three DC-DC conversion methods and the associated principles of energy storage in capacitors, inductors and their combination:

1. *Capacitors:* (Sect. 2.2.1) The charging of a capacitor by means of a voltage source or another capacitor is intrinsically prone to losses. The energy charging efficiency η_{C_charge} is higher when the steady-state region is more closely approximated and if the initial voltage over the capacitor being charged is as close as possible to that of the voltage source or charging capacitor.
2. *Inductors:* (Sect. 2.3.1) The charging of an inductor by means of a voltage source is ideally lossless, unless when a finite, non-zero series resistance is assumed. In the latter case η_{L_charge} is higher when the charge time of the inductor is shorter and/or if the initial current through the inductor is lower.
3. *Capacitors and inductors:* (Sect. 2.3.2) The charging of a capacitor in series with an inductor by means of a voltage source is ideally lossless, unless when a finite, non-zero series resistance is assumed. In either case the energy stored in the capacitor will be maximal after the first half period, for a periodically damped system. At this point η_{RLC_charge} is also maximal and it will be higher when the initial voltage over the capacitor is closer to that of the voltage source, or when the initial current through the inductor is lower.

By using this knowledge the two methods for switched-mode DC-DC conversion are explained, together with the linear conversion method:

1. *Linear voltage converters:* (Sect. 2.1) This converter can only decrease the output voltage and is based on dissipating the excess energy. The power conversion efficiency is proportional to the voltage conversion ratio, for a series converter, and in addition proportional to the output power, for a shunt converter.

2. *Charge-pump DC-DC converters*: (Sect. 2.2) This converter can both decrease or increase the output voltage. The energy conversion efficiency will ideally only reach 100% at the optimal voltage conversion ratio, which depends on the used topology, and is independent of the output power.
3. *Inductive type DC-DC converters*: (Sect. 2.3) This converter can also both decrease or increase the output voltage. The energy conversion efficiency will ideally always reach 100%, regardless of the voltage conversion ratio and output power. The mathematical methods for calculating the voltage conversion ratio and output ripple, both for CCM and DCM, for an ideal boost converter example are explained in Sect. 2.3.3.

Finally a figure of merit for comparing DC-DC step-down converters, called the Efficiency Enhancement Factor (*EEF*), is introduced in Sect. 2.4. The EEF allows comparison in terms of power conversion efficiency that is independent of the voltage conversion ratio.

Design and Implementation of Fully-Integrated Inductive
DC-DC Converters in Standard CMOS

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