

Preface

Networks-on-Chip (NoC) is an emerging on-chip interconnection centric platform that leverages modern high speed communication infrastructure to mitigate the ever increasing on-chip communication challenges of modern many-core System-on-Chip (SoC) designs. Continuing shrinkage of feature dimensions of nano-scale semiconductor devices has raised grave concerns of the reliability, signal integrity, and quality of services (QoS) of traditional bus-based on-chip interconnect infrastructure. NoC represents a major paradigm shift to address these concerns by incorporating state-of-the-art high-speed data network components (such as routers and switches) and packet-based routing protocols into a novel on-chip network infrastructure. The aims of NoC developments are to provide a reliable on-chip communication platform to facilitate scalable giga-scale SoC design.

Over the past decades, numerous ground-breaking NoC-related platform development, component innovation, algorithm and protocol refinement have been reported in the form of journal and conference publications, as well as a couple of edited monographs. This book represents a succinct summary of NoC research outcome of an international collaboration team over the past few years. The emphasis of this book is on the QoS aspects of NoC development. Specifically, a case study of a bidirectional NoC architecture is discussed and several QoS issues, including performance, fault tolerance, and energy-aware computing, are carefully elaborated. The authors feel that this book would be a good complement of existing NoC literatures and should provide a practical implementation perspective of NoC which has not been fully explored in present NoC publications.

This book is organized into three integral parts. In Part I, a brief introduction of the key notions of NoC is provided. In addition to motivations and rationales, a comprehensive of preliminary background materials are provided to give a quick overview of relevant subject materials. In Part II, performance enhancing NoC network design methodologies, including routing, fault tolerance, energy awareness, and task scheduling are discussed. In Part III, a case study of a bidirectional link based NoC platform architecture is described. Its design rationale, performance enhancement characteristics, fault tolerance, and energy awareness features are also carefully analyzed.

This monograph is the outcome of a collaborative work written for researchers who are interested in learning the fundamental theories, architectures, and algorithms of NoC, as well as those who want to acquire the state-of-the-art NoC development. The authors would like to sincerely thank the foreword writer, Professor and Director Giovanni De Micheli at the Institute of Electrical Engineering and the Integrated Systems Center at the École Polytechnique Fédérale de Lausanne, Switzerland.

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