

Chapter 2

General Considerations of High-/Mixed- V_{DD} Analog and RF Circuits and Systems

2.1 Introduction

Instead of just following the rapid downsizing of V_{DD} in technology scaling, high-/mixed-voltage RF and analog CMOS circuits and systems have emerged as a prospective alternative [1], to deal with the wireless technology trends such as software-defined radio and cognitive radio; both are hungry for bandwidth and dynamic range. An elevated V_{DD} , or a hybrid use of I/O and core V_{DD} 's, in conjunction with optimum selection of thin- and thick-oxide MOSFETS open up much new design possibilities in re-defining circuit topologies, while maintaining most speed and area benefits of advanced fine linewidth processes [2]. Voltage-conscious bias techniques and overdrive protection circuits are simple and low overhead techniques to ensure the reliability of all devices. This chapter studies the basic design concept, system design considerations and some state-of-the-art circuit examples. A wide variety of analog and RF CMOS circuits featuring high-/mixed- V_{DD} is discussed. Those circuits comprise power amplifier, low-noise amplifier, mixer, operational-amplifier-based analog circuits, sample-and-hold amplifier and line driver. Reliability metrics such as oxide breakdown voltage, hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and bias temperature instability (BTI) will be briefly addressed. The involved concepts and techniques are generally extendable to different wireless and non-wireless applications.

2.2 System Considerations

A general system architecture of mixed-voltage wireless system-on-chip (SoC) for portable applications is depicted in Fig. 2.1. Thin-oxide transistors powered by $V_{DD,c}$ (core V_{DD}) exhibit the simplest structure to maximize the speed-to-power efficiency

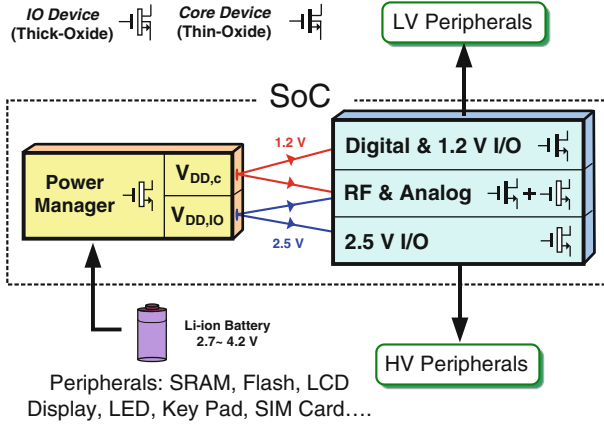


Fig. 2.1 Increase the design flexibility of analog and RF circuits with more options on voltage supplies and devices

of digital functions such as the digital signal processor. However, RF and analog circuits such as the RF power amplifier and the baseband operational amplifier are not that efficient to work under the same $V_{DD,c}$, which in the latest technologies, such as the 65 and 40-nm CMOS, has values in the order of 1 to 0.9 V [3], respectively. Such a reduced $V_{DD,c}$ limits: (1) the overdrive voltages on transistors, and (2) the linear output swing. Both of them can directly burden the performance optimization, especially in multistandard wireless systems that demand high-linearity low-noise wideband RF circuits [4]. Consequently, the exploration of a *voltage islanding concept* in a power management unit would become essential for distribution of the supply voltages to different RF and analog functions appropriately.

On the other hand, since many peripherals do not scale synchronously with the silicon technologies, thick-oxide transistors are still kept available in advanced processes to facilitate I/O communications. Thus, bringing thick-oxide transistors, and their associated $V_{DD,IO}$, into the RF and analog circuit design portfolio appears to be a handy option to increase the design flexibility. Thick-oxide transistors can be considered as devices from previous technology nodes: 0.25 and 0.18 μm . Their reliable operating voltages are 2.5 and 1.8 V, respectively. Both are much more comfortable values for RF and analog circuit design and can be easily generated by a 3.6/3.7-V Li-ion battery. Obviously, circuits built with purely thick-oxide transistors are not preferred as they cannot profit the speed and area benefits of advanced processes. A hybrid use of thin- and thick-oxide transistors, $V_{DD,c}$ and $V_{DD,IO}$, emerges then as a new art in electronics that should be adopted with a sensible balance. In the next sections, before the high-/mixed-voltage-enabled circuits for wide types of RF and analog functions are described, we will discuss the key device reliability concerns.

2.3 Device Reliability in Ultra-scaled Processes

The technology Design Rule Manual provides the key device reliability concerns including the absolute maximum rating (AMR), hot carrier injection (HCI), electrostatic discharge (ESD), time dependent dielectric breakdown (TDDB), bias temperature instability (BTI) and punchthrough effect. Complying with them in the design indeed translates the term “design for reliability” into “voltage-conscious design”, highly simplifying the design and verification methodologies [5]. Furthermore, in the topology formation phase, their implications to the circuits can be easily identified. Other reliability issues related to interconnects and materials like electromigration, stress-induced voiding and mechanical weakness are beyond the scope of this work.

2.3.1 AMR

The AMR corresponds to the maximum voltage applied to a minimum-gate-length device with no unrecoverable hard failure. AMR is concerned mainly with the gate-oxide breakdown voltage as it is 3–4 times smaller than the junction breakdown voltage [5]. A device biased close to the AMR limit may also lead to a deviation in device parameters, degrading the long-term reliability. The tolerable AMR is continuously reducing with the technologies (e.g., 1.6 V in 90-nm CMOS), complicating the design of ESD protection in high-frequency pins.

2.3.2 HCI Lifetime

Degradation of MOS device characteristics occurs as a result of exposure to a high V_{DS} with a large drain current. Examples of degradation are a shift of V_T and a shorter gate-oxide breakdown lifetime. HCI normally happens in high-power circuits such as the power amplifier, where the worst HCI bias conditions: $V_{DS} \geq V_{GS} \geq V_T$ and $V_{DS} \geq V_{DD}/2$ are concurrently satisfied. HCI degradation can be reduced by lowering the drain current or increasing the device channel length (L).

2.3.3 TDDB

TDDB is the wear-out of insulating properties of silicon dioxide in the CMOS gate, leading to the formation of a conducting path through the oxide to the substrate. In order to protect the circuit against TDDB the catastrophic destruction of gate oxides induced by the maximum DC gate oxide voltage at different temperatures

Table 2.1 Maximum DC gate oxide voltage to prevent TDDB

90 nm CMOS			65 nm CMOS		
	45°C	150°C		45°C	150°C
GP NMOS	1.43 V	1.28 V	GP NMOS	1.35 V	1.23 V
GP PMOS	1.29 V	1.17 V	GP PMOS	1.23 V	1.11 V

must be considered. According to the maximum DC gate oxide voltages of 90 and 65-nm CMOS given in Table 2.1, NMOS has a higher voltage standing capability than PMOS for all cases to prevent TDDB. Thus, NMOS is preferable when considering TDDB in circuit design.

2.3.4 NBTI

BTI degradation happens under steady-state conditions. It is design dependent in analog and RF circuits and primarily only PMOS devices are subjected to BTI stress, namely negative BTI (NBTI). In a V_{DD} -upscaled design, analyzing NBTI involves detecting, in all modes of operation (DC and small signal), which PMOS device is exposed to a peak or rms voltage value exceeding the standard V_{DD} , which is around 1 V in 90 and 65-nm CMOS. Thus, NMOS is also preferred when implementing analog switches.

2.3.5 Punchthrough

Transistor gate length should be increased wherever possible to prevent the drain-source depletion regions from punchthrough. In 90-nm CMOS, for a transistor having an aspect ratio (W/L) of 10/0.1, a strong increment of drain current due to punchthrough effect starts at a value of $|V_{DS}|$ around 2.3 V. Although the punchthrough effect is not intrinsically destructive it can accelerate, in the long term, the gate oxide breakdown because of the induction of hot carriers. Punchthrough is a critical concern in high-power circuits such as the power amplifier (PA), but it can be avoided for low-power RF circuits such as the low-noise amplifier (LNA).

2.4 Extend the Voltage Capability of Thin- and Thick-Oxide Transistors

With respect to the above-mentioned reliability concerns, individual thin (thick)-oxide transistors can withstand maximally just one $V_{DD,c}$ ($V_{DD,IO}$) voltage difference for any of the two terminals. In order to extend their voltage capability,

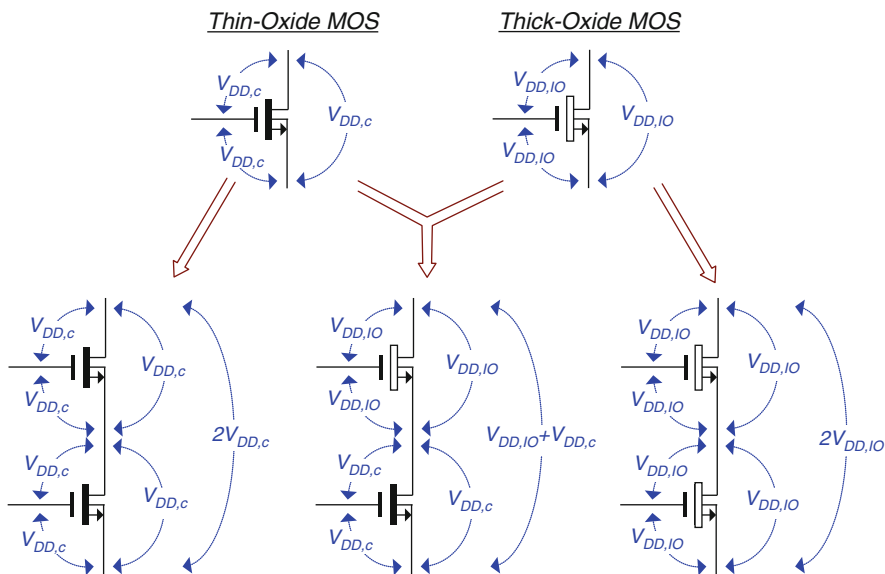


Fig. 2.2 Extending the voltage capability of thin- and thick-oxide transistors through stacking

stacking of devices can be applied. The concept is illustrated in Fig. 2.2. In steady state, the possible structures can be a stack of two (or more) thin-oxide transistors, thick-oxide transistors, or a hybrid use of both. Generally, the voltage capability across the drain and source terminals can be multiplied by the number of stacked transistors. One basic request of this technique is that the bulk should be tied to the source terminal to avoid overstress between them, implying the need of a triple-well process for NMOS to have an isolated bulk.

Among the three structures shown in Fig. 2.2 only pure stack of thin-oxide transistors and a hybrid stack of thin- and thick-oxide transistors are relevant to balance the speed and voltage capability. A pure stack of thick-oxide transistors cannot take advantage of the area and speed features of advanced technologies. In the hybrid case the thin-oxide transistor can serve as the amplification device for minimization of the loading effect to the previous stage. The thick-oxide transistor serves as the cascode device thus increasing the voltage capability. High-/mixed-voltage RF and analog circuits are generally based on these two stacking structures.

In addition to steady-state overstress, transient-state overstress should not be allowed too. Depending on the nature of the signal processing, large-signal circuits (e.g., line driver) requires checking the trajectory of all nodes. Alternative solutions are to employ voltage-biased and self-biased circuit topologies; both of them have the benefit that the internal node voltages can be easily controlled during power up/-down transients. Examples of the techniques will be discussed in the next section.

2.5 High-/Mixed-Voltage Building Blocks

2.5.1 Power Amplifier and Wideband Balun-LNA (High- V_{DD} + Mixed-Transistor)

V_{DD} -upscaling circuits have appeared in the literature for many years. The most common application is on the PA. As shown in Fig. 2.3a a hybrid use of thin- (M_1) and thick-oxide device (M_2) in cascode permits using of a higher V_{DD} beyond the standard value to maximize the possible output power in 0.13- μm CMOS [6]. The reliability test should be under the maximum output power level with the entailed modulation (e.g., 64QAM OFDM), to ensure the steady-state overstress conditions are met (i.e., $|V_{GD,rms}|$, $|V_{GS,rms}|$ and $|V_{DS,rms}|$ have to be less than V_{DD} of each device type). M_2 entails a triple well for independent bulk-source connection.

On the other hand, in order to protect M_1 from overstressing automatically during the power-up/down transients, we propose to add a thick-oxide device M_{pt1} can be added to the V_x node. Its size is not critical as its aim is to ensure $V_x < V_{DD,c}$ when $V_{DD,elevated}$ is activated first and can be turned off when $V_{DD,c}$ has caught up automatically.

Mixed-transistor circuit topologies also find applications in recent small-signal linearity-demanding wireless circuits and systems [7–9]. A 90-nm CMOS ultra-wideband balun low-noise amplifier (LNA) [7] based on an elevated V_{DD} (2.5 V)

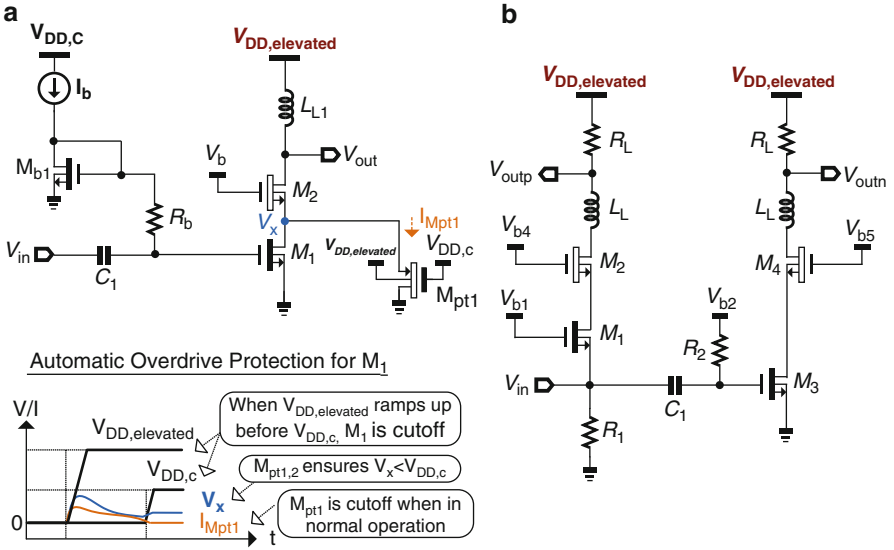


Fig. 2.3 RF circuits using an elevated V_{DD} . (a) Power amplifier with automatic protection of M_1 from being overstressed. (b) Wideband balun LNA

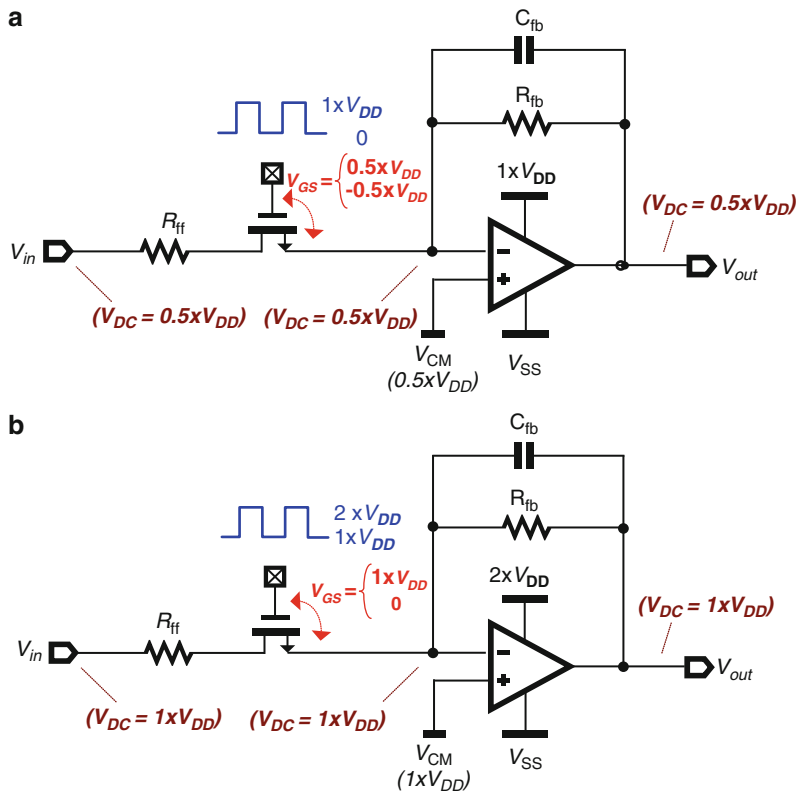


Fig. 2.4 Downconversion passive mixers: (a) $1 \times V_{DD}$ design. (b) $2 \times V_{DD}$ design

increases the output dynamic range while allowing more voltage drop at the resistive load R_L (Fig. 2.3b), achieving both high gain and high linearity but a smaller output bandwidth due to an increased R_L . A gain-peaking inductor L_L can be exploited to extend the output bandwidth. M_{pt1} in Fig. 2.3a can also be applied to this topology to protect M_1 and M_3 .

2.5.2 Passive Mixers (High- V_{DD} + Thin-Oxide Transistor)

A passive current-mode downconversion mixer can be implemented with a resistor R_{ff} in-series with a MOS switch, and terminated with a virtual ground through the use of an operational amplifier (OpAmp). The OpAmp provides linear I-V conversion and first-order lowpass filtering at the output. In order to achieve a rail-to-rail output swing the output dc-level should be at half of the supply. For a generic $1 \times V_{DD}$ design as shown in Fig. 2.4a, the clocked MOS switch can only have

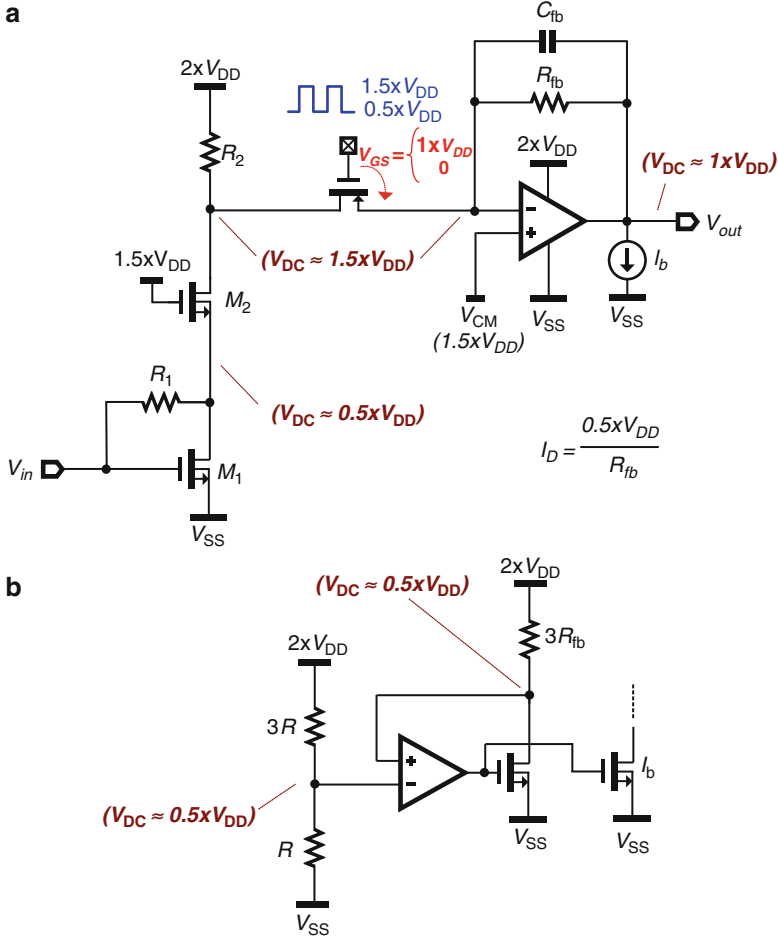


Fig. 2.5 (a) $2 \times V_{DD}$ passive mixer with mixer driver and its (b) I_b generation circuit

a maximum overdrive voltage of $0.5 V_{DD}$. However, by doubling the supply to $2 \times V_{DD}$ as shown in Fig. 2.4b, the overdrive voltage of the MOS switches is maximized to the technology allowable limit, i.e., $1 \times V_{DD}$. This act significantly reduces the size of the MOS switch and its induced nonlinearity. The design of $2 \times V_{DD}$ OpAmp will be presented later in this chapter.

Another type of $2 \times V_{DD}$ passive mixer with a mixer driver is shown in Fig. 2.5a. A $2 \times V_{DD}$ 90-nm CMOS cascode amplifier serves as the mixer driver improving the linearity and reverse isolation but the output dc-level is up-shifted to $1.5 \times V_{DD}$. Under a $1.5 \times V_{DD}$ dc-level PMOS is preferred as the mixing MOS to maximize the overdrive voltage. The unmatched input and output dc-levels of the OpAmp require an extra bias current I_b to sink out the excess dc-current in the feedback loop. Since I_b depends on the absolutely value of R_{fb} , a resistance-tracking

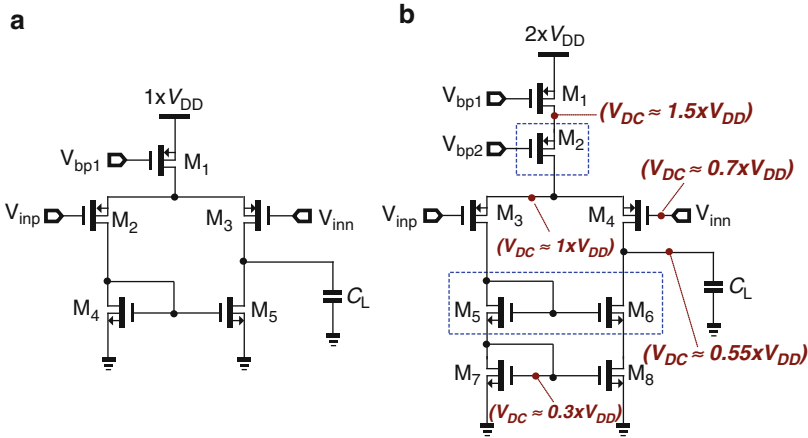


Fig. 2.6 Typical OpAmp's input stage: (a) 1 V (typical) (b) 2 V-enabled

Table 2.2 Comparison between 65-nm 1-V and 2-V OpAmp's input stage with a current-mirror load

Parameters	1 V OpAmp's input stage	2 V OpAmp's input stage
Technology	65 nm CMOS	
Transistor type	1 V GP NMOS and PMOS	
Power consumption	0.4 mW	
Load C_L	1 pF	
DC gain	10 dB	18.4 dB
Unity-gain frequency	318.5 MHz	191 MHz
Phase margin	107°	95°
HD3 (@ 1 MHz input)	45.6 dB at 125 mV _{pp} Output	44.3 dB at 330 mV _{pp} Output
Output noise voltage (@ 100 MHz)	14.6 nV/sqrtHz	14.7 nV/sqrtHz

bias circuit can be utilized for this purpose. As shown in Fig. 2.5b, an error amplifier together with a $3R_{fb}$ and a current mirror generates the required value of $I_b = 0.5 \times V_{DD}/R_{fb}$. It should be noted that no device is under overstress.

2.5.3 Differential Pair (High- V_{DD} + Thin-Oxide Transistor)

A 3.3-V 0.18- μ m CMOS two-stage operational amplifier (OpAmp) was demonstrated in [10]. The concept of extending the voltage is related with the addition of extra cascode transistors, boosting the voltage-withstand capability from 1.8 to 3.3 V. The input stage is of particular interest as it is based on a high-voltage-enabled differential pair using a current mirror load. In order to understand the performance difference in an advanced process, we re-designed and compared only the input stage of the OpAmp (output stage is more customized) in 65-nm CMOS, as shown in Fig. 2.6a and b. Table 2.2 summarizes the simulation

Table 2.3 Design equations of $1 \times V_{DD}$ FC, RFC, RFC and $2 \times V_{DD}$ RFC OpAmps

	FC	1-V RFC	2-V RFC
Current	$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$		
Transconductance	$G_{m,FC} = g_{m1}$	$G_{m,1V-RFC} = g_{m1a}(1+K)$	$G_{m,2V-RFC} = g_{m1a}(1+K)$
Output impedance	$R_{O,FC} \approx \frac{(r_{o1} r_{o3}) [(g_{m5} + g_{mbs}) r_{o5}]}{(g_{m1} r_{o7})} \cdot R_{O,FC}$	$R_{O,1V-RFC} \approx \frac{[(g_{m5} + g_{mbs}) r_{o5} (r_{o1a} r_{o3a})]}{(g_{m1} r_{o7})} \cdot R_{O,1V-RFC}$	$R_{O,2V-RFC} \approx \frac{[(g_{m5} + g_{mbs}) r_{o5} (r_{o1a} r_{o3a})]}{(g_{m1} r_{o7})} \cdot R_{O,2V-RFC}$
Gain	$A_{v,FC} = G_{m,FC} \cdot R_{O,FC}$	$A_{v,1V-RFC} = G_{m,1V-RFC} \cdot R_{O,1V-RFC}$	$A_{v,2V-RFC} = G_{m,2V-RFC} \cdot R_{O,2V-RFC}$
GBW	$GBW_{FC} \approx \frac{G_{m,FC}}{C_L}$	$GBW_{1V-RFC} \approx \frac{G_{m,1V-RFC}}{C_L}$	$GBW_{2V-RFC} \approx \frac{G_{m,2V-RFC}}{C_L}$
Output swing	$V_{O,Swing,FC} = 2 \times [1 - (V_{ov3} + V_{ov5} + V_{ov7} + V_{ov9})]$	$V_{O,Swing,1V-RFC} = 2 \times [1 - (V_{ov3a} + V_{ov5} + V_{ov7} + V_{ov9})]$	$V_{O,Swing,2V-RFC} = 2 \times [2 - (V_{ov3a} + V_{ov5} + V_{ov7} + V_{ov9})]$
Slew rate	$SR_{FC} = \frac{I_b}{C_L}$	$SR_{1V-RFC} = \frac{K I_b}{C_L}$	$SR_{2V-RFC} = \frac{K I_b}{2 C_L}$
Thermal noise	$\frac{v_{f,FC}^2}{v_{f,FC}^2} = \frac{8k_B T \gamma}{g_{m1}} \cdot [1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}}] \cdot \Delta f$	$\frac{v_{f,1V-RFC}^2}{v_{f,1V-RFC}^2} = \frac{8k_B T \gamma}{g_{m1a}(1+K)} \cdot \left[\frac{(1+K^2)}{1+K} + \frac{g_{m3a}}{g_{m1a}} + \frac{g_{m9a}}{g_{m1a}} \right] \cdot \Delta f$	$\frac{v_{f,2V-RFC}^2}{v_{f,2V-RFC}^2} = \frac{8k_B T \gamma}{g_{m1a}(1+K)} \cdot \left[\frac{(1+K^2)}{1+K} + \frac{g_{m3a}}{g_{m1a}} + \frac{g_{m9a}}{g_{m1a}} \right] \cdot \Delta f$
Flicker noise	$\frac{v_{f,FC}^2}{v_{f,FC}^2} = \frac{K_{FP}}{\mu_p C_{ox} W L f} [1 + 2 \frac{K_{FV}}{K_{FP}} (\frac{L_1}{L_3})^2 + (\frac{L_1}{L_3})^2] \cdot \Delta f$	$\frac{v_{f,1V-RFC}^2}{v_{f,1V-RFC}^2} = \frac{K_{FP}}{\mu_p C_{ox} W L f} \frac{K_{FP}}{(K-1) (\frac{L_1}{L_3})^2 + (\frac{L_1}{L_3})^2} \frac{[(1+K^2)]}{(1+K)} + K \frac{K_{FV}}{K_{FP}} (\frac{L_1}{L_3})^2 \cdot \Delta f$	$\frac{v_{f,2V-RFC}^2}{v_{f,2V-RFC}^2} = \frac{K_{FP}}{\mu_p C_{ox} W L f} \frac{K_{FP}}{(K-1) (\frac{L_1}{L_3})^2 + (\frac{L_1}{L_3})^2} \frac{[(1+K^2)]}{(1+K)} + K \frac{K_{FV}}{K_{FP}} (\frac{L_1}{L_3})^2 \cdot \Delta f$
Power	$P = I_{Total,FC} \times 1$	$P = I_{Total,1V-RFC} \times 1$	$P = I_{Total,2V-RFC} \times 2$

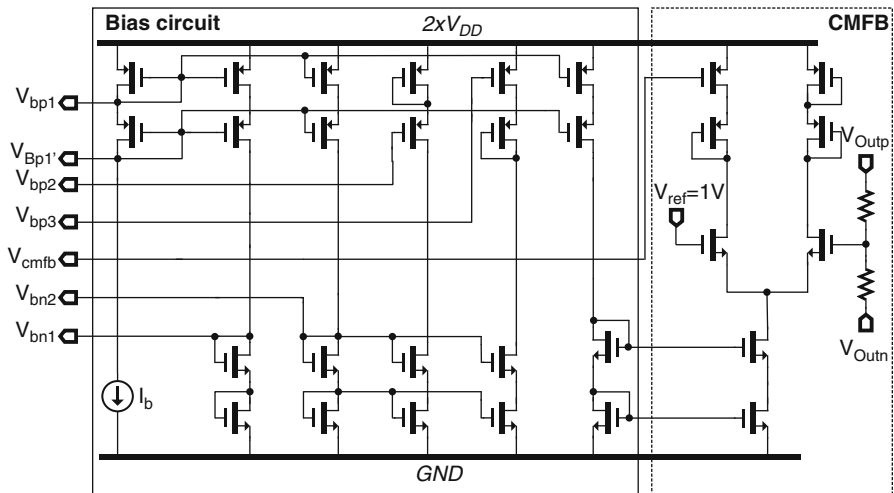


Fig. 2.10 Bias and CMFB circuits for the $2 \times V_{DD}$ -enabled RFC OpAmp

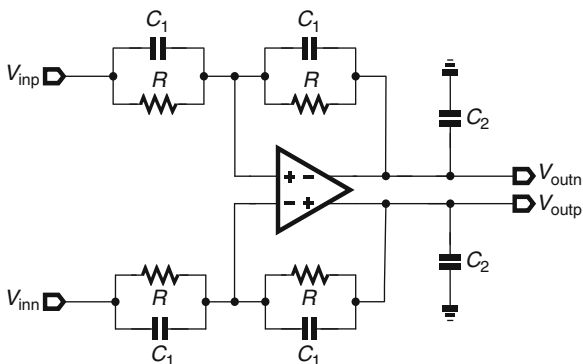


Fig. 2.11 A unity-gain amplifier is used to assess the performance and reliability of a $2 \times V_{DD}$ -enabled RFC OpAmp. $R = 600 \text{ k}\Omega$, $C_1 = 2 \text{ pF}$ and $C_2 = 4 \text{ pF}$. The input and output dc-levels are $1 \times V_{DD}$ to maximize the signal swing and allow ease of cascading

As for the GBW, the FC, 1-V RFC and 2-V RFC is 68.2 MHz, 157.8 MHz and 97.5 MHz, The GBW of the $2 \times V_{DD}$ design, as expected, is less than to that in the $1 \times V_{DD}$ design under the same power budget, but is fairly adequate for most analog functions with signal bandwidth of less than 10 MHz. The phase margin simulated for FC, 1-V RFC and 2-V RFC is 86.6° , 60.9° and 70.7° at their respective GBWs. The phase margin of 1-V RFC is smallest since it has the largest GBW, and has more poles compared to FC. The 2-V RFC shows less phase margin compared to FC, since the larger GBW and the multiple poles added by

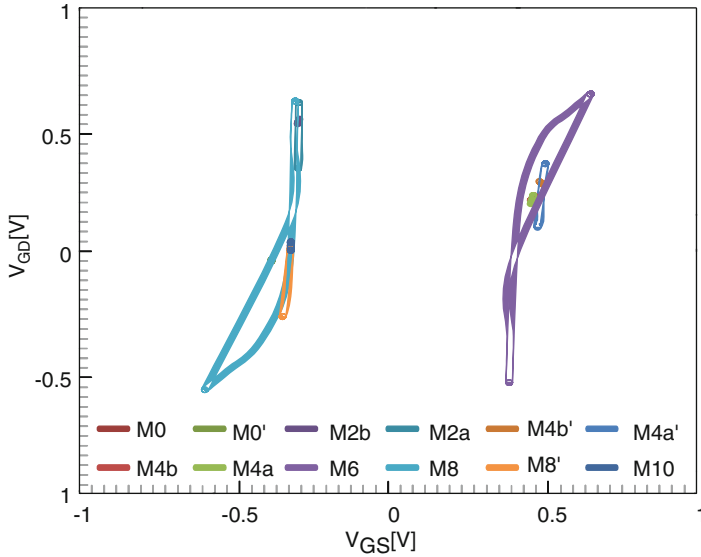


Fig. 2.12 $2 \times V_{DD}$ -enabled RFC OpAmp's V_{GS} - V_{GD} trajectories when a square-wave input is applied with a signal swing of $1.2 V_{pp}$

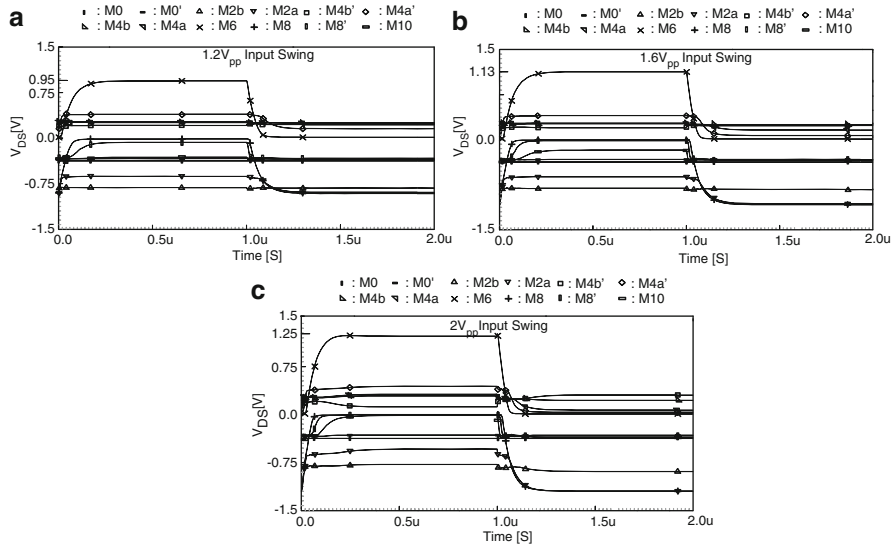


Fig. 2.13 V_{DS} variation versus time at an input swing of (a) 1.2 V, (b) 1.6 V and (c) 2 V. The notations correspond to Fig. 2.9. The maximum V_{ds} is within 0.95/1.13/1.25 V, respectively

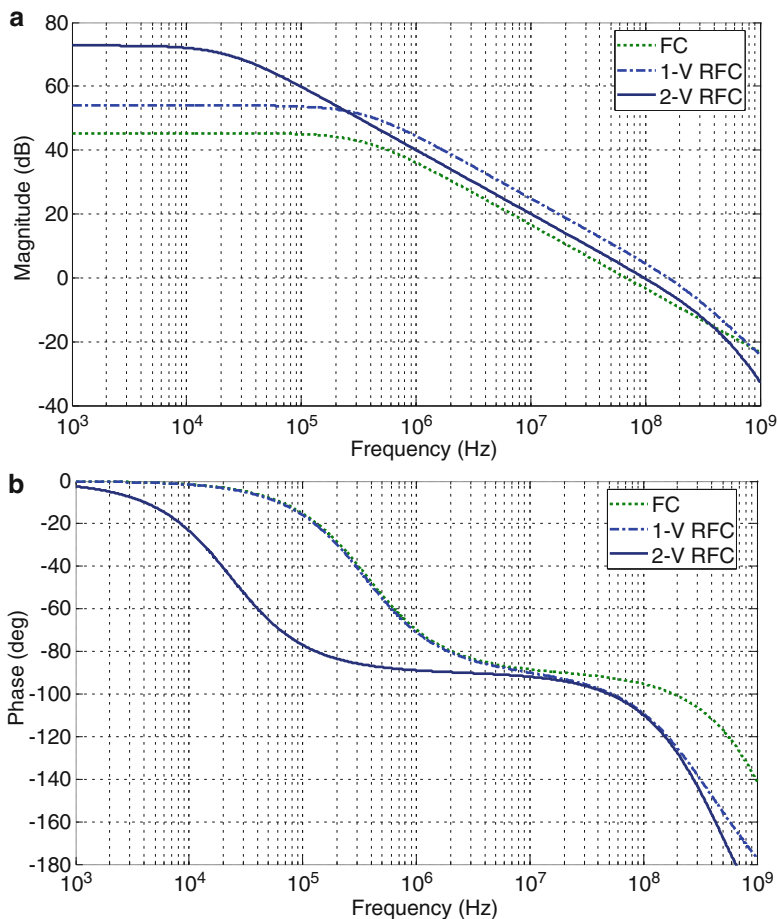


Fig. 2.14 (a) Gain and (b) phase responses of 1-V and 2-V RFC OpAmps

cascode and current mirror. Nevertheless, neither amplifier shows any ringing in the transient performance.

The linearity of the OpAmps is assessed as follows: a two-tone test centered around 500 kHz (250 mV_{pp} at 450 kHz and 250 mV_{pp} at 550 kHz) was applied to the three OpAmps, and their results are shown in Fig. 2.15a–c. The third intermodulation distortion, $IM3$, is -49.7 dB (1-V FC), -57.2 dB (1-V RFC) and -76.5 dB (2-V RFC), as shown in Fig. 2.16. For an analog-to-digital converter, the achieved gain of the 2-V RFC OpAmp corresponds to >11 -bit resolution for an output swing as large as $0.8 V_{pp}$. When they are in a unity-gain configuration, Fig. 2.17 confirms the high gain accuracy of the 2-V RFC OpAmp over such a wide output swing.

The input-referred noises of the three OpAmps are shown in Fig. 2.18. When integrated over a bandwidth of 1 Hz to 100 MHz, the noises are $74.4 \mu V_{rms}$ (FC), $64.3 \mu V_{rms}$ (1-V RFC) and $83.2 \mu V_{rms}$ (2-V RFC). The latter is actually inferior

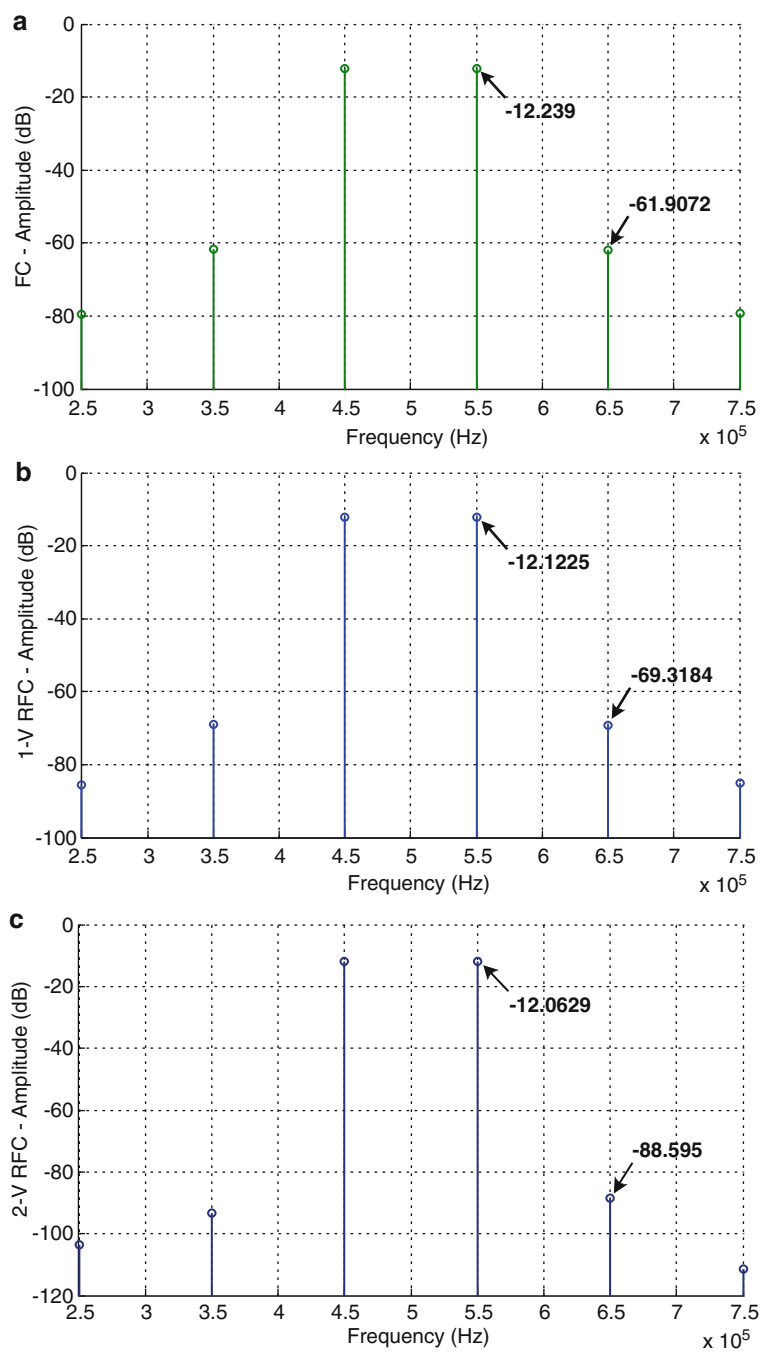


Fig. 2.15 Two tone FFT spectrums of (a) the FC, (b) the 1-V RFC and (c) the 2-V RFC for a 0.5 Vpp signal centered at 500 kHz and separated by 100 kHz

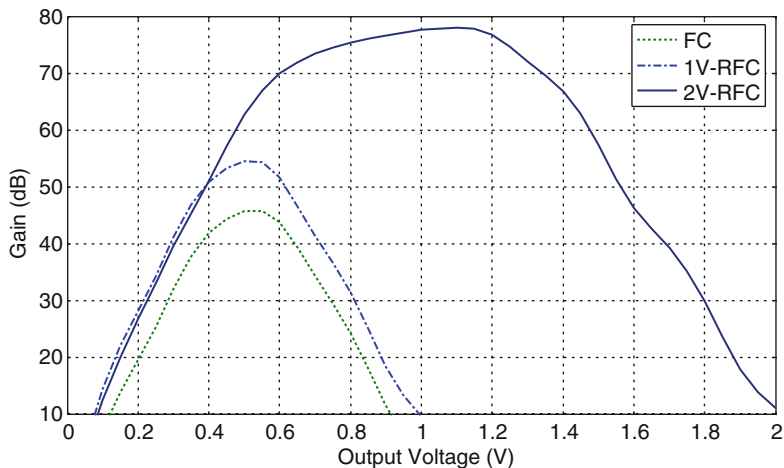


Fig. 2.16 Open-loop gain versus output voltage. The common-voltage voltages are $V_{cm, FC} = 0.5$ V, $V_{cm, 1-V\ RFC} = 0.5$ V and $V_{cm, 2-V\ RFC} = 1$ V

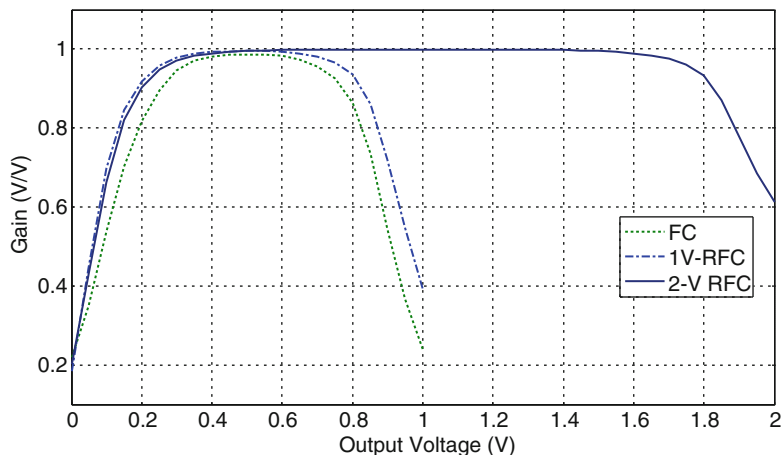


Fig. 2.17 OpAmps in a unity gain configuration. The common-voltage voltages are $V_{cm, 1-V\ FC} = 0.5$ V, $V_{cm, 1-V\ RFC} = 0.5$ V and $V_{cm, 2-V\ RFC} = 1$ V

comparing with the 1-V ones. Table 2.4 summarizes their simulation results. It concludes that the $2 \times V_{DD}$ RFC OpAmp is more efficient in improving the gain precision and linearity of analog circuits. However, when GBW and noise are the priorities, the 1-V RFC OpAmp becomes more superior. Voltage-oriented OpAmp design, therefore, improves the performance metrics very different from the current-oriented ones in nm-length CMOS processes.

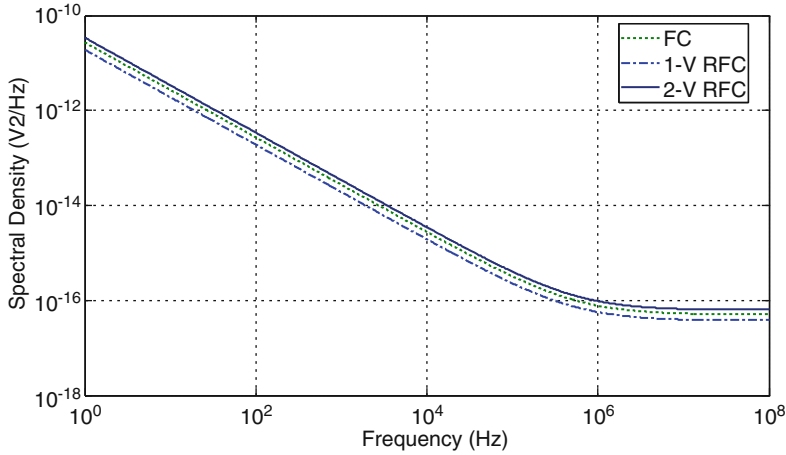


Fig. 2.18 Input referred noise spectral power density

Table 2.4 Performance summary for 1-V and 2-V RFC OpAmps

Parameter	FC	1-V RFC	2-V RFC
Power (bias current) [μ A]	600	600	300
DC gain [dB]	45.3	54.0	72.8
GBW [MHz]	68.2	157.8	97.5
Open loop PM [deg]	86.6	60.9	70.7
Capacitive load [pF]	5.0	5.0	5.0
Slew rate (average) [V/ μ s]	53.3	96.6	65.4
1% settling time [ns]	24.8	9.8	18.0
Gain precision (closed loop, ideal case is 1)	98.6%	99.4%	99.8%
IM3, 0.5 Vpp at 0.5 MHz [dB]	-49.7	-57.2	-76.5
Input referred noise (1 Hz–100 MHz) [μ Vrms]	74.4	64.3	83.2

2.5.5 OpAmp-Based Analog-Baseband Circuits (Mixed- V_{DD} + Mixed-Transistor)

As shown above, a $2 \times V_{DD}$ recycling folded-cascode (RFC) OpAmp can achieve better performances than its $1 \times V_{DD}$ counterpart such as DC gain and close-loop linearity under a similar power budget. The applications of such an OpAmp are extensive, as shown in Fig. 2.19. Depending on the selected impedances of Z_{fb} and Z_{ff} several types of continuous-time and discrete-time circuits can be synthesized. Of course, in some cases, it will need to interface between standard- V_{DD} and high- V_{DD} building blocks. As shown in Fig. 2.20a, in a transmitter the use of $1 \times V_{DD}$ and $2 \times V_{DD}$ OpAmp allows a progressively increase of linear output swing. The level shifter is a current source I_b . Another case is shown in Fig. 2.20b for receiver, a $2 \times V_{DD}$ OpAmp (at the front) offers wider linear output swing to handle the out-of-channel interferer $1 \times V_{DD}$ OpAmp (at the back) easily interfaces with $1 \times V_{DD}$ ADC. Again, I_b allows seamless cascade of blocks having different common-mode voltages.

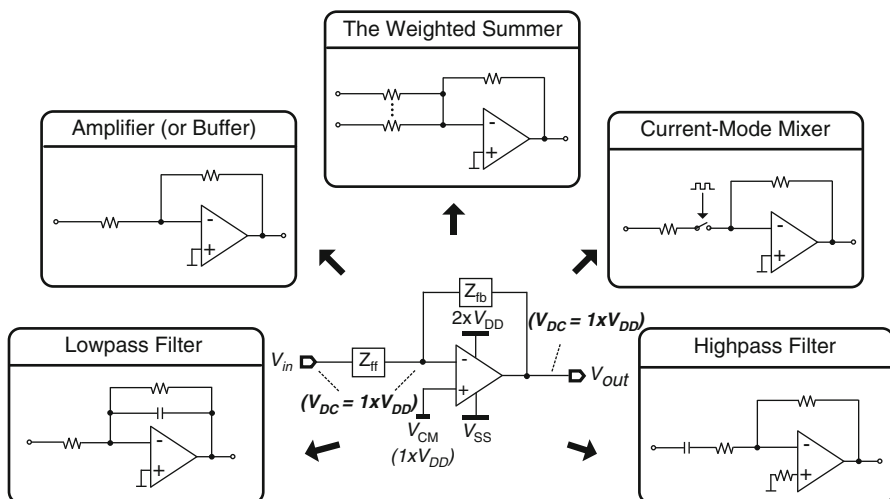


Fig. 2.19 Analog-baseband circuits based on a $2 \times V_{DD}$ OpAmp

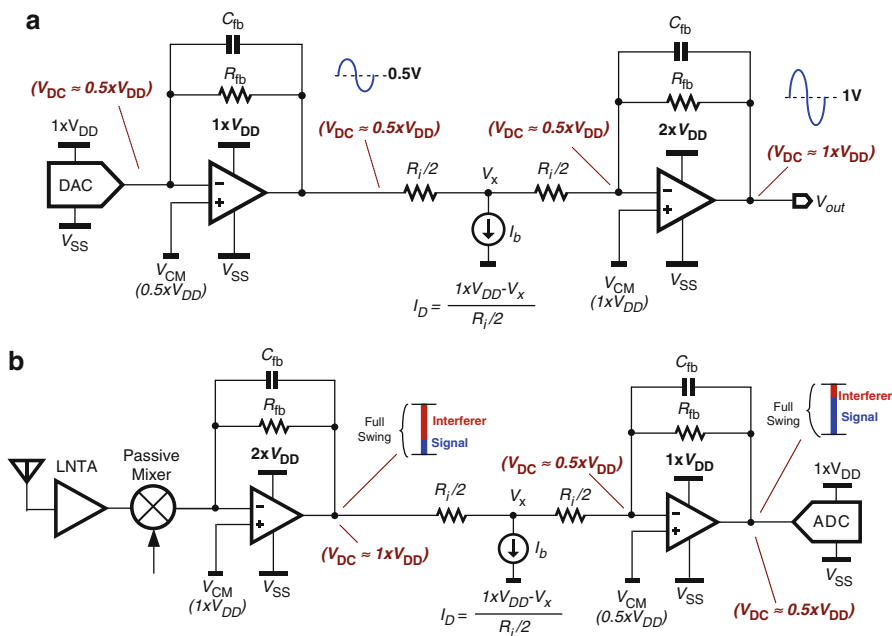


Fig. 2.20 Level shifting: (a) $1 \times V_{DD}$ to $2 \times V_{DD}$. (b) $2 \times V_{DD}$ to $1 \times V_{DD}$

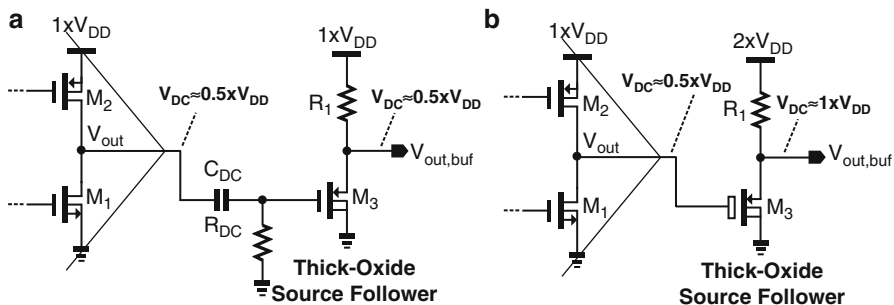


Fig. 2.21 (a) Standard- V_{DD} and (b) mixed- V_{DD} source follower serves as a buffer

After lowpass filtering, the baseband signal can be driven off-chip or to the analog-to-digital converter (ADC). In either case, a high- V_{DD} source follower with a thick-oxide MOS can be used as the buffer, as compared in Fig. 2.21a and b for mixed- V_{DD} and standard- V_{DD} design. The mixed- V_{DD} design inherently offers level-shifting, avoiding any AC-coupling circuit that is area hungry at baseband, i.e., the highpass cutoff frequency should be sufficiently low to prevent notching the signal spectrum.

2.5.6 Low-Dropout-Regulator (*Mixed- V_{DD} + Mixed-Transistor*)

Low-dropout regulators (LDOs) are widely employed in SoC for improving the power-supply rejection ratio (PSRR) of the internal circuit. PMOS-based LDO (Fig. 2.22a) is more popular than its NMOS counterpart (Fig. 2.22b) for its lower dropout voltage property. The main issue of PMOS-based LDO is the necessity of an external big capacitor to ensure the stability. Such a requirement significantly increases the manufacturing cost and pin counts because many LDOs are entailed for a SoC. The NMOS-based LDO, on the other hand, is free from such a request (i.e., cap-less) and features better stability and PSRR+. The key appeal is that V_G will need to be greater V_{DD12} , which is not normally possible in a single- V_{DD} design. In a mixed- V_{DD} design, $V_G > V_{DD12}$ can be solved as shown in Fig. 2.22c. The abovementioned benefits of NMOS-based LDO are retained, while an add-on benefit is that the maximum $V_{out,max}$ can now be V_{DD12} (i.e., no dropout voltage!). The drawback is that every 1-mA current to Z_L yields 1.3-mW power loss in the pass transistor. Thus, the technique befits better low-power high-sensitivity circuits.

In addition to V_{DD} -LDO, ground-LDO is becoming more crucial to desensitize low-noise high-DR circuits, e.g., voltage-controlled oscillator (VCO), from substrate noise coupling in a noisy SoC environment as shown in Fig. 2.23. Due to the

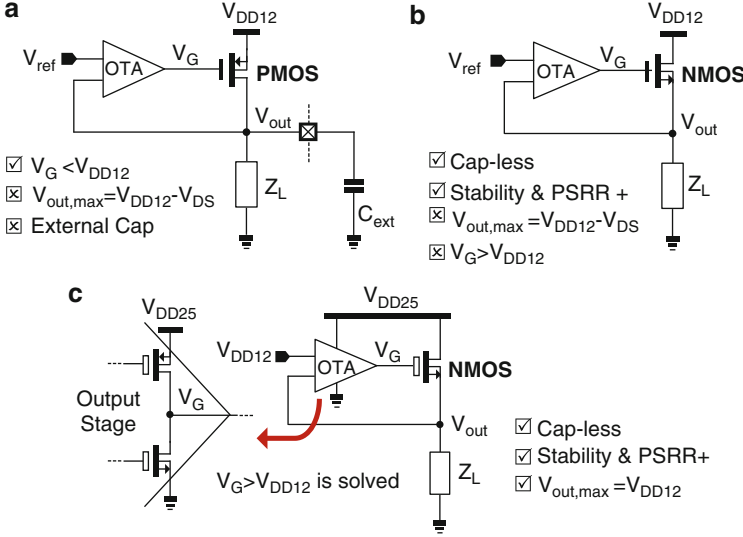


Fig. 2.22 LDO with (a) a PMOS pass transistor. (b) a NMOS pass transistor, and (c) mixed-voltage design on a NMOS pass transistor

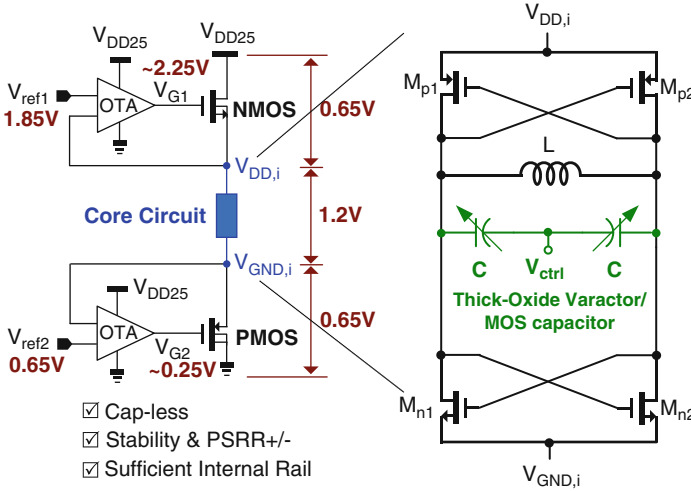


Fig. 2.23 Mixed-voltage mixed-transistor LDO for both positive and negative rails

presence of V_{DD25} , V_{DD} -LDO and ground-LDO can be jointly employed. The VCO may employ a thick-oxide varactor or MOSFET capacitor as the frequency tuning element, covering potentially a wider tuning range. Proper biases can ensure the internal rail sufficiently large for the core circuit, surpassing the voltage-headroom

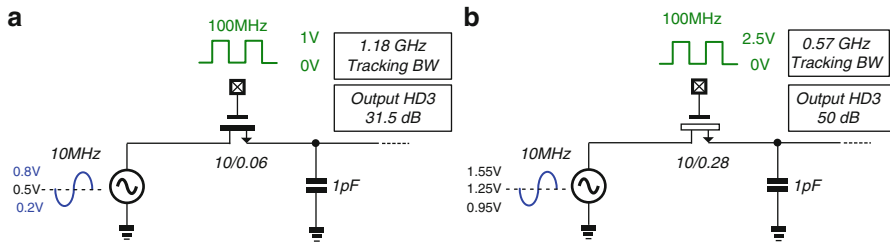


Fig. 2.24 Sample-and-hold circuits: (a) 1-V design. (b) 2.5-V design

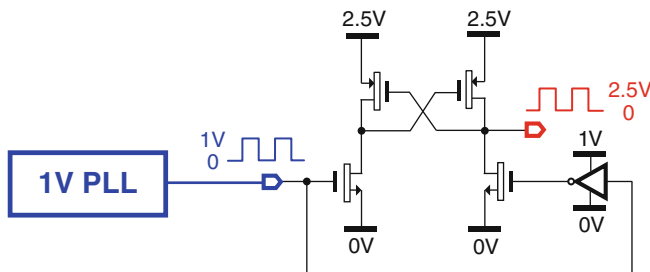


Fig. 2.25 Clock level shifter for 1–2.5 V

tradeoff when employing LDO for PSRR improvements. Again, the drawback is that every 1-mA current to Z_L yields 1.3-mW power loss in the two pass transistors.

2.5.7 Sample-and-Hold Amplifier ($\text{High-}V_{DD} + \text{Mixed-Transistor}$)

Discrete-time analog-baseband circuits not only can benefit from the area and power savings of a V_{DD} -elevated OpAmp, but also the extra voltage headroom to improve the linearity of sampling. Shown in Fig. 2.24a and b are two sample-and-hold circuits with 1-V and 2.5-V supplies, respectively. At a 100-MHz sampling rate, to sample-and-hold a 10-MHz 0.6-V_{pp} sinusoidal input at a dc level that is midway to $V_{DD}/2$, the former, based on thin-oxide MOS with a minimum channel length of 60 nm can achieve 1.18-GHz tracking bandwidth (BW) but the HD3 is limited to 31.5 dB. Alternatively, the latter based on thick-oxide MOS with a minimum channel length of 280 nm can achieve 50-dB HD3, but the tracking BW is almost halved. Then, this speed-linearity tradeoff is subject to applications and can be flexibly selected in advanced processes, as both thin- and thick-oxide devices are available. Since the clock is normally synthesized with the thin-oxide circuit for power and area reduction, a clock level shifter, as shown in Fig. 2.25, would be required for the 2.5-V design. Thus, power and speed overheads must be considered.

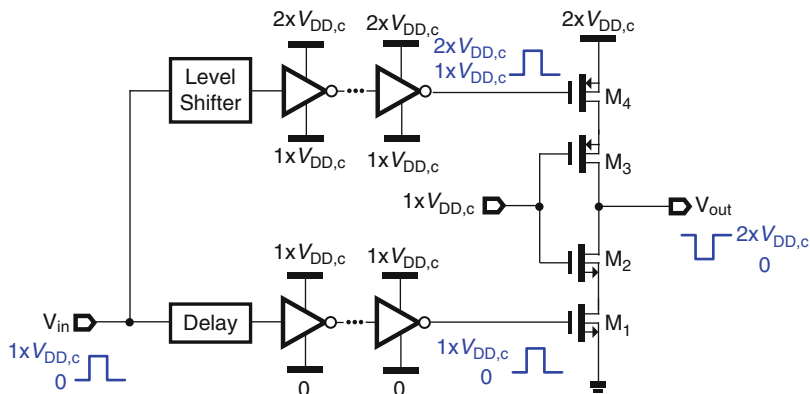


Fig. 2.26 CO line driver with a $2 \times V_{DD,c}$

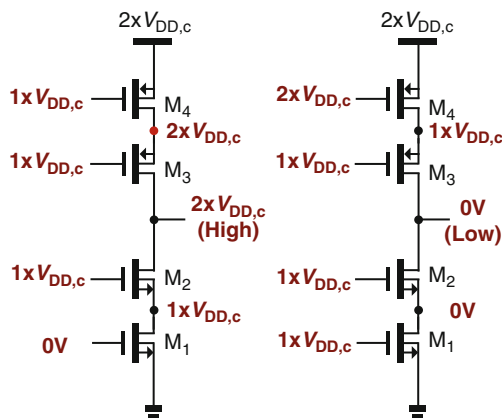


Fig. 2.27 The internal node voltages when the output stage is delivering high and low-state outputs showing all voltage differences are within $1 \times V_{DD,c}$

2.5.8 Line Driver ($High-V_{DD} + Thin-Oxide Transistor$)

Reference [13] has demonstrated that a 5.5-V line driver realized in a standard 1.2-V 0.13- μm process is capable of attaining state-of-the-art performances with no reliability degradation. Figure 2.26 depicts the block schematic of such a central office (CO) line driver topology (the output stage), where a $2 \times V_{DD,c}$ supply is adopted for simplicity. The input signal is delayed (to synchronize with the upper path) and buffered to drive the NMOS device M_1 , besides being also level-shifted up to drive the PMOS device M_4 . The cascode transistors M_2 and M_3 serve to increase the voltage-withstand capability. With a $2 \times V_{DD,c}$ supply, the gate-bias voltages of M_2 and M_3 are very simple, i.e., $1 \times V_{DD,c}$ to ensure no overstress in both high- and low-state outputs (Fig. 2.27). For a higher V_{DD} multiplying design (i.e., greater than 2),

a dedicated bias circuit for each cascode transistor is necessary to guarantee no device is under overstress in both steady-state and transient operations. The circuit needs two supplies $1 \times V_{DD,c}$ and $2 \times V_{DD,c}$. The application-related performance metrics are available elsewhere [13].

This $2 \times V_{DD}$ line driver has been recently modified to work on a 90-nm CMOS switched-capacitor power amplifier [14] and 32-nm CMOS class-D power amplifier [15]; both demonstrate state-of-the-art performances, further proving the importance of high-/mixed- V_{DD} designs in nanoscale CMOS.

2.6 Summary

High-/mixed-voltage techniques feature high potential to boost up the performances of RF and analog circuits without degrading the reliability. Bringing the $V_{DD,IO}$ and thick-oxide transistors into the RF and analog circuit design portfolio does not by itself require any add-on resource or technology option (at least up to now), but it effectively increases the design flexibility. Circuit techniques play a key role in this development, and are therefore long-term reusable when the technology continues to advance.

This chapter only serves as a glimpse of this research trend and guiding direction, while highlighting the necessary gate-drain-source engineering skills to take a broader advantage of available techniques. One of the critical points would be to guarantee the circuit reliability compliance with the foundry guidelines when considering device size and the potential adopted bias in transient and steady states. Advantages of high-/mixed-voltage analog and RF CMOS circuits have been demonstrated by several recent works, and are easily extendable to other applications.

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