

Chapter 2

Semiconductor LCI Methods

Sources of environmental impacts in IC production and use include emissions from electricity generation and fuel incineration as well as direct process emissions at manufacturing sites. Looking upstream, environmental impacts also occur due to process heating, electricity generation, and direct emissions in several additional life-cycle stages, including production and purification of silicon, infrastructure construction, equipment manufacturing and chemicals production. Transportation also contributes to impacts as a component of these upstream life-cycle stages, and as a stage of its own, when wafers are conveyed from the wafer fabrication facility to the assembly plant and chips are transported to the point of use. Figure 2.1 depicts the sequence of some of the key life-cycle stages for a semiconductor product, as well as some environmentally significant ancillary stages.

A variety of methods have been used to evaluate the energy use, global warming impact or other environmental effects resulting from the production and use of semiconductors. In this chapter, a summary of the techniques available for evaluation or estimation of semiconductor LCI data, including upstream processes (chemicals, facility and equipment production) will be presented. Particular attention will be paid to LCI of wafer fabrication, and the customization of existing integrated circuit LCI data for downstream use, in LCA of electronics.

2.1 LCI of Wafer Fabrication

In order to develop an LCI for the life-cycle stage of wafer fabrication, power, water and materials use, and facility emissions should be accounted for. An LCI may be developed by develop measuring or taking data on site, using established estimation methods such as those developed by governments, or by adapting existing LCI data for wafer production of an equivalent IC to the application. In this section, these three methods will be described in detail.

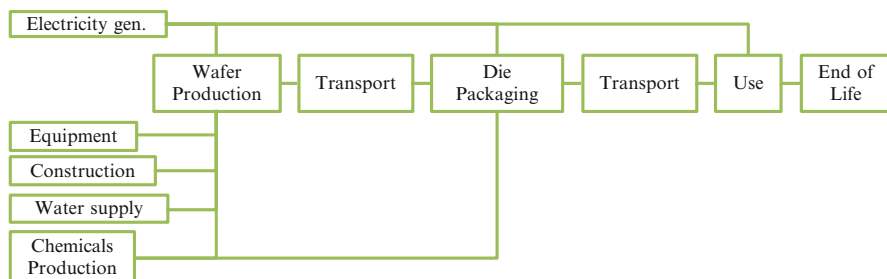


Fig. 2.1 Life-cycle stages of an integrated circuit

2.1.1 Mass and Energy Flow Modeling

Life-cycle inventory data for a semiconductor device may be developed using measured or estimated data taken at the facility or equipment level (aka, process level). An example of data taken at the facility level includes the total annual power usage by the fab, which could be determined by reading the building power meter. Data taken at the equipment level would include chemical usage in a particular process step, which would be metered at the inlet of the manufacturing equipment. The advantage of facility data is that it is more easily obtained; however, if the facility is used to produce different types of devices, the facility's resource uses and emissions must be allocated among those products. The choice of allocation method (economic, per unit, by mass) is essentially a qualitative decision and allocation introduces uncertainty into the LCI data. Equipment-level data, because it involves smaller mass flows, is more precise than facility data. In addition, it does not entail allocation when collected in a multi-product facility. However, basing an LCI entirely on process-level data requires testing power consumption and measuring chemical use and emissions for each and every step in the process flow of a device, which is usually not feasible. In addition, equipment data alone does not represent all of the energy used in production, as the facility systems which provide the cleanroom environment, process cooling water, ultra-pure water and manage emissions must also be accounted for in the LCI. When possible, collection of data at both the facility level and equipment level allows error checking. Power may be measured at the equipment level, for example, and chemical usage may be estimated using data from facility purchases. When both equipment-level and facility-level data are available, facility data and results from a process model based on equipment data may be cross checked against one another. Once data for both the resource uses and emissions of the production process are known, a mass balance of the system may also be used as an error checking tool.

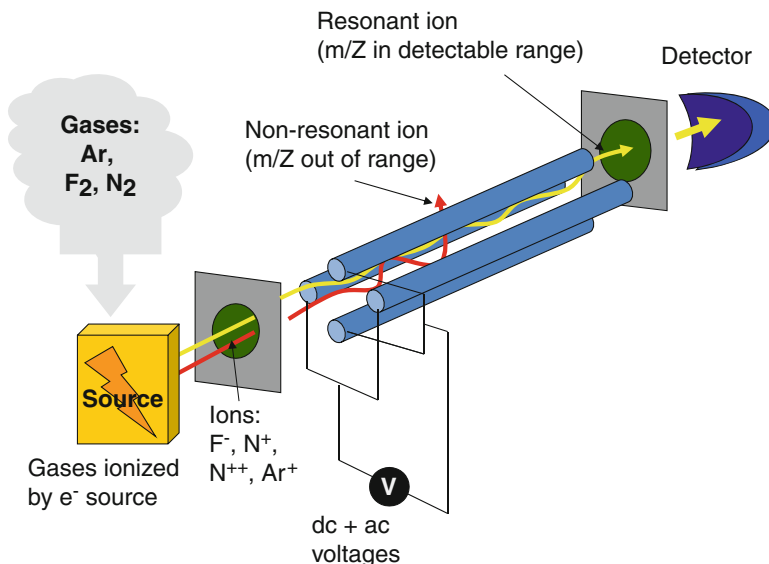


Fig. 2.2 Quadrupole mass spectrometry

2.1.1.1 Semiconductor Process Emissions Measurement

Mass emissions can be measured at the manufacturing tool chamber inlet and outlet using a combination of quadrupole mass spectrometry (QMS), Fourier transform infra-red (FT-IR) spectroscopy, and chemiluminescence-based fluorine gas analysis [109]. The combination of analytical techniques required is dependent on the possible range of chemicals present.

QMS is a popular mass measurement technique in which the molecular or atomic masses of species present in a gas medium are determined through ionization of the gas and subsequent electrical resonance and acceleration of the charged ions. As shown in Fig. 2.2, the four electrical poles carry ions towards the detector, but at any given moment, the generated charge only carries those ions with a particular mass to charge ratio. The poles sweep through a spectrum of charge, delivering a corresponding mass spectrum to the detector.

QMS is not sufficient to detect all materials present when multiple ionized species with common mass to charge ratios are present.

FT-IR spectroscopy is a powerful analytical technique which is used to identify and quantify the chemicals present in a medium based on their signature absorbance of the IR spectrum. A diagram of an FT-IR analyzer is shown in Fig. 2.3. A beam of collimated, polychromatic infrared light is split, such that one half is sent to a moving mirror, and the other half is directed toward a static mirror. These beams reflect back, are transmitted through the sample and are recorded by the detector. The recording taken over each full length of travel by the moving mirror is called an

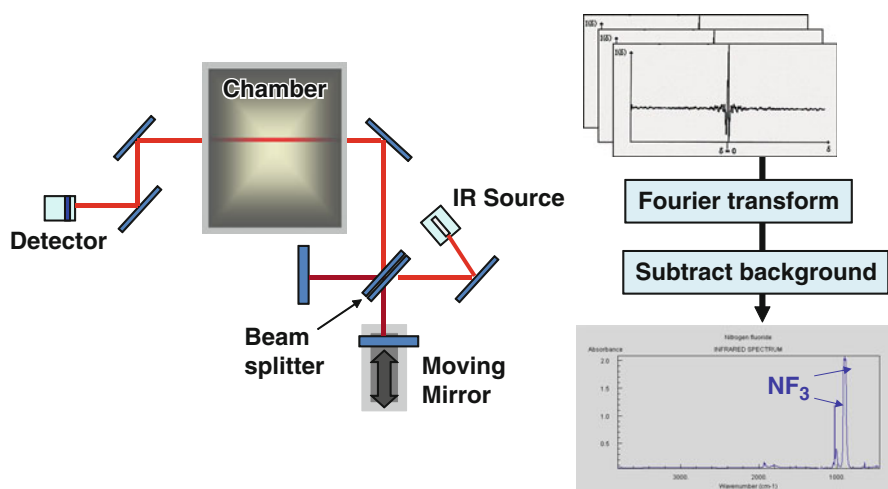


Fig. 2.3 Fourier transform infrared spectroscopy

interferogram. The set of all interferograms across the spectrum are transformed (via Fourier transform) from the physical length domain into the wavenumber domain, the background spectrum is subtracted, and the resulting spectrum can be used to identify the species present.

Water and carbon dioxide, which are both nearly ubiquitous and difficult to remove from vacuum environments, interfere with sizeable ranges of the IR spectrum. When the background spectrum, which contains the spectra representing the water vapor, carbon dioxide and other gases present in the chamber before the measurement is taken, is subtracted out, the differences between the background scan and the actual concentration of water and CO₂ present during the measurement scan result in noise and information loss over those spectral areas. This limitation, inherent in the technology, creates difficulties in the interpretation of species over the water and CO₂ spectral areas. QMS may be used in complement to FT-IR to overcome these informational losses, as QMS can quantify those species which cannot be accurately measured using FT-IR alone.

2.1.1.2 Facility Utilities and Equipment Design

As mentioned earlier, equipment-level data alone does not provide a complete picture of the energy use in wafer fabrication. When equipment data is used to compose the LCI, the energy and water use associated with the utilities delivered to the manufacturing tool must also be accounted for. These facility utilities include ultrapure water (UPW), process cooling water (PCW), nitrogen, clean dry air (CDA), and the cleanroom environment delivered by the heating ventilation and air conditioning (HVAC) system. The industry standard SEMI S23 which was

developed primarily for equipment life-cycle costing may be used to estimate the power demand and water use associated with these facilities.

SEMI S23 is a “Guide for Conservation of Energy, Utilities and Materials used by Semiconductor Manufacturing Equipment” created by the semiconductor industry association Sematech and defines a set of energy conversion factors with the general form:

$$ECF_{utility} = \text{Electrical energy (kWh)}/\text{Unit of Utility(m}^3 \text{ or kWh)}$$

S23 presents energy conversion factors ($ECF_{utility}$) for electricity, UPW, PCW, facility nitrogen, CDA, house vacuum, exhaust, and HVAC as a function of the heat load of the other utilities.

2.1.1.3 Emissions Factors for Electricity Generation

Values for the greenhouse gas emissions associated with electricity can vary from nearly zero in certain places, such as Brazil (blessed with significant hydropower resources) to above 1 kg CO₂eq/kWh in the most coal-reliant geographies such as China and parts of Eastern Europe. Within countries and regions producing ICs, the values range from Chinese production (near 1 kg CO₂eq/kWh) down to lows of Costa Rica (about 0.08 kg CO₂eq/kWh). Given a potential order of magnitude difference in the carbon intensity of electricity, and because a large proportion of impacts occurring in wafer production are due to emissions from electricity generation, impact totals are very sensitive to the electricity emissions factor used in the LCI. For these reasons, particular care should be taken to use a representative and accurate emissions factor for electricity in LCI of wafer fabrication.

2.1.2 *Government and Policy Methods Applicable to Semiconductor LCI*

PFCs are an important group of emissions from semiconductor manufacturing due to their high infrared absorption, long lifetimes and consequential global impact. These compounds are used in wafer etching and post-deposition chamber clean and include CF₄, C₂F₆, NF₃, and SF₆, among others. In addition, a variety of fluorinated ethers, alkanes, amines and aminoethers are used as heat transfer fluids [39, 124] in equipment cooling, and N₂O is used in certain deposition reactions. A table of the global warming potential (GWP) impact factors for some of the PFCs used in wafer fabrication are shown in Table 2.1 [63]. These chemicals have impact factors many thousands of times that of CO₂. As such, global warming impacts are an important impact category to consider in the production of ICs, and, as noted in Chap. 1, previous LCA of semiconductors indicate the direct emissions of PFCs from wafer fabrication are an important contributor to this impact category.

Table 2.1 Global Warming Potential (GWP) values for some PFCs used in semiconductor manufacturing [63]

Chemical formula	GWP
NF ₃	17,200
CF ₄	7,390
CHF ₃	14,800
C ₂ F ₆	12,200
C ₃ F ₈	8,830
CH ₄	25
SF ₆	22,800
N ₂ O	298
C ₄ F ₆	0.1–2 ⁱ

Note: GWP values reflect 100 year time horizonⁱ undefined under IPCC AR4

Because the climate change potential of PFCs is a global issue, the UN has developed models for predicting or estimating the GWP of emissions from semiconductor wafer fabrication operations, for use in regulation and voluntary policy.

The United Nations Intergovernmental Panel on Climate Change (IPCC) has developed tiered methods which may be selected on the basis of data availability. The methods range from the least rigorous estimation scheme, requiring minimum data (Tier 1), to the most rigorous and data-intensive method (Tier 2a). Here we will review the Tier 2a method as described the 2001 IPCC Good Practice Guidance document, which requires process-specific parameters.

IPCC Tier 2a Method - Process-specific parameters

Emissions of FC_{*i*} (E_{*i,p*}):

$$E_{i,p} = (1 - h) \sum_p ([FC_{i,p} (1 - C_{i,p}) (1 - a_{i,p} d_{i,p})]) \quad (2.1)$$

Where:

p = Process or process type (etching or CVD chamber cleaning).

$FC_{i,p}$ = kg of gas i fed into process/process type p (CF₄, C₂F₆, CHF₃, C₃F₈, c-C₄F₈, NF₃, or SF₆).

h = Fraction of gas remaining in shipping container (heel) after use.

$C_{i,p}$ = Use rate (fraction destroyed or transformed) for each gas i and process/process type p (in kg).

$a_{i,p}$ = Fraction of gas volume fed into in processes with emission control technologies (company- or plant specific).

$d_{i,p}$ = Fraction of gas i destroyed by the emission control technology. If more than one emission control technology is used for process/process type p , $d_{i,p}$ is the mass-weighted average of the fractions destroyed by those emission control technologies.

Table 2.2 IPCC Tier 2c standard values [62]

	h_i	$1 - C_i$	B_i	d_i
CF ₄	0.1	0.8	NA	0.9
C ₂ F ₆	0.1	0.7	0.1	0.9
CHF ₃	0.1	0.3	NA	0.9
C ₃ F ₈	0.1	0.4	0.2	0.9
c-C ₄ F ₈	0.1	0.3	NA	0.9
NF ₃	0.1	0.2	NA	0.9
SF ₆	0.1	0.5	NA	0.9

By-product emissions of CF₄ for FC_{*i,p*} (BE_{*i,p*}):

$$BE_{i,p} = (1 - h) \sum_p [B_{i,p} FC_{i,p} (1 - a_{i,p} d_{CF4,p})] \quad (2.2)$$

Where:

$B_{i,p}$ = Fraction of gas *i* transformed into CF₄ for each process type *p*.

$d_{CF4,p}$ = Fraction of byproduct CF₄ destroyed by the emission control technology used for process type *p*.

Values used in this method are listed in Table 2.2.

This method provides a way to estimate emissions from a manufacturing facility without performing emissions measurements on site, and using only facility data for chemical purchasing. The definition of this methodology also allows such estimates to be standardized and comparable.

The US EPA developed a technique for estimating the annual mass of pollutant emissions at the scale of the US economy [17]. The EPA method uses data on facility production capacity, combined with factors for PFC emissions per unit of silicon area (area of product) specific to the number of layers of active area in the device being manufactured. The mass-balance method used to determine the annual emission of fluorinated greenhouse gases in the EPA model follows the IPCC tier 2c method [62].

From the EPA:

PFC emissions in year *y* (PFC_{*i*}):

$$PFC(y) = \sum_{\tau(y)}^{T(y)} \langle e_{\tau(y)} \rangle S_{\tau(y)} \quad (2.3)$$

PFC(*y*) is the total for US PFC emissions in year *y*, for all PFCs from semiconductor processes:

$\langle e_{\tau(y)} \rangle$ is the population average emissions factor for linewidth technology τ .

$S_{\tau(y)}$ is the silicon consumed in producing linewidth technology τ in year *y*.

This method allows coarse modeling of a very large set of manufacturers, using a small set of well-designed, technology-specific emissions factors, combined with economic data which is available through public reporting (silicon purchasing data).

2.1.3 *Adaptation of Existing Semiconductor LCI Data*

While it is possible to develop an LCI for wafer fabrication using original data collection and estimation, LCA practitioners can also estimate the impacts associated with the production of a specific IC from published data in the literature. In this section, we will show how to tailor published LCI data for wafer production to estimate impacts related to a specific device. Care should be taken to match the subject of analysis with the functional unit of the previous study. When consulting the literature, be sure that the subject of the study found matches your device of interest in the following ways:

Product type: Is the integrated circuit a logic or memory device? If the device is memory, what type is it (DRAM, flash, EEPROM, etc.)? If the device is logic, is the product an analog or digital circuit? Computer processors and microcontrollers are normally digital circuits. If the product is a power or communications circuit, it may be analog.

Transistor configuration: Is the underlying transistor design a CMOS (complementary metal, oxide, semiconductor), bipolar or another configuration? Most digital ICs are currently built on CMOS-based circuits. Until recently, most analog circuits were built on bipolar transistors, which have been in some cases replaced by a CMOS-like bipolar implementation referred to as Bi-CMOS.

Year of production or technology node: A “technology node” is a term used to commonly refer to a set of production technologies specific to a device type (CMOS logic, DRAM and flash memory) and production year. The term was originally defined within the International Technology Roadmap for Semiconductors (ITRS) to allow a common shorthand within industry. The definition of the term “technology node” has changed over time, but the relevant definition for your year of production can be found in the ITRS report or update for that year [104]. If an older technology LCI is scaled up to represent a later IC, the results would likely overestimate in many impact categories if it is scaled per number of transistors, and may underestimate if scaled by area.

If the technology node is not known, then among chips of the same product type, year of production is an acceptable proxy.

Die size: The area of bare silicon die can be found through product specifications, or by physically grinding down the surface of a packaged chip to reveal the silicon device. The die surface is sometimes referred to as the “active area” of the chip. The die size is distinct from the package size, and may occupy anywhere from less than 10% to more than 80% of the package area.

Chip size: The dimensions of the packaged chip may be measured or determined from the chip’s specifications.

If your functional unit matches the above parameters of the study, that study’s results will be a good fit for your LCI. If the die size or chip size do not match, then

it may be possible to adapt the study by normalizing its results per die area and chip area, if the front and back end LCI are reported separately in the study. Normalizing only on the basis on the external chip dimensions is dangerous, as there is wide variation in the fraction of chip size occupied by the die. If a previous study of an IC with a high die-to-chip area ratio is normalized per chip area, it will overestimate results for chips with lower die-to-chip area ratios.

2.1.4 Use of Economic Input-Output LCA for Wafer Fabrication

Economic Input-Output LCA (EIO-LCA) modeling is a useful tool for estimating impacts on a per dollar basis for particular industrial sectors [54]. EIO-LCA is particularly useful in quantifying impacts for large, stable commodity industries, in which products of the sector category are uniform, interchangeable or may otherwise be represented well by average pricing and environmental impact data across the sector. Because the energy consumption is easily tracked using economic data, EIO-LCA is most effective for sectors in which environmental impacts are predominantly energy-related.

Because the semiconductor industry represents a wide variety of products, from light emitting diodes to high-end computer processors, the aggregate results available through EIO-LCA are not the most accurate for most products. Also, because of the rapid technological change in the industry, product types, prices, energy use and emissions per unit economic value may not be expected to be stable from year to year. For both of the above reasons, EIO-LCA is not an ideal tool for estimating impacts from semiconductor fabrication. In addition, unless an EIO-LCA model is specifically modified to include direct emissions from semiconductor manufacturing, EIO-LCA does not provide complete LCI data for semiconductor manufacturing.

Economic data and EIO models are very useful for cross-checking specific results from other methods of LCI development, such as average values for silicon consumption or energy consumption per unit of economic value. These comparisons can also be made without the step of economic normalization, allowing the uncertainties associated with product pricing to be eliminated from the comparison. For example, using census data on the sector's annual consumption of silicon wafer area and total annual energy consumption, an average value for energy use per unit area of silicon can be determined for comparison [2].

2.2 LCI of Chemical Production

In one early, influential paper on LCI of semiconductors, Williams presented an LCI of a memory chip and hypothesized that energy consumption in production of the high purity chemicals used in wafer fabrication would contribute considerably

to the life-cycle environmental impact of ICs [130]. Other studies have attempted to address this hypothesis, and one conference paper in particular has shown chemicals production to be a substantial fraction of energy use in production [55x], but as there is still a lack of publicly-available LCI of the high purity gases used in wafer processing, this conjecture cannot be repeated or substantiated for additional cases. Based on the available evidence, it seems that the production of chemicals is large enough that it should be accounted for as a part of the life-cycle of an IC.

In Williams' analysis of a memory chip, the author stated that chemical production and purification likely contributes a considerable amount to life-cycle energy consumption, yet due to a lack of representative data, the question of how much could not be definitively resolved [130]. In that study, the LCI data used for process chemicals production (typically in the purities of 99.999% to 99.999995%) was based on LCI data representative of industrial grade (90–99% pure), and was therefore considered a lower bound. Nevertheless, even using these low estimates, the LCI for production of chemicals amounted to over 4% of total life-cycle energy consumption. It is important to keep in mind that the subject of that study, a DRAM chip, had low use phase power consumption and thus a lower use phase contribution to life-cycle impacts, causing production impacts to be of higher relative importance. For ICs with higher use phase power, for example logic ICs, the upstream impacts would have a lower percentage contribution.

In a later study from Intel, a closer investigation of the energy associated with chemicals production is made as a part of a paper concerning boundary definition for semiconductor carbon footprint [55x]. Due to the large number of different chemicals used in production, LCI data collection for all chemicals was not possible, and the study defined a mass threshold for inclusion in the LCI, limiting the total number of materials considered to only 30. Unfortunately, by definition, the low-volume materials which are excluded are the most exotic, expensive and most highly processed chemicals used in manufacturing. Therefore, although the study accounts for 99% of the total mass of chemicals and gases used, the author states that there is uncertainty remaining about how much of the carbon impact is excluded when a mass threshold is used.

The author, Higgs, states that the LCI data for most chemicals included in the study represent standard, industrial grades rather than the actual high-purity grades used, but that for some gases, the existing LCI datasets were modified to reflect representative, high-purity electronics grade materials. It may be assumed that for some bulk gases purification is done on site, and that this aspect of the LCI for some gases could be accounted for as a part of facility data collection, which would be a high quality data source. One valuable finding from the paper is that, for those chemicals modeled, purification to electronics grade required a CO₂ impact of 20–1,000% higher than the initial industrial grade. While the effort made to account for purification of process chemicals was commendable, and provides valuable insight into the range of values potentially associated with data gaps, purification modeling was only possible for a few materials in this study, and so the baseline LCI totals for chemicals production may still underreport. The missing purification data is addressed with an upper bound, which is estimated using the modeled purification

process data as a proxy for purification of the remaining high-purity chemicals. The report indicates that, using these LCI methods, the upstream production of chemicals contributes 23–28% of GWP impacts in semiconductor production.

Despite further inquiry on this subject, including some attempts to develop LCI data for high purity chemicals using theoretical models [74], the lack of publicly-available LCI data for the high-purity gases and specialized chemicals used in wafer fabrication limits the ability to model this life-cycle stage.

2.3 LCI of Infrastructure

Semiconductor fabs are large, extremely expensive capital projects. The cost of building construction and equipment for a new fab topped one billion dollars in as early as 1997 [46], and can currently exceed 10 billion dollars. It is clear that a significant amount of economic activity and material use is involved in the development of a wafer fab, and it is tempting to account for this aspect of semiconductor fabrication using LCI data from the construction industry, but fab construction is not representative of an average construction project. Possibly because aspects of the cost incurred in fab construction are intellectual, non-physical costs, if construction LCI data is applied per dollar of activity, it would be representative of a much larger physical facility. The potential to over-predict impacts is amplified when impacts are depreciated over the useful life time of a fab, which can be typically 10–15 years, rather than the lifetime of an average building, which can be 20–50 years. Indeed, the total potential lifetime of the fab in a secondary use as a non-wafer fab building may be the same as any other large building. This uncertainty about fab lifetime and the absence of representative LCI data for a semiconductor fab construction make quantification of this life-cycle stage difficult. In the LCI presented in this paper, economic input-output data for the construction industry is used as an upper bound for impacts in this life-cycle stage.

PAS 2050, the British standard which outlines the methodology required for LCA in environmental reporting, does not require accounting for capital infrastructure, such as the building and equipment used in production. For this reason, as well as the uncertainty in evaluating the indirect impacts of fab construction, this life-cycle stage is commonly omitted from analysis.

2.4 Modeling Energy Consumption in the Use Phase

Operational energy efficiency at the CPU has shown dramatic improvement over the past several years, yet brings continued challenges, as operational power is inextricably linked to IC performance. While power consumption per transistor falls with scaling, the total number of transistors per chip increases to deliver

greater performance in each successive generation. Chip-level power management can be governed by a wide variety of choices made in the definition of an IC product's process technology, beginning with the choice of substrate (silicon-on-insulator vs. bulk silicon wafers), through to the choice of packaging and design for heat dissipation. As the process technology choices which affect chip power consumption also affect performance, and because these process technologies are continuously evolving, it is important to take care in assumptions made for power consumption in the use phase of an LCI model. A high-performance logic chip from one year cannot be expected to have the same power ratings as an equivalent product just two years earlier.

In many cases, the use phase is the dominant source of environmental impacts for integrated circuits among the life-cycle stages. Some ICs, like sensors and some types of memory, operate at very low power or are active with rare intermittency. For these products, use phase energy consumption may be modest and the manufacturing phase becomes the primary concern. Nevertheless, apart from these exceptions, the use phase is an important life-cycle stage for the broad majority of ICs for use on most electrical grids throughout the world. Most integrated circuits which consume more than a few watts in operation will have a use phase which dominates life-cycle energy consumption.

The relative impacts of the use stage are dependent on not only the power consumption of the chip, but the emissions factor for electricity at the location of use as well as other factors which come into play at the level of the electronic product (power supply efficiency, availability of product idle and standby states, and software-integrated power management) and the use phase scenario (the frequency and intensity of use).

2.4.1 Specifying the Use Phase Scenario: Location, Time in Operation and Utilization Rate

The use phase scenario will define the location, frequency and length of use, as well as the utilization rate being demanded from the IC.

Depending on the electricity mix in the location of use, when use phase operation is the largest consumer of primary energy resources, it may or may not also be the largest contributor to GWP, acidification, ground-level ozone formation, water demand and other environmental impacts. When use occurs in a location with an exceptionally low emissions factors (e.g. Brazil, 73 g CO₂eq/kWh) or water consumption factors for electricity, other use phase impacts besides primary energy consumption are mitigated. Because there is such a wide range of emissions factors for electricity among all of the electrical grids in the world, the range of potential impacts for a certain chip's operational life can span over many orders of magnitude depending on the location of use. The choice of a representative emissions factor for electricity in the use phase, and understanding of the location or mix of use locations, is thus very important to an accurate life-cycle assessment for IC.

Frequency and duration of use are intuitive to grasp and are commonly addressed in LCA of any energy-using product. The total time in operation will be defined by the number of hours of active use per day, number of days per year, and years in the product's lifetime. Warranty reports, when available, can be a good source of information on the average lifetime of a product group, such as laptops or netbooks. In addition to the time in active operation, an IC in most cases will spend time in other operational modes, such as stand-by or idle. Because, in many cases, an IC will spend more time in idle or standby than in active operation, it is important to also quantify the energy consumption (the period of time and power consumption) in these other modes.

The utilization rate, the average fraction of the maximum power used in a given application, is a less intuitive but equally important aspect of an IC's use phase. Unlike most other electric products, the rated power for a logic chip will often be the maximum power demand. In normal operation, the chip will almost never require the maximum rated power. Instead, an IC will use the necessary fraction of its total computational, memory, control, or communication resources, and demand the associated fraction of its rated power. On average, for example, a central processing unit (CPU) may only use 15% or 30% of its rated power.

The utilization rate or application rate of the chip will be defined by the use case. For memory, the power required by the chip to deliver streaming video is different from the power used to support the memory demands of a typical office application suite. Similarly, a processor operating in a datacenter server will employ a much higher fraction of its computational power on average than one in a laptop. There are different energy efficiency or power consumption benchmarking tests for different IC device types, and these testing procedures can change frequently to adapt to new circumstances (i.e., changes in software, communication standards or peripheral devices). One example for central processors and chipsets is the SYSMark standard.

2.4.2 System-Level Factors

Because most any chip which is being used in a computer, laptop or server is being delivered DC power through a power supply, the efficiency of that power supply's conversion from AC to DC power has a large influence over the chip's use phase energy consumption. If, for example, a power supply has an efficiency of 74%, the chip's use phase energy demand, when considered in the context of the integrated product, will be 1.35 times the chip's direct power demand. In a computer with a 90% efficient power supply, the same chip would demand 1.11 times the chip's own energy demand, or 18% less energy over its life-cycle.

If the functional unit of study is used in a server, other system-level factors which arise at the level of a data center may be of concern. For example, the IC's excess heat dissipation will affect the heat load in the data center, and therefore the center's cooling requirements and associated energy consumption.

2.4.3 *Software*

In the early 2000s, operating system-integrated chip power management (aka, advanced or dynamic power management) was introduced, which allowed software to hibernate or shut down the CPU when the user was inactive. Windows 2000 and XP both integrated advanced power management but neither of these versions of Windows had advanced power management settings enabled by default, and the functionality was often not enabled by the user. In a 2007 market research study, as many as 60% of computer users in the US did not shut down their computer at the end of the day, resulting in the needless emission of roughly 14 million tons of CO₂ that year [5]. In Windows 7, the default settings for shipment were for lower power consumption, which supported wider use. The default setting, rather than the available functionality, is a critical aspect of power management, and also of the life-cycle impacts of an electronic product.

The influence of software over the life-cycle impacts of computing also extends into other life-cycle stages beyond the use phase. Software's demand for increasing memory and computational power drives the obsolescence of a computer, specifically through the demand for more advanced logic and higher capacities of DRAM. By driving ICs into retirement, ever bulkier and more memory-intensive operating systems and applications not only trigger the impacts associated with EoL to occur at an earlier point in time, but also obligate production of their replacements. The role of software in the lifetime of electronics is easy to let slip into the background. In the case of LCA of ICs, software is usually not considered when the functional unit and boundary of a LCA of ICs is set, but given the influence of software over life-cycle impacts, this practice should be reconsidered where possible.

2.5 End of Life

The most evident end-of-life (EOL) impacts from integrated circuit chips are lead emissions, when the solder or wire-bonding materials contained inside the packaged chip or used to attach the chip to a board contain lead, a potent neurotoxin. EOL lead emissions have been mitigated since 2006, when the EU's Restriction on Hazardous Substances (RoHS) regulation banned the sale of products containing leaded solders in the EU. Studies of EOL electronics have identified and quantified other end effects of computer disposal through modeling as well as measurement of toxic compounds present near informal recycling sites [21, 28, 132, 133]. These other toxins (dioxins, brominated flame retardants, and other bio-accumulative or toxic materials) largely represent emissions from the breakdown or combustion of a computer's more massive components, such as the printed wiring board and plastic housings. While there may be harmful emissions besides lead from the decomposition of a logic chip, these have not yet been identified or measured.



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Life-Cycle Assessment of Semiconductors

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