

Chapter 2

Materials and Interfaces in Microsystems

2.1 Levels of Interconnections, Typical Stress Factors and Related Failure Mechanisms

The interconnections in electronic systems are traditionally divided into four (or more) categories: (i) interconnections on the IC-level, (ii) interconnections on the package level, (iii) interconnections on the board level and (iv) interconnections on the system level [1]. Since, the system level is product or application field-dependent, only the three levels, which are generic to all products, are considered here. Each level is characterised by typical materials and manufacturing processes. In addition, both the internal and external stresses vary between the levels. However, the ongoing trend to develop new solutions with higher integration has fused these interconnection levels closer to each other both dimensionally as well as technologically. Currently, materials and manufacturing methods that were previously used in IC (frontend) processes are utilised also in system level packages [2]. Since microsystems are heterogeneous structures (see Fig. 2.1) composed of many materials where components are integrated by different kinds of interfaces, the reaction between the materials and their environment decides manufacturability, functionality and reliability.

As can be seen from Fig. 2.1, within volume of less than 0.001 mm^3 there are materials from all basic material groups; polymers (epoxy and polyimide), insulators (SiO_2 and SiN), semiconductors (Si) and metals (Al, Cu, Ni, Sn and Ti) that all behave differently under varying temperature or stress states. Therefore, understanding on materials' compatibility is fundamentally important and provides the basis for comprehending the ever increasing electrical, thermal, thermo-mechanical and environmental challenges that must be faced.

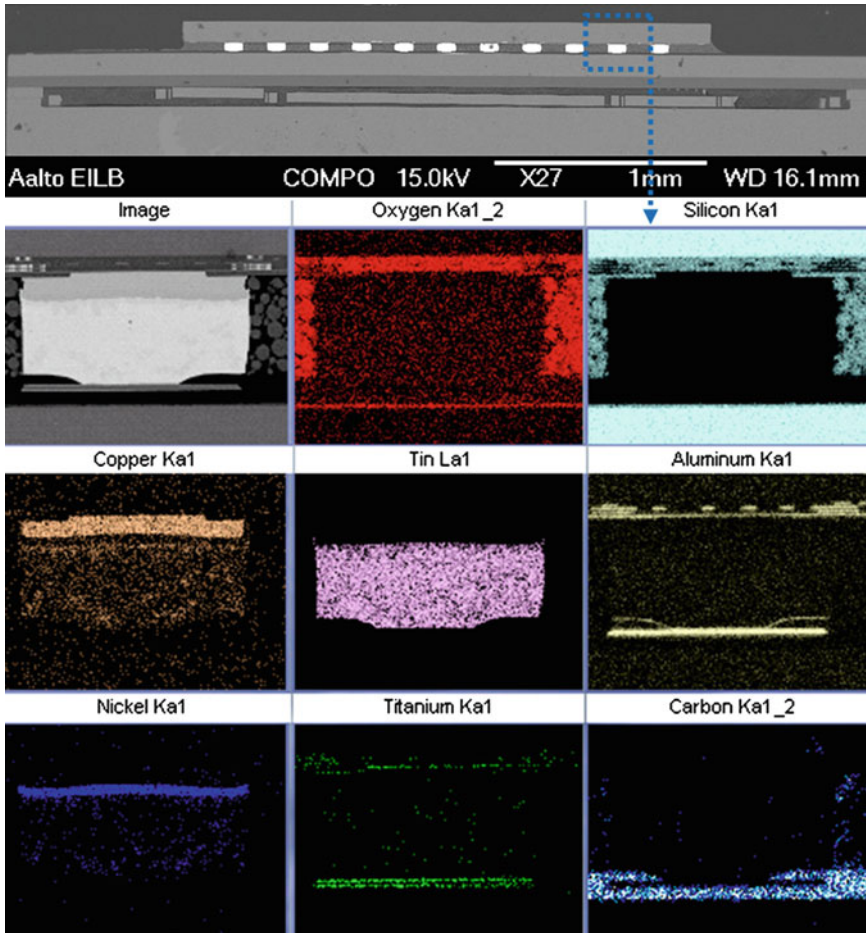


Fig. 2.1 SEM micrograph and EDS element maps from MEMS accelerometer with integrated ASIC

2.1.1 IC Level

Practically all microelectronic devices are based on “components” that are fabricated by employing metal-semiconductor contacts that are integrated with metallic connectors insulated by ceramic or polymer layers as shown in Fig. 2.2.

Semiconductor devices are based on a vast variety of thin conducting and insulating layers in contact with each other as well as to semiconducting materials [3]. Therefore, the interfacial compatibility between dissimilar materials is especially important on the IC-level. Typically, the main manufacturing and reliability challenges are related to the polycrystalline conducting thin films, which provide the electrical contacts between the devices and to the outside world via the packaging. It is to be noted that the physical and chemical properties of thin films

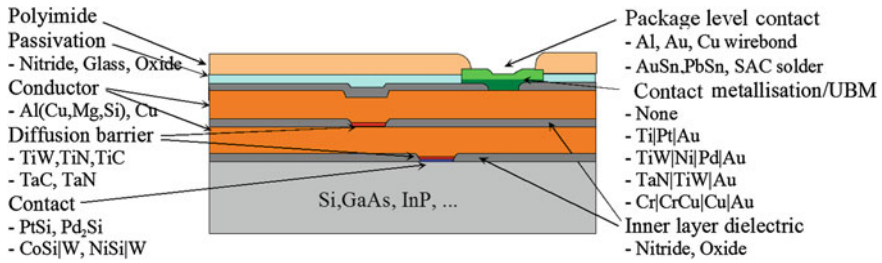


Fig. 2.2 Simplified schematic representation of typical frontside material solutions from an electronic component. (N.B. Layers are not in scale.)

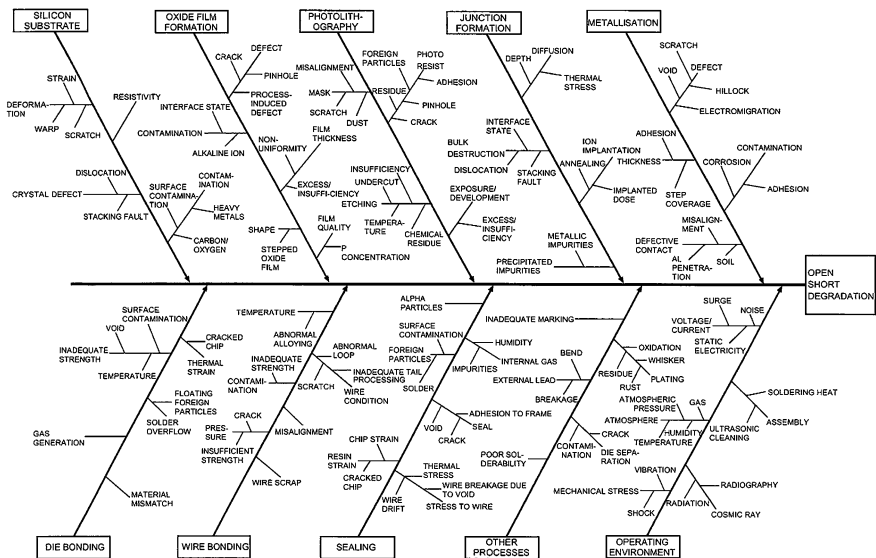


Fig. 2.3 Failure mechanisms in IC and packaging levels

can differ significantly from those of bulk materials. This, on the one hand, provides a huge amount of possibilities to tailor the material properties, but, on the other hand, makes the fundamental understanding of materials scientific aspects even more important, in order to avoid unwanted events. The key issue in comprehending the use of thin film structures is through understanding on diffusion and reaction mechanisms as well as the electrochemical and electromigration properties of these materials. The huge range of different factors affecting the failure mechanisms on the IC and packaging level is illustrated in Fig. 2.3 by the fish-bone diagram.

The above described aspects are mainly related to “traditional” ICs and the relative importance of these aspects can be quite different when one considers for instance high power or RF-components as well as LED or MEMS systems. For

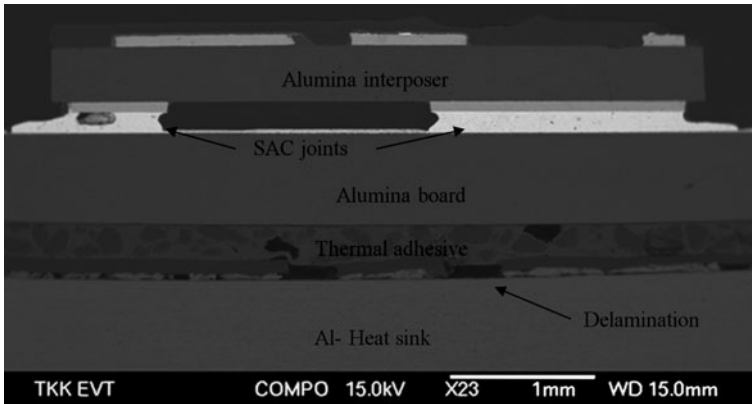


Fig. 2.4 Heat-sink attachment failure in high-power LED product after thermal cycling $0 \Leftrightarrow 100^{\circ}\text{C}$, 2 h cycle time and 500 cycles (N.B. The LED component is not seen in this section)

example, the major challenges in RF-circuits and modules, in addition to increasing power consumption and difficulties in thermal management, are related to low noise and high linearity issues. Therefore different approaches must be taken for both manufacturing methods and materials selection points of view. On the other hand, the performance and reliability of LED components are greatly dependent on thermal management since high operating temperatures at the LED junction adversely affect performance, resulting both decreased output and lifetime. It is to be emphasised that the majority of LED failure mechanisms are temperature-dependent. When designing lighting systems using high-power LEDs, the most important guideline is to minimise the amount of heat that needs to be removed and enhance the thermal conductivity between the heat sink and the LED. Since the LED components are typically very reliable, it has been shown that many lighting applications the packaging or, especially, board-level interconnection reliability defines the lifetime of the product. Figure 2.4 shows a cross section from a high-power led-module after 500 cycles of thermal cycling, where the thermal adhesive between the alumina board and aluminium heat sink has failed. In addition, it is important to separate the LED drive circuitry from the LED board so that the heat generated by the driver will not contribute to the LED junction temperature.

2.1.2 Package Level

As was already mentioned above, the integration of microsystems is continuously blurring the distinction between the interconnection levels. However, since on the packaging level the volume drivers have continuously shifted towards consumer electronics, many material and manufacturing solutions, like ceramic packaging,

Fig. 2.5 Schematic presentation of typical die attach structure and commonly used materials

Integrated circuit	Silicon, GaAs,...
Adhesion layer	Ti,TiW,Cr,...
Barrier layer	Ni, NiV,Ni(P), Co, Co(P), NiCo,...
Oxidation protection layer	Au, Pt,...
Die attach material	AuSn20, PbSn10, Ag-epoxy, Ag-glass,...
Substrate metallization	ENIG, ENEPIG, Cu/OSP, Cu/Sn, CuAg,...

must be ruled out due to cost factors. Therefore, in this “cost-performance” category the methods used and developed are based on the low-cost polymer and solder materials and technologies.

Die attach (also known as die mount or die bond) is the process where the silicon chips are mounted on the substrate. The most commonly used methods are adhesive or glass bonding and soldering or eutectic die attach. In addition to mechanical support, the die attach materials also provide thermal and/or electrical conductivity between the die and the package thus affecting the performance of the device during field operation. When solder materials are used in the die attach, backside metallisation of the semiconductor device is required. The backside metallisation is typically a multilayer structure composed of an adhesion layer, a barrier/wetting layer and an oxidation protection layer (See Fig. 2.5).

The requirements of a die attach material are application-dependent, but typically include that (i) mechanical strength must be maintained up to 150°C, (ii) the attachment process temperature must not affect the die function and (iii) the attachment should withstand board-level assembly processes (temperatures up to 260°C for a few minutes), the absorption of continuous and cyclic mechanical and thermomechanical stresses, etc. The most common stress-related failures during product life are die/adhesive cracks, passivation cracks, pad delamination and corrosion [4]. Figure 2.6 shows an example of a cracked Si-chip due to lack of mechanical support of the die attach film during wire bonding in a stacked die application.

Wirebonding has been the most commonly used method for connecting ICs to packages or other substrates already now for many decades. The most important advantages are related to the flexibility of the manufacturing process, long experience and reliability. Wirebonding can also be considered as low-cost from an equipment and materials used point of view. There are three methods used: Thermocompression (T/C), Thermosonic (T/S) and Ultrasonic (U/S) (see Table 2.1). Depending on the method, the shape of the bond can be either “ball-wedge” (T/C- or T/S-methods) or “wedge-wedge” (U/S-method). Aluminium (Si or Ge alloying) wires are typically used with the U/S-method. T/C- and T/S- methods typically use Au-wires, but Pd, Cu and Ag are also possible.

The challenges in wirebonding are frequently related either to bonding process parameter control (temperature, pressure, etc.) or to reliability problems caused by high operational temperatures or aggressive environments. Figure 2.7 shows optical micrographs from a typical process-related problem, where the Al pad has been consumed locally by the IMC-reaction with Au-ball due to excessive bonding temperature.

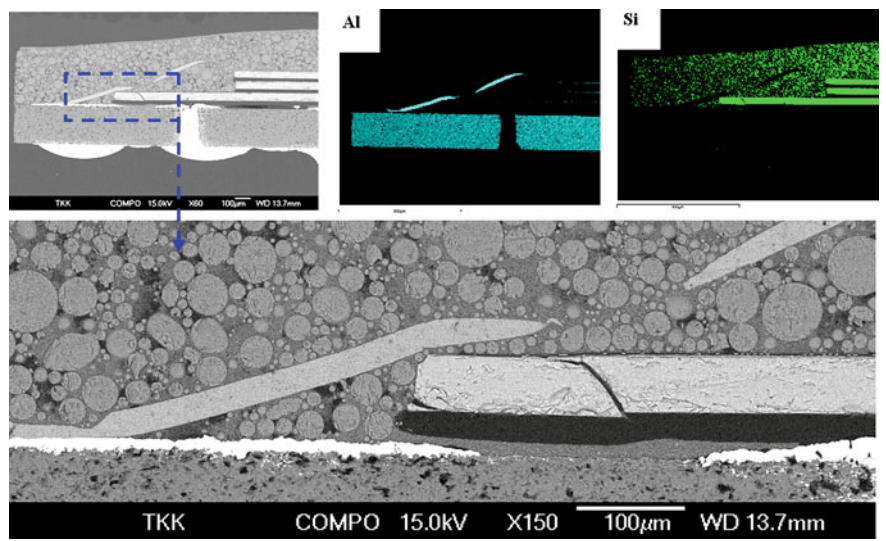


Fig. 2.6 Cracked Si-chip due to lack of mechanical support from die attach film

Table 2.1 Three wirebonding methods and their typical properties

	Thermocompression (T/C)	Thermosonic (T/S)	Ultrasonic (U/S)
Definition	Contact between wire and contact pads is based on plastic deformation and interfaces	Ultrasound is used to assist the disruption of the oxide layers	Ultrasound is used together with pressure but no external heating
Temperature	300–400°C	150–200°C	Room temperature Bond interface ~70–80°C
Pressure	100 g/contact area		
Time	0.1 s	5 ms < t < 25 ms	t < 25 ms
Bond type	“ball-wedge” Factors affecting reliability: Surface roughness and voids, oxidation, adsorbed impurities, moisture	“ball-wedge” Used especially when wire bonding thick-film hybrid substrates	“wedge–wedge” Problems in “wedge–wedge” is that both contacts have to be aligned in the same direction
Wire	Usually Au	Au, also Cu and Pd	Al

Two typical operational stress-related reliability problems are shown in Figs. 2.8 and 2.9. Local corrosion of an Al pad in a Cl^- containing environment can be clearly detected from Fig. 2.8. The EDS element maps show higher chlorine and oxygen content at the surface pits. Figure 2.9 shows the well-known “purple plague” problem, which is the formation of an excessive amount of AuAl_2 intermetallic at the interface [5]. The growth of AlAu intermetallics is often accompanied by the formation of so-called Kirkendall voids, which are caused by

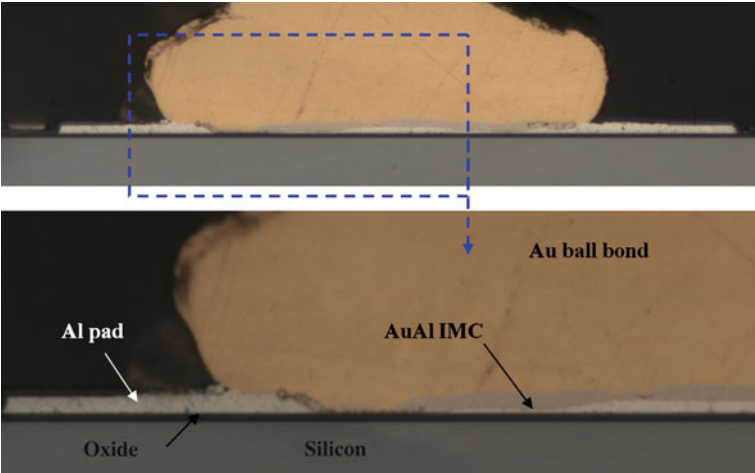


Fig. 2.7 Au ball | Al pad interfacial reaction during the bonding process

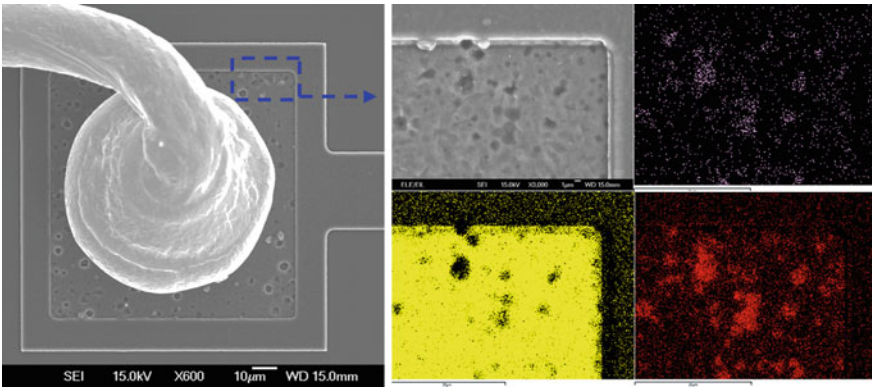


Fig. 2.8 SEM micrograph from local corrosion at the Al-bond pad together with EDS element maps (violet_chlorine, yellow_aluminum, and red_oxygen)

the differences between the intrinsic diffusion fluxes of Al and Au, i.e. Au moves faster than Al and thus the vacancies accumulate on the Au side.

Tape Automated Bonding (TAB) technology was developed as a low-cost method during the 1960s for small scale integration (SSI) circuits to replace wirebonding. During the 1980s, the use of surface mount technology made it more popular also in high I/O components (see Fig. 2.10). The TAB process uses typically bumped chips, which are first bonded to metallised tape fingers (ILB, Inner Lead Bonding). After ILB the chips are tested and/or encapsulated before singulation and outer lead bonding to a substrate or card.

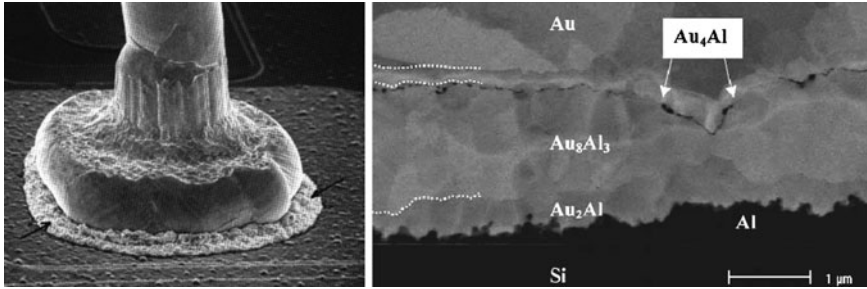


Fig. 2.9 Left “purple plague” and right AuAl IMC layers [5]

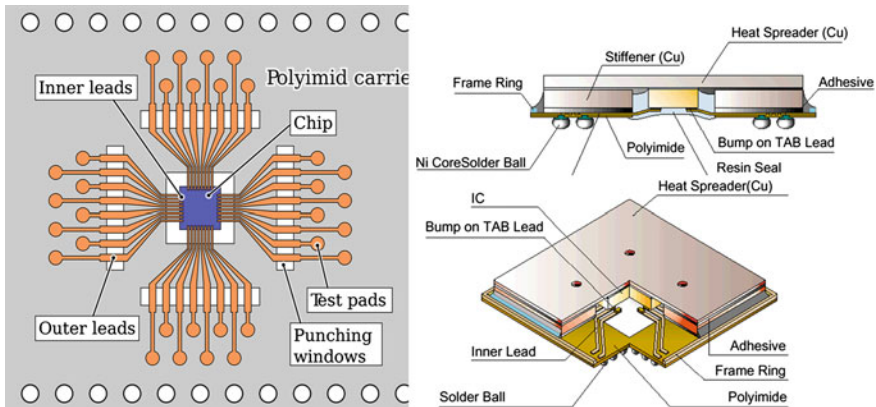


Fig. 2.10 TAB used in a component package

Flip-chip is defined as a bare chip mounted on the substrate upside down, the active side towards the substrate. Flip-chip technology is the so-called Area Array method, which means that the whole IC area can be used for interconnections. Therefore flip-chip provides higher interconnection densities than both wire bonding and TAB. The I/O contact pads are located under the chip, and connections to the substrate can be made with various interconnection materials and methods (see Fig. 2.11), such as solder bumps, conductive adhesives or Stud Bump Bonding (SBB). The substrate can either be a component (like CSP or BGA) interposer or a mere PWB (Flip-Chip On Board, FCOB), ceramic (FCOC), glass (FCOG) or flex (FCOF) substrate.

From an electrical performance point of view flip-chip is also a superior direct chip attachment method. Due to the advantages of the technology it is commonly used in microprocessor components. However, as a result of the small height of the solder interconnections, which are the most commonly used, the large difference in the coefficients of thermal expansion (CTE) between the Si-chip and the organic substrate cause reliability problems. Large strains are already formed during the

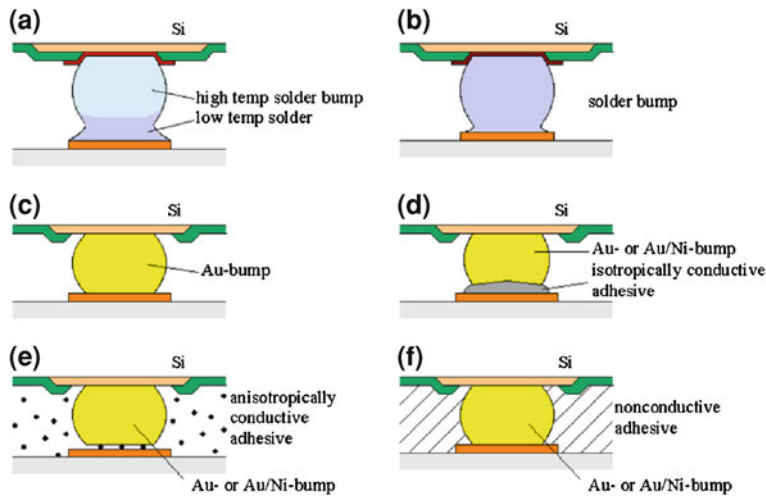
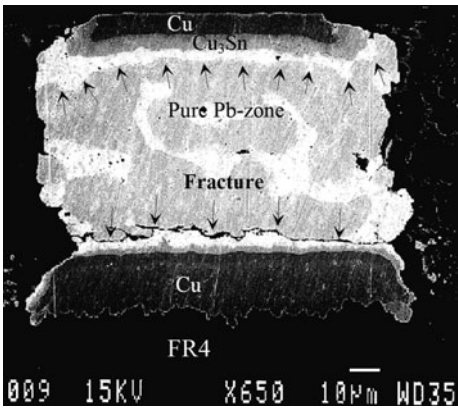


Fig. 2.11 Comparison between different flip-chip connection types [6]

Fig. 2.12 Fatigue failure in flip-chip solder joint



cooling in the soldering process and changes in operational temperature lead to thermomechanical low-cycle fatigue. Figure 2.12 shows a fatigue failure from a flip-chip interconnection.

Another challenge related to solder interconnections in flip-chip joints is caused by the small solder volume. During the soldering process (and consequent high-temperature use) a relatively large fraction of the solder material can be consumed by the interfacial intermetallic reactions with component and/or PWB metallisations. A particularly challenging situation is faced if only one element (usually Sn) is consumed, but the other element (like Pb or Bi) takes no part in the chemical reactions. This leads to local enrichment of the non-reactive element near the interface, which can thus become very brittle. This small volume effect can also be seen in Fig. 2.12, where the fatigued crack clearly follows the interface between the IMC-layer and Pb- enriched area. [7]

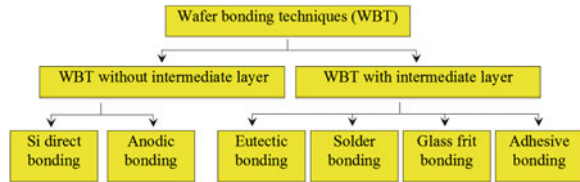
Table 2.2 Properties of packaging materials [8]

Material (wt%)	Melting point/ Softening temp. (°C)	CTE (ppm/K)	Thermal conductivity (W/mK)	Electrical resistivity (Ωm)	Young's modulus (GPa)
Alumina	~2,000	6.5	37	$>10^{14}$	370–410
AlN	~2,800	5.7	140–220	$>10^{13}$	350
SiC	~2,500	3.7	270	$>10^{13}$	420
Glass	Soft >450	5.3	0.4–1.3	7.5×10^{11}	
Alloy 42	1,425	4.5–5.5	14.6	72×10^{-8}	148
Nickel	1,455	12.7	91	6.8×10^{-8}	214
Copper	1,084	16.8	386	1.7×10^{-8}	115–130
Au80Sn20	280	16	57	16.4×10^{-8}	59
Au97Si3	370	10–13	94		83
Pb95Sn5	305–315	29	32.3		7.4
Ag epoxy	Soft. >300	30–55(below T _g)	0.8	1.4×10^{-6}	
Sn95.8Ag3.5Cu0.7	217			13×10^{-8}	56

Moulding/Encapsulation/Underfilling is typically the final manufacturing step in a non-hermetic packaging process. Hermetic packaging requires the use of ceramic, glass or metallic materials that makes this approach too expensive in consumer electronic products. Plastic encapsulation also provides lighter and smaller packages compared to ceramic counterparts. The major difficulties are related to the process, which is still not well characterised or optimised and reliability. The complexity of the rheokinetics of thermosetting encapsulants, the complex mould geometries and conditions can lead to incomplete filling of the mould, void formation and transport, wire sweep and die pad shift.

The main purpose in both (hermetic and non-hermetic) packaging methods is to provide protection to circuits from damage during next level assembly the service life environmental stresses. In addition, the package provides a path for the thermal energy to be dissipated from the IC. Table 2.2 shows typical physical, mechanical and electrical properties of packaging materials

Wafer Level Packaging (WLP) defined as a technology, where packaging and interconnections are fabricated on the wafer prior to dicing and no other packaging steps are performed prior to board assembly. The process eliminates a few conventional packaging steps like die attach and wire bonding and thus provides batch processing to lower costs, streamlining of handling and shipping logistics, minimal form factor and the avoidance of known good die (KGD). It also facilitates faster time-to-market. Furthermore, when wider pitch is achieved it allows for wider UBM, taller bumps, and thus better joint reliability. The major challenges of WLP are related to (i) an infrastructure that is not fully established, (ii) the high cost for poor yield wafers and wafer bumping, (iii) die shrink strategies and, (iv) in particular, solder joint reliability (since underfilling cannot be used in all applications). The development of so-called pre-applied or wafer level underfills may provide solution for this in future. Another important question is whether the

Fig. 2.13 Wafer bonding techniques

package manufacturer is an IC or bumping house. Currently WLP applications are typically passives and discrettes as well as RF- and memory components where the I/O amount is up to a few hundreds, but the WLP approach is rapidly expanding to logic ICs and MEMS components (already shown in Fig. 2.1).

Wafer bonding techniques have recently become more attractive in wafer level packaging of MEMS components since they are able to meet the versatile requirements placed upon them: like for instance, a vacuum inside an hermetically sealed package or simultaneous protection from the environment while at the same time alloying chemical, pressure, flow, optical or other measurement, detection or actuation. Wafer bonding (see Fig. 2.13 and Table 2.3) includes direct bonding methods like anodic and fusion bonding and methods that utilise intermediate metal or insulator layers. Generally, it can be stated that wafer bonding is challenging since the thermal expansion of the wafers produce alignment problems. An even bond over the entire bond-surface, and clean bond surfaces are required.

Anodic (or electrostatic) bonding utilises temperatures of up to 550°C and high voltages of up to 2,000 V to obtain a chemical process, which creates a permanent joint between the silicon and sodium rich glass. This way an insulating, biocompatible and highly hermetic package without CTE problems is achieved. However, due to the relatively thick glass layers needed it is not optimal for thin-film packaging. In addition, surface roughness better than 500 nm is required. Fusion bonding is based on formation of chemical Si–OH (hydrophilic) bonds or Si–H (hydrophobic) bonds. Fusion bonding requires extremely smooth (<50 nm), clean and flat wafers and utilises temperatures up to 1,100°C. The main advantages of fusion bonding are strong connection due to covalent forces, relatively free choice of wafer material, frontend compatibility, fast process and wide process window. The main challenges are related to cleanliness and surface quality requirements and that the standard annealing process is not CMOS compatible.

Metal bonding methods, which are most common in MEMS packaging, include solder bonding, eutectic bonding, thermocompression bonding (TCB) and rapid thermal processing (RTP). They are used to seal “rough” surfaces at low temperatures. In eutectic bonding two thin films on both wafers form an alloy. This typically is achieved while one thin film (pure metal) in contact with the alloy on the second wafer is heated above the melting point of the alloy. Alignment, temperature and bond pressure need proper control. Also electrical feedthroughs may cause problems and wafers are limited in the topography. In glass frit bonding the printing and alignment are required before the wafers are bonded using a combination of pressure and heat. The glass frames serve as an adhesive and

Table 2.3 Wafer bonding techniques

Method	Material	Temperature (°C)	Comments
Anodic	Glass to Si-glass	180–550	Small amount of surface roughness hermetic
Fusion	Si to Si	>800	Very small surface roughness. hermetic
Eutectic	Au–Si, Al–Ge, Au–Sn	Typically 260–420 system-dependent	“Rough” surfaces, hermetic
Solder	AuSn, PbSn, InSn or AISi to Si and glass	System-dependent from 118–800	“Rough” surfaces. hermetic
Thermocompression bonding (ICB)	Au or Cu to Si	25–250	High force required hermetic
Rapid thermal processing (RIP)	Al to Si ₃ N ₄	750 Short duration	Hermetic
Adhesive	SU-8, BCE, PI	<300	“Rough” surfaces, non-hermetic
Glass	Reflowed glass frit	375–410	“Rough” surfaces hermetic

sealant between the wafers. The main advantages are related to a very flexible and economical process, a relatively free choice of wafer material, the fact that the bond surfaces do not need to be very smooth and that the glass adapts itself to the wafer topography. The main disadvantages are related to the relatively “dirty” process and small process window.

Printed circuit/wiring boards (PCBs/PWBs) and interposers can also be considered to belong to the package level. The miniaturisation, environmental aspects and increased performance of the modern packages have forced the evolution of printed circuits too. The current requirements for PCBs include high density wiring, bare chip attachment capability, smallness of size, a light and thin form factor, high reliability, cost efficiency, functionality at high frequencies, high thermal conductivity and an environmentally friendly manufacturing process and recycling. Generally PCBs have three main functions: (i) To support the mechanical structure of the device, (ii) To be a foundation for electrical connections between components and (iii) To help in removing thermal power. Since the PCB is one of the most expensive components in an electronic device, it is necessary to ensure the manufacturing quality of this component. On the other hand the reparability of a PCB after assembly is usually impossible or at least much more difficult than repairing (changing) an individual component/solder joint. It is also to be emphasised that there are not “standard” PCBs for multiple customers and products but each board represents an application-specific design. PCBs can be classified with different means for instance according to manufacturing process or based on the dielectric or core material. As seen from Fig. 2.14 in the most commonly used classification the metal core printed circuit boards (MCPCB), which are typically used in thermally demanding applications like LED modules, are included under rigid organic boards. [9]

Fig. 2.14 Classification of printed wiring boards

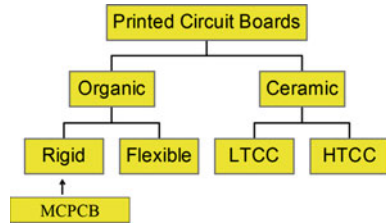
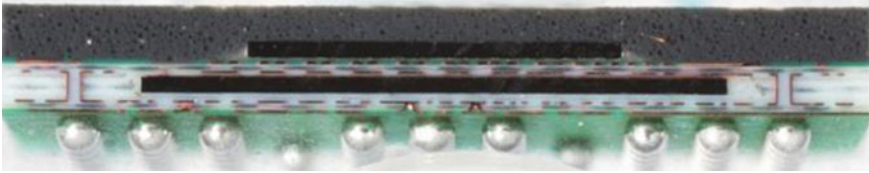


Fig. 2.15 iSiP structure with one embedded component. Substrate top layer is utilised by one wire-bonded die, moulded (Courtesy of Imbera Electronics)

The advances in substrate technology play a crucial role in achieving the aim of microminiaturised multifunctional systems. Traditionally, the substrates have played a passive role, but currently the embedding of active components in PCBs is becoming a significant option.

The embedded components are currently used in various application areas, today mainly hand-held consumer electronics since that can provide miniaturisation/form factor reduction (x – y , and thickness) simultaneously with excellent electrical and thermal performance. Embedding techniques for ceramic substrates were developed already during the 1980s, but due to high material and process costs their applicability was limited to only a few high performance devices [10, 11]. During the 1990s the emphasis was placed on utilising organic substrates and known PCB manufacturing processes like laser drilling, photolithography, etching techniques and chemical or electrochemical copper deposition [12–14]. The current trend is to implement embedding techniques also in System-In-Package modules (see Fig. 2.15) utilising novel 3D packages with z -axis connections. This enables the usage of the package top surface for package stacking

Embedding can include active integrated circuits or passive components such as resistors, capacitors or integrated passive devices. Typically, a terminal metal-lurgy—for example 5 μm copper—is required on embedded component pads. Figure 2.16 shows an example of a typical process flow and die level interconnection made with the IMB[®] technique.

The utilisation of component embedding techniques, especially at the component level, can offer a highly accurate and cost effective way of making interconnections. These benefits can be achieved with a wide variety of embedded components by utilising panel-sized volume production. Since the interconnections can be considered as pure Cu–Cu the long-term reliability is inherently

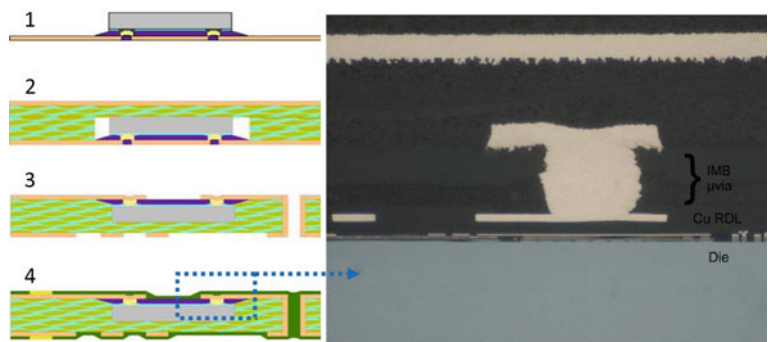


Fig. 2.16 Left_IMB[®] 3.0 generation process flow Right_Die copper terminal (bump/RDL) is connected to PCB copper layer with IMB microvia (Courtesy of Imbera Electronics)

Table 2.4 Commonly used solders, PCB and component metallisations [15, 16]

Solder (wt%)	PWB metallisation	Component metallisation
Sn–Pb	HASL (SnPb, SnCu)	Aluminium
Sn–Bi	Cu OSP	Bright tin
Sn–Sb	Electroless Ni Immersion gold	Chromium
Sn–Ag	Electrolytic Ni Electroplated Au	Gold
Sn–In	ENEPIG	Indium
Sn–Zn	Cu Immersion Sn	Matte Sn
Sn–Aez	Cu Immersion Ag	Ni Au
Sn–Cu–Ni		Ni Pd Au
Sn–Ag–Bi		Cu OSP
Sn–Ag–In		Palladium
Sn–Ag–Zn		Pt Pd Ag
Sn–Ag–Cu–Ni		Silver
Sn–Ag–Cu–Sb		Ag Pd
Sn–Ag–Bi–Cu–Ge		Tin and Sn based alloys
Sn–Ag–Cu–RE		Zink

excellent. The challenges with embedding techniques are related to requirements of high level material and process quality control required to achieve a high yield. Moreover, since no rework is possible with embedded components, KGD is required to achieve cost efficiency.

2.1.3 Board Level

The interconnections at the board level are typically made by soldering. During the last decade the soldering has changed markedly due to both environmental as well as manufacturability reasons. For more than five decades the components were

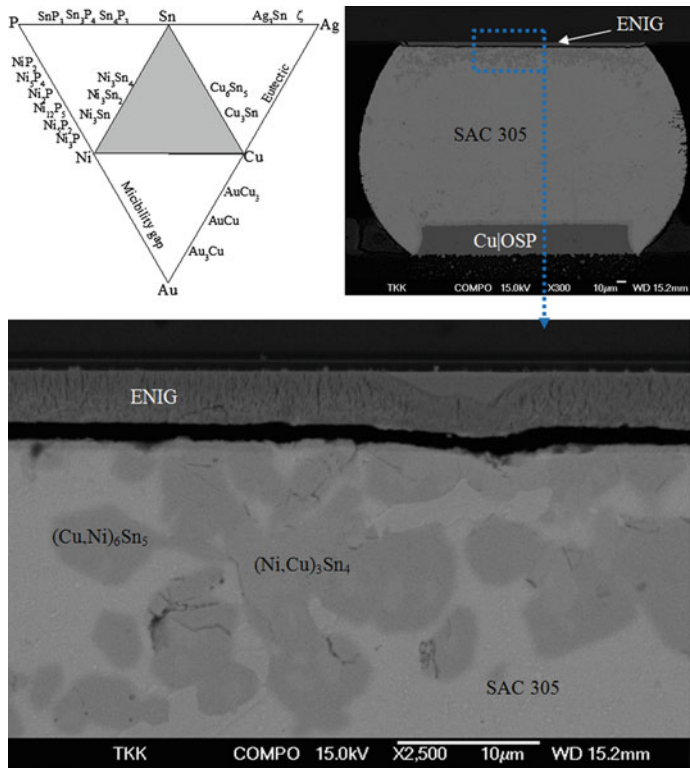


Fig. 2.17 a Schematic representation of a six component thermodynamic description including the binary IMCs, b SEM micrograph from SAC305 solder interconnection and c solder microstructure from SAC305 | ENIG interface

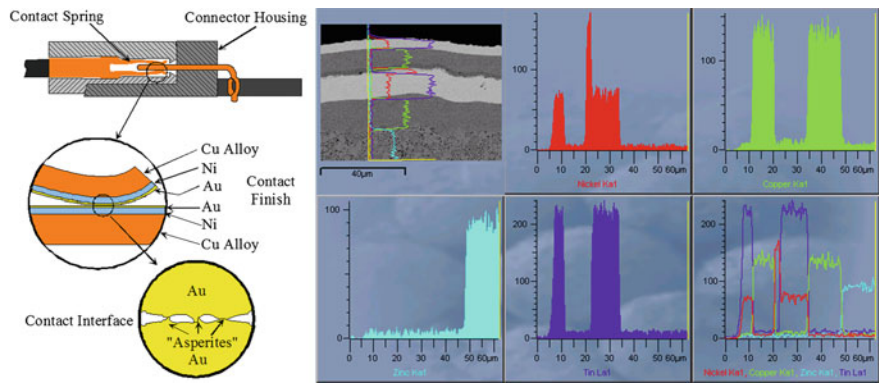


Fig. 2.18 Left_ Schematic illustration of a connector cross section (redrawn from 17). Right_ Example of contact finish layers from a DIN connector

attached to boards with SnPb solder, but the prohibition of lead changed the situation drastically. Even though, the soldering is still grounding on the chemical interaction between tin and typically copper or nickel contact metalisation, the implementation of lead-free solders and many different types of PCB or component metallisations has made the metallurgical system very complex. Table 2.4 shows commonly used solders, PCB and component metallisations.

Since the amount of different combinations is still increasing inevitably as, for example, new alloying elements to SAC solders are implemented, the manufacturability and reliability analyses purely by means of trial and error becomes impractical. For example, if one wishes to analyse the microstructural evolution of solder interconnections (see Fig. 2.17) at a constant temperature, where the contact metalisation is electroless nickel and immersion gold (ENIG) on the component side, CuOSP on board side and the solder is SAC305 (Sn 3.0Ag 0.5 Cu), a six component thermodynamic description (over 20 phases, even excluding ternary and higher order phases) is required.

The connections between circuit boards or products are characterised by utilisation of cables and connectors. The functionality and reliability of electromechanical connections has been the key enabling factor in system-level performance for decades. However, currently—especially in high-speed connections—optical signal transmission is utilised. Even though the solutions may be totally different between optical and electrical connections, the majority of the challenges are still related to (contact) interfaces (see Fig. 2.18) [17]. In electromechanical connectors the functionality and its stability over time is based on the interfacial phenomena at the contact surfaces. Typically, only a small fraction (even less than 1%) of the whole contact area is carrying the current through s.c. asperites or a-spots and, therefore, it is necessary to have a thorough understanding of the effects of parameters like, adsorption contamination, wear, fatigue, stress relaxation, etc.

There remain still very many challenges related to optical interconnects since the contamination of contact surfaces can cause severe power losses. Fluxless soldering is one of the possibilities in board-level interconnections, but a great many new innovations are still required before optical signal transmission can be adopted from system/product level down to component board or component level. The advanced SOP approaches may provide solutions in the future also for mass production. [2]

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2012, X, 218 p., Hardcover

ISBN: 978-1-4471-2469-6