

Preface

This book represents a contribution to the design of sigma-delta ($\Sigma\Delta$) modulators intended for the A/D conversion in multi-standard multi-mode wireless transceivers, implemented in nanometer CMOS technologies. In these transceivers, ADCs are key parts because they need to operate with a wide spread of their specifications; namely, effective resolution and signal bandwidth. $\Sigma\Delta$ modulators are very suited for the implementation of reconfigurable ADCs in highly integrated transceivers. On the one hand, the key principles of $\Sigma\Delta$ modulators (oversampling and noise shaping) determine the dynamic range of the ADC, so that their adjustment contributes to adapt the converter performance to different specifications with large hardware reuse. On the other, both principles make them robust with respect to non-idealities of an integrated implementation.

In spite of the advantages mentioned above, the design of nanometer CMOS $\Sigma\Delta$ ADCs is not easy, specially when considering adaptability and reconfigurability features. It involves a number of practical issues and trade-offs at both architectural and circuit level that must be taken into account for optimizing performance in terms of power dissipation (device portability and autonomy), silicon area (cost) and time-to-market deployment.

In this context, the work in this book presents innovative solutions for the implementation of flexible $\Sigma\Delta$ modulators intended for the next generation of wireless hand-held mobile terminals, implemented as a SoC in nanometer CMOS processes. Novel adaptive and reconfigurable $\Sigma\Delta$ modulator topologies—based on the combination of resonance, unity signal transfer function, and a new type of cascade with extra inter-stage feedback loops and simplified digital cancellation logic—are presented. These strategies allow to reduce the requirements of the embedded amplifiers in terms of finite DC gain, non-linearity and output swing. This makes them very suited for the implementation of low-voltage low-power wideband ADCs. At the circuit level, different strategies are applied to adapt the performance of the $\Sigma\Delta$ modulators to the different sets of specifications with adaptable power consumption.

A number of architectures, circuit techniques and design procedures presented in this book are demonstrated through the design, implementation and experimental characterization of three IC prototypes. The first one—implemented in a 130-nm CMOS technology—consists of an expandable cascade topology that comprises

a 2nd-order front-end stage followed by 1st-order stages, with the last one being switchable and also incorporating multi-bit quantization. The chip reconfigures the modulator loop filter order, the sampling frequency and the number of bits of the internal (back-end) quantizer, and scales the power consumption of internal building blocks in order to adapt the performance to the specifications of 2G/3G standards, considering a direct conversion receiver. Measurement results show a correct operation for GSM/Bluetooth/WCDMA standards, featuring a dynamic range of 86.7/81.0/63.3 dB for signal bandwidths of 200 kHz/1 MHz/4 MHz, respectively. The power consumption is 25.2/25.0/44.5 mW, of which 11.0/10.5/24.8 mW corresponds to the analog part of the circuit.

The second chip—implemented in a 90-nm CMOS process—consists of a two-stage (2–2) topology with 3-level quantization and unity signal transfer function in both stages. The chip reconfigures its loop filter, clock frequency and scales power according to the required specifications for different standards included in B3G wireless telecom, covering: GSM, Bluetooth, GPS, UMTS, DVB-H and WiMAX. Measurement results feature a dynamic range of 78/70/71.5/66/62/52 dB within bandwidths of 100 kHz/500 kHz/1 MHz/2 MHz/4 MHz/10 MHz, while consuming 4.6/5.35/6.2/8/8/11 mW, respectively.

The third chip is a 2-2-2 cascade made up of unity-STF stages. Similarly to the second chip, a 1.2-V 90-nm CMOS technology is employed. The chip can reconfigure its loop filtering order from 6 to 4 or 2 by switching off one or two stages in the cascade, respectively. The quantization in each stage can be selected to 3 or 5 levels. Every stage can work concurrently or as part of a cascade, so this $\Sigma\Delta$ modulator can process up to three standards in parallel. The employed architecture incorporates programmable resonance in the last two stages. The bias currents of main modulator building blocks are adjustable on-chip. Also, the sampling frequency can be adapted to the requirements of each operation mode. Experimental characterization of this chip indicates a correct operation for most of the reconfiguration techniques implemented; namely, adaptation of the in-loop filtering order, programmability of the bias currents in the modulator building blocks, variation of the internal quantization and concurrency.

The work in this book demonstrates the feasibility of using $\Sigma\Delta$ modulators for the efficient implementation of multi-standard telecom systems and shows the way for the practical deployment of the software defined radio paradigm.

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