

## Chapter 2

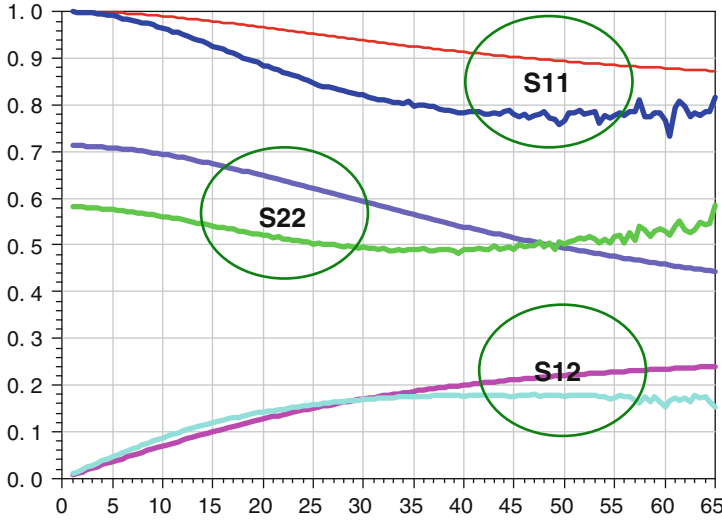
# mm-Wave Device Modeling

Circuit designers are mostly used to assume device models as given, instantiate their desired devices in their schematic windows, set up the simulation and run! They might perform their simulations in a number of different process corners and this is as much as they should worry about the whole notion of device modeling. mm-wave circuit design, at least for now, is an exception and both active and passive devices need extensive modeling. In this section, first reasons for this importance are discussed, then the device modeling procedure up to 100 GHz is presented and modeling results for single-transistor devices are shown. This follows by a discussion about measurement and de-embedding at these frequencies. Finally modeling of cascode devices are included as an example of a multi-transistor structure.

### 2.1 The Importance of Modeling in mm-Wave

Available models that circuit designers use in their daily simulations are the so-called “compact” models. Compact models are the interface between the technology and the design. A circuit designer learns about a process by experimenting with the compact model, rather than running expensive and time-consuming experiments.

Several good compact models have been developed for digital, analog, and RF applications [1,6,18,20]. These models use a combination of physical and empirical methods to develop general equations, usually a large number of them, to describe the behavior of the device. Several parameters are embedded in each equation in order to capture the details of a given technology. These parameters are necessarily determined through complicated curve fitting procedures (parameter extraction) and shape the familiar model card for circuit designers. Most compact models have the advantage of describing the behavior of the device in all regions of operation at the same time. Furthermore, they provide small and large signal analysis as well as noise analysis. They also operate over a fair range of geometry, width and length of the device, over which the extracted parameters are valid. This generality

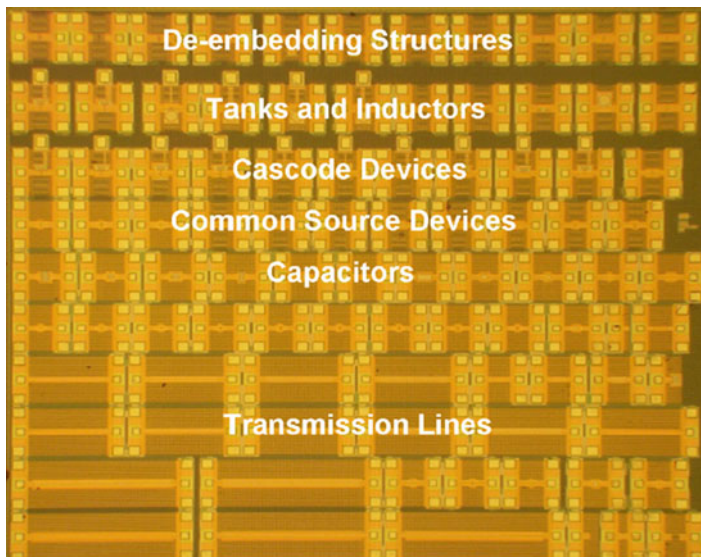


**Fig. 2.1**  $S$  parameters of an  $80\mu\text{m}$  common-source device, measurement versus model using available BSIM3v3 foundry model

however comes with an accuracy penalty if the model is used over a bias or geometry range outside of the extraction process. Moreover, the core equations in most compact models have been derived under quasi-static assumptions. This, together with the fact that most of available extracted parameters are also for low frequency applications, make these compact models less desirable and inaccurate for millimeter wave applications. Figure 2.1 shows the foundry modeled  $S$  parameters of a common-source device and compares it with the actual measurement of the device.

There are two main reasons for this inaccuracy: First of all, as mentioned before, the fact that the parameter extraction has been done in lower frequencies makes the extrapolation to mm-wave frequencies problematic [2]. Some of device mechanisms that are not well captured at low frequencies, and naturally not modeled properly, have considerable effect on the performance of the device in higher frequencies, resulting in some inaccuracy. The substrate network including capacitances and resistances is an example of such an effect [13]. The inaccuracy due to this effect could be addressed by increasing the frequency range of parameter extraction process.

The second reason for the error in modeling – which is more difficult to address – is due to the layout effect [5, 11]. The device interconnections to the outside world introduce small inductors, resistors and capacitors to the model. These small components are generally negligible at lower frequencies making the device model more or less independent of layout. These components however change and in fact dominate the performance of the device as the frequency increases and therefore should be included in the model. An accurate prediction of these parasitic requires



**Fig. 2.2** A sample 90 nm test chip fabricated for modeling and characterizing

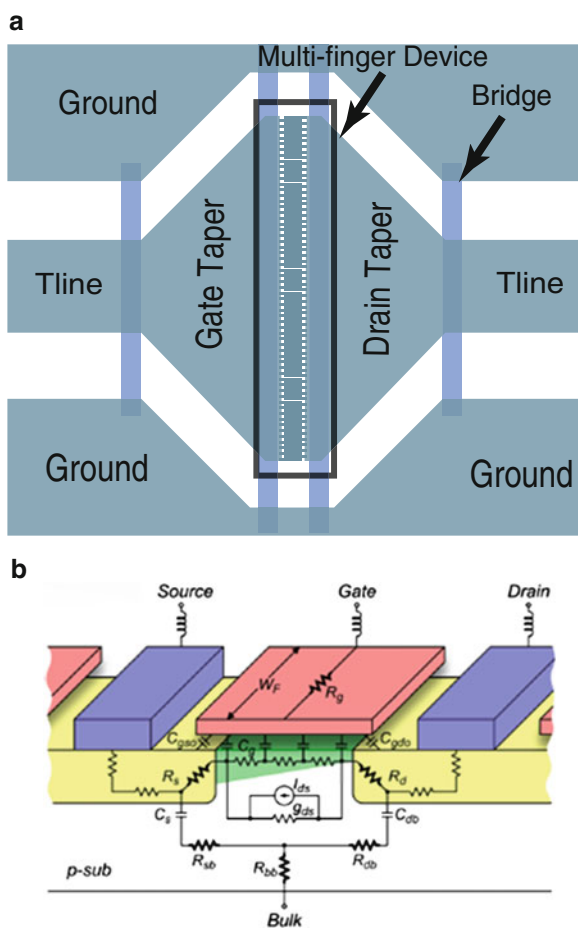
a detailed full-wave electromagnetic simulation, which is difficult and lengthy. Therefore existing compact models are used as the core for a hybrid customized mm-wave model. In essence, each small finger of the transistor is modeled with the “intrinsic” transistor model and interconnects are captured by a combination of selective electromagnetic simulation and experimental techniques. Due to the importance of device modeling in this project, two round of test structures were fabricated and modeled. The micrograph of one of these chips is shown in Fig. 2.2. The test chip contains common-source, common-gate and cascode transistors with various sizes as well as different transmission lines and capacitors. The characterized devices were used in all circuits designed and fabricated in 90 nm process in Berkeley wireless research center.

Given the difficulties in modeling the device, one may be tempted to work directly with measured data. In traditional microwave design the common approach is to use measured S-parameter data for a specific device and treat the transistor as a black box [9, 19]. This approach is very accurate in nature and accounts for all parasitics and distributed effects associated with the device and the layout. While this method is sufficient for small-signal circuit design applications, the accuracy of the S-parameter data hinges on reliable measurements of the device and de-embedding structures. As a result, the accuracy of the method may deteriorate for very high frequencies, both due to limited accuracy of test equipment and due to de-embedding errors. Besides, since S-parameters are small-signal in nature, this method is not suitable for simulation of any non-linear circuit such as mixers or oscillators or the assessment of the dynamic range of amplifiers. Moreover, because the transistor is treated as a black-box, there is no physical insight for improving

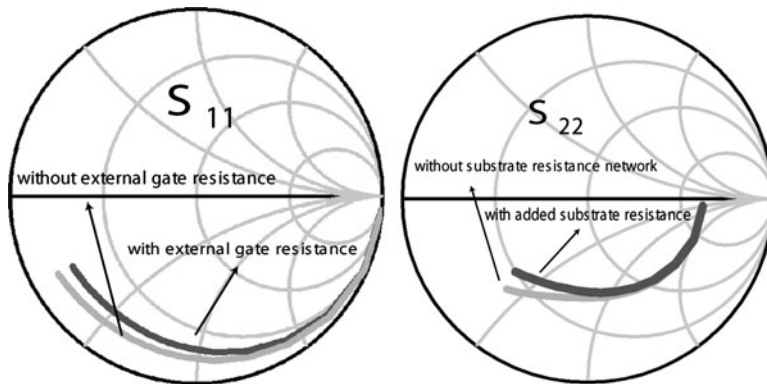
the device performance or layout. Due to these issues, for mm-wave application, a combination of “RF” and traditional microwave methodology is preferred even for small-signal applications.

## 2.2 High Frequency Modeling Procedure

A typical transistor layout designed for high frequency is shown in Fig. 2.3a. The device usually is long and narrow as it is designed with a large number of short fingers to minimize the gate resistance. A connection at the gate and the drain, usually in the form of a transmission line connects the device to the outside world. These transmission lines are connected through a  $45^\circ$  taper to the transistor for a



**Fig. 2.3** (a) Layout of a typical high frequency MOSFET. (b) A cross-section of a MOS transistor showing various parasitics



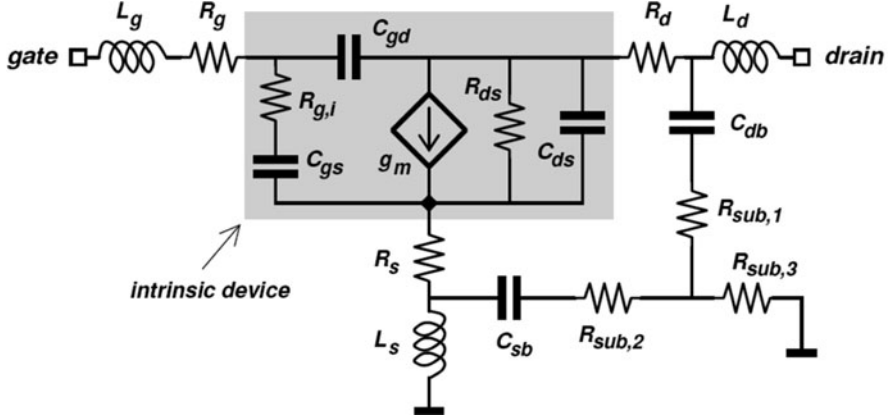
**Fig. 2.4** Model of a common-source NMOS (a)  $S_{11}$  with and without the gate resistance. (b)  $S_{22}$  with and without the substrate resistance network

proper current distribution to and from the device. The cross-section of a device is also shown in Fig. 2.3b to show several parasitics that should be considered in the high frequency modeling of the transistor.

At mm-wave frequencies, series resistive and inductive parasitics become more significant. While the resistive parasitics are always a part of the device, the inductive portion is usually more significant in high-frequency transistors because of the special layout considerations as mentioned earlier. Consequently, it is critical to properly model these parasitics, in addition to the capacitive effects that are traditionally captured by digital CMOS models. Moreover, neglecting or oversimplifying the substrate network of the device can introduce a considerable error at these frequencies. Figure 2.4 shows the error in the  $S_{11}$  and  $S_{22}$  of the device caused by ignoring the gate resistance and the substrate network in the small signal model of a typical NMOS transistor.

Equivalent circuits have been an effective approach to analyze the electrical behavior of a device by representing the important components [4, 17]. As shown in Fig. 2.5a MOSFET device can be divided into two portions: intrinsic part and extrinsic part. The intrinsic part (the shaded area in Fig. 2.5) is the familiar hybrid- $\pi$  model of the device, used for low frequency circuit analysis. The extrinsic part consists of parasitic resistances and inductances at the gate, drain and source as well as a proper substrate network. It is shown that a three resistor substrate network is sufficient to model the device behavior in the mm-wave frequencies [8]. Note that extrinsic parasitic capacitances between various terminals could be embedded in the internal device capacitances and be modeled as a part of the intrinsic part.

For each model, the extrinsic component values and device parameters were extracted from measured data using a hybrid optimization algorithm in Agilent IC-CAP [12]. Values of the components that could minimize the measurement to model error are not unique and one could come up with several equivalent circuits of the device for the same set of measurement data. This is acceptable as long as the model is used within the measured range of frequency. However, if the component



**Fig. 2.5** Small signal high frequency equivalent circuit of a MOS transistor

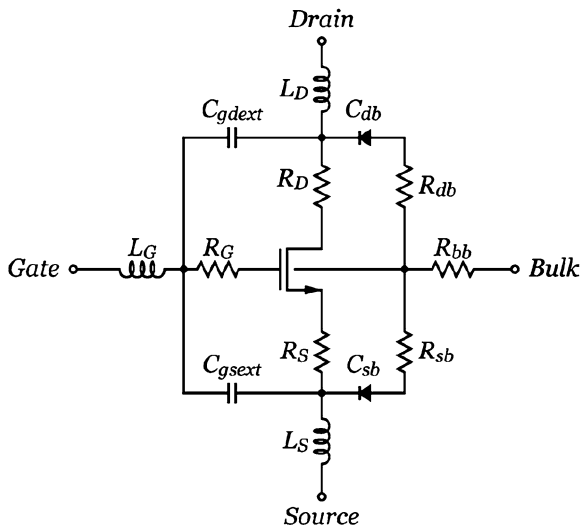
values in the model are made close to their physical values, there is an additional benefit and they can be used in frequencies well beyond the maximum measured frequency. Moreover, having a physical equivalent model can help with an accurate assessment of the value of parasitics and the sensitivity of the device performance to them. These information are very useful in optimization of the device physical structure as will be discussed in Chap. 3. Because of these reasons, the initial values of the components are calculated using proper equations and based on the measured  $Y$  parameters of the device up to 20 GHz [17]. The initial value of external resistances and inductances could also be estimated by simulating the connection leads and contacts on the terminals using EM simulators. These initial values then are fed to the optimizer with reasonable tuning ranges to get an accurate physical model.

### 2.2.1 Large Signal Modeling

Although small signal models are usually sufficient for the design of linear circuits, the design of high performance non-linear blocks such as mixers, oscillators and power amplifiers depends on capturing the nonlinear characteristics of the active devices over a wide range of voltage and current.

Developing a large-signal equivalent model from the scratch is a very complicated process and many physical effects that affect the DC behavior of the device need to be considered. Fortunately, available compact models, such as BSIM3v3 or BSIM4 are specifically created to capture most of these effects. By adding proper parasitics to these foundry given compact models as shown in Fig. 2.6, both DC nonlinearities and high frequency effects could be captured simultaneously. Since external terminal resistances and the substrate network are added manually, the BSIM model should be adjusted to turn-off the internal options for these parasitics. Moreover, due to the inherent accuracy compromise in these models to

**Fig. 2.6** Large signal high frequency equivalent circuit of a MOS transistor



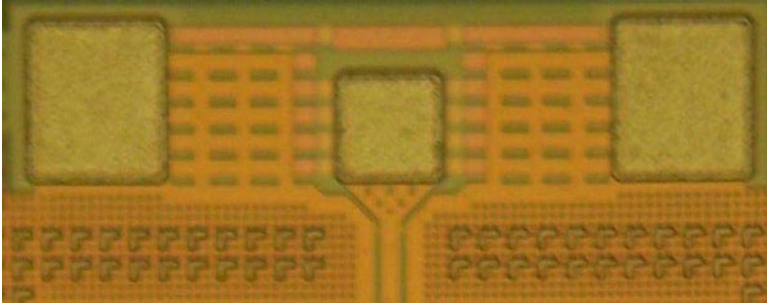
enable them to cover all geometries, the DC behavior of each individual device could be made more accurate and should be also fitted to the measurement by adjusting proper BSIM parameters [7].

## 2.3 Measurement and De-embedding

In the high frequency measurement of active and passive devices, the effect of probing pads and extra leads are typically subtracted from the measurement through a de-embedding method [23]. In direct de-embedding, the measured results from test structures (such as open and short circuits) are used directly and subtracted from the measurements. In a model based approach, a suitable physical equivalent circuit topology is selected and rough values for these equivalent circuit parameters then are estimated using a combination of equation-based calculations based on low frequency data. The final fine tuning and fitting is done using an optimizer such as Agilent IC-CAP [12]. In this section we review the major de-embedding procedures and discuss the problems and advantages of the various techniques.

### 2.3.1 RF Measurement Pads

Since most connections to the external world go through measurement pads, a good model for the pad is critical. In the model based de-embedding approach, this model



**Fig. 2.7** Layout of a common RF GSG pad

also serves as a foundation for de-embedding the effects of the pads whereas in the design of building blocks, the effects of the pads must be included in order to predict the real world performance of the device or circuit.

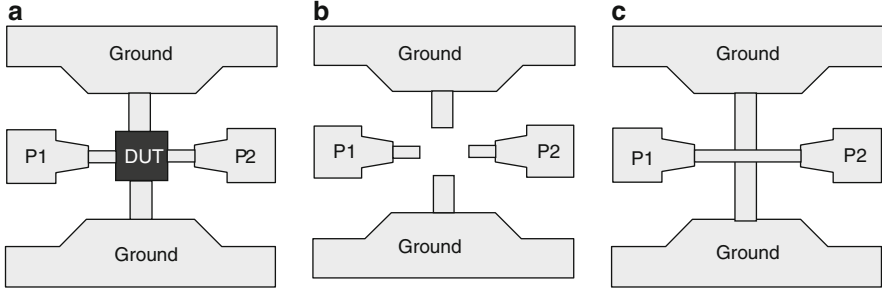
A common RF pad arrangement is the ground-signal-ground (GSG) structure shown in Fig. 2.7. These pads mate naturally with CPW probes and have good performance in the mm-wave band. Often the signal pad is shielded from the substrate, forming a grounded CPW (G-CPW) structure at the pad. If the transmission line leads to the rest of the circuit are microstrip or G-CPW, then this is the best option to use. Otherwise, if CPW is used, the decision to ground the pad is not clear cut. A shielded pad will form a high-Q structure, since the fields are isolated from the lossy substrate, but the shield adds extra capacitance and a discontinuity in the fields from the probe to the device. In order to reduce the pad capacitance, the signal pad is reduced to the minimum allowable probing dimensions, or about  $90\text{ }\mu\text{m} \times 90\text{ }\mu\text{m}$ , for  $150\text{ }\mu\text{m}$  pitch pads. For smaller pitch pads, smaller pads can be used. The RF pad is considerably smaller than the ground pads. A short  $45^\circ$  taper is used at the output of the pad in order to reduce the reflections due to discontinuities. In the example shown, a  $40\text{ }\mu\text{m}$ ,  $50\Omega$  transmission line connects the pad to the rest of the circuits.

### 2.3.2 Open-Short De-embedding

A popular de-embedding approach is the so-called open de-embedding, which simply removes the effects of the pads from the measurement structure shown in Fig. 2.8a by subtracting the measured  $Y$  parameters of the pad from the measured device, as shown in Fig. 2.8b. The key assumption is that the pads are connected in parallel to the DUT, which neglects the physical nature of the pads and treats the signal entry/exit points as lumped circuit nodes. The equivalent circuit for parasitics that could be captured in the open measurement is shown in Fig. 2.9. For the DUT we can write:

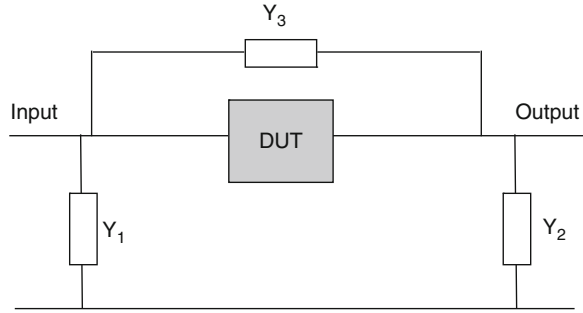
$$Y_{dut} = Y_m - Y_o \quad (2.1)$$





**Fig. 2.8** (a) The device under test and the measurement pads. (b) The open test structure. (c) The short test structure

**Fig. 2.9** The equivalent model of parasitics for the open de-embedding



And we can write these equations for the parasitics:

$$Y_3 = -Y_{12,o} = -Y_{21,o} \quad (2.2)$$

$$Y_1 = Y_{11,o} + Y_{12,o} \quad (2.3)$$

$$Y_2 = Y_{22,o} + Y_{21,o} \quad (2.4)$$

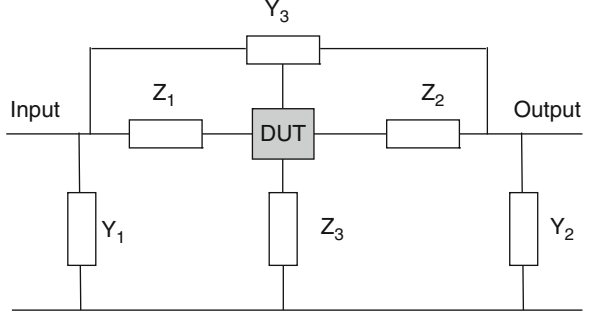
The other assumption for in the open de-embedding is that we can indeed measure a true pad *open* structure by simply open circuiting the pad test structure. In reality, the open circuits have finite fringe capacitance and radiation, which invalidates the above assumptions. In practice this procedure is quite accurate up to 10 GHz for small on-chip structures. In summary, open de-embedding removes the *shunt* parasitics from the measured device.

As the frequency increases, open de-embedding is not sufficient to de-embed all the parasitics and a more common approach is the so called open-short de-embedding. In this approach, in addition to measuring the embedded structure and open pads, a short structure as shown in Fig. 2.8c is also measured. A typical DUT with parasitics can be represented by an equivalent circuit shown in Fig. 2.10.

If we device the matrix  $Z'_s$  as

$$Z'_s = \begin{pmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{pmatrix} \quad (2.5)$$

**Fig. 2.10** The equivalent model of parasitics for the open-short de-embedding



Then we can calculate the  $Z'_s$  matrix from this equation:

$$Z'_s = (Y_s - Y_o)^{-1} \quad (2.6)$$

the same correction is applied to the measured data of interest

$$Y'_m = Y_m - Y_o \quad (2.7)$$

and then the modified short measurement is subtracted from the measurements

$$Z''_m = Y'^{-1}_m - Z'_s = (Y_m - Y_o)^{-1} - (Z_s^{-1} - Y_o)^{-1} \quad (2.8)$$

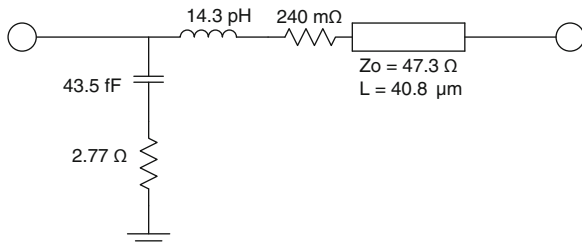
In practice this technique is reliable up to about 40 GHz or more, depending on the size of the test structures. By neglecting the distributed nature of the pads, we are limited to frequencies where all dimensions are negligibly small compared to the wavelength.

### 2.3.3 Recursive Modeling Process

Evidently, the de-embedding step is a major source of inaccuracy at mm-wave frequencies. It introduces error in the data due to imperfect assumption about the de-embedding structures. For example, for open-short de-embedding, the error arises from imperfect open and short especially at higher frequencies and the distributed nature of the structure. These inaccuracies make the de-embedded result noisy, directly affecting the accuracy of the extracted model. In order to resolve this problem several high frequency de-embedding methods have been proposed [14, 15, 22]. Here as an alternative a model based de-embedding approach, dubbed the *recursive modeling* has been employed.

A typical test structure comprises of probing pads, lead transmission lines and the device under test (DUT). In this method, probing pads are modeled in the first step. Pad models are then used to model the transmission line leads and finally the

**Fig. 2.11** Equivalent circuit of pad includes a section of transmission line



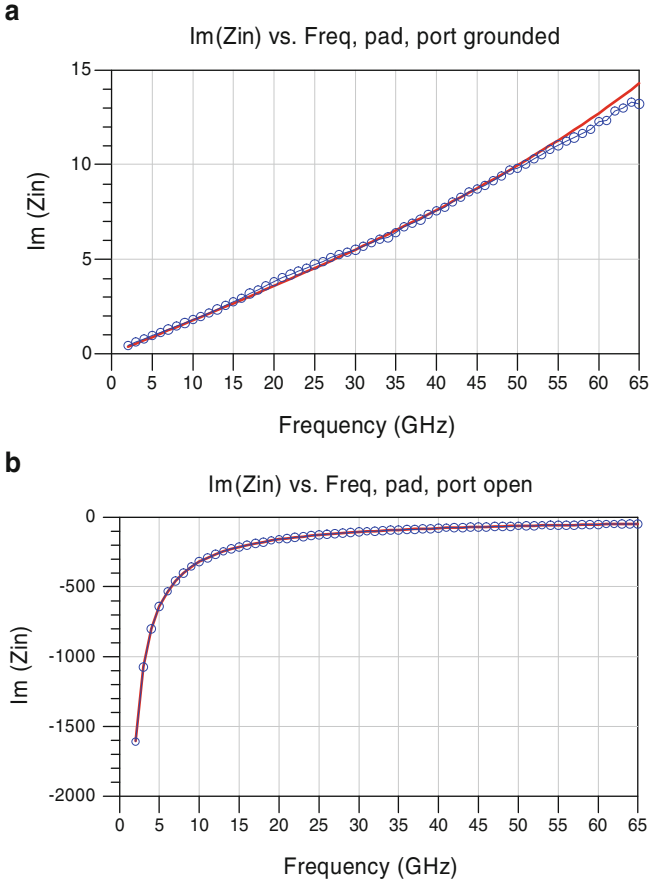
two models are employed to model the complete DUT. Typically all different test structures use identical probing pads and lead transmission lines making it sufficient to model them only once for all the structures. This modeling technique in principal is applicable for any structure, passive or active, as long as an equivalent circuit can capture the behavior of the structures.

The circuit shown in Fig. 2.11 is used to model the pad over a broad frequency range from 40 MHz to 65 GHz. The parallel branch represents the equivalent circuit for the pad itself and the series branch models the extra lead. The 1-port  $S$  parameters measurements are performed for the pad in two configurations, the first with the output port connected to ground, and the second with the output port left open. To increase the accuracy of the modeling, the  $Z$  and  $Y$  parameters of the model are simultaneously matched with the measured parameters in both configurations. The results in Fig. 2.12 show that the model accurately captures the RF pad behavior over the frequency range of interest.

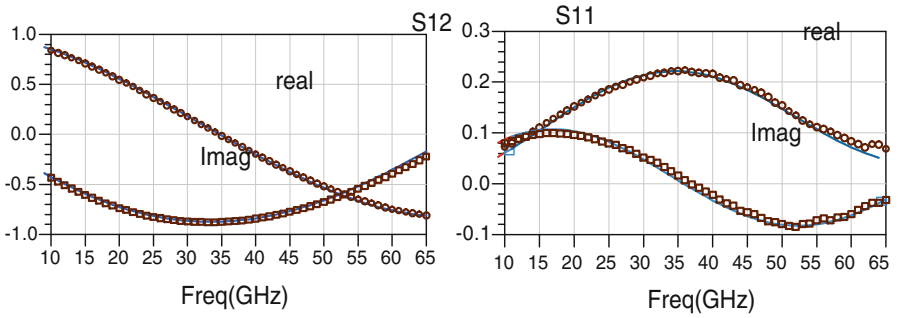
The transmission line that is used as a lead from the probe to the device has to be modeled in the next step. Coplanar waveguide (CPW) transmission lines are used in all test structures. A length scalable electrical transmission-line model has been developed to capture the complex propagation constant and frequency dependent characteristic impedance. Figure 2.13 shows the modeling result for a  $500\mu\text{m}$  CPW transmission line with a  $4\mu\text{m}$  signal-to-ground gap.

In the next step, the DUT is modeled. The complete model of the measured structure is made by connecting the previously modeled pad and transmission line whose models should be kept unchanged during this step and the equivalent model of the DUT that could be both small-signal or large-signal as was discussed in the previous section. The initial guesses of the equivalent circuit components are calculated and the whole model is then fitted to the raw device measurement through optimization of transistor core and external parameters.

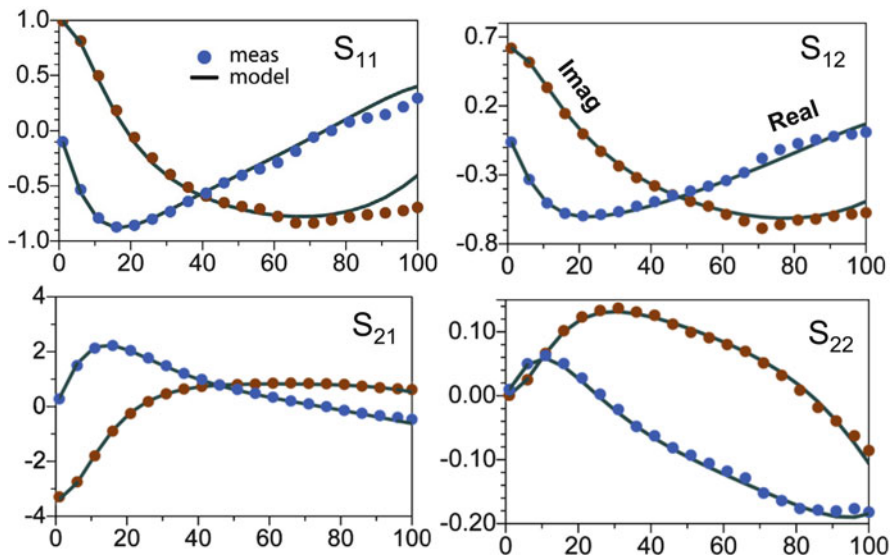
An experimental verification of this approach has been performed. All the measurements have been done using on-chip probing up to 110 GHz. Agilent IC-CAP software and the hybrid optimization method has been employed to perform model optimizations. Figure 2.14 shows the modeling result, the measured and modeled real and imaginary parts of  $S$ -parameters for an  $80\mu\text{m}/0.09\mu\text{m}$  transistor up to 100 GHz. The cleanness of the measured data is an advantage of this method which helps the accuracy and speed of the modeling process. The good agreement



**Fig. 2.12** Measured vs. simulated  $\Im(Z)$  parameters for the RF pad with the port (a) grounded and (b) open



**Fig. 2.13** Measured versus model of a  $500\mu\text{m}$  long CPW transmission line with gap spacing  $S = 4\mu\text{m}$



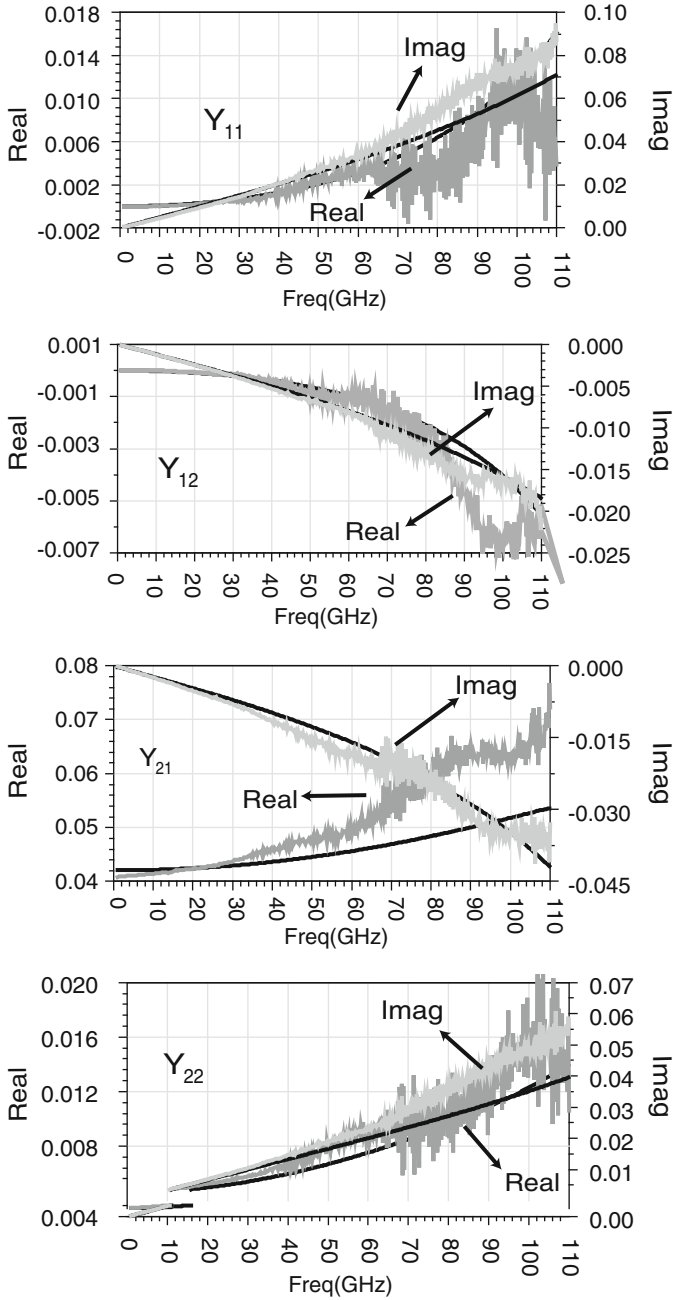
**Fig. 2.14** Measured (marker) versus simulated (lines)  $S$ -parameters of a 40μm/90nm transistor modeled using the recursive approach

between the model and measurement suggests that the extended lumped hybrid- $\pi$  model is valid to frequencies as high as 100 GHz.

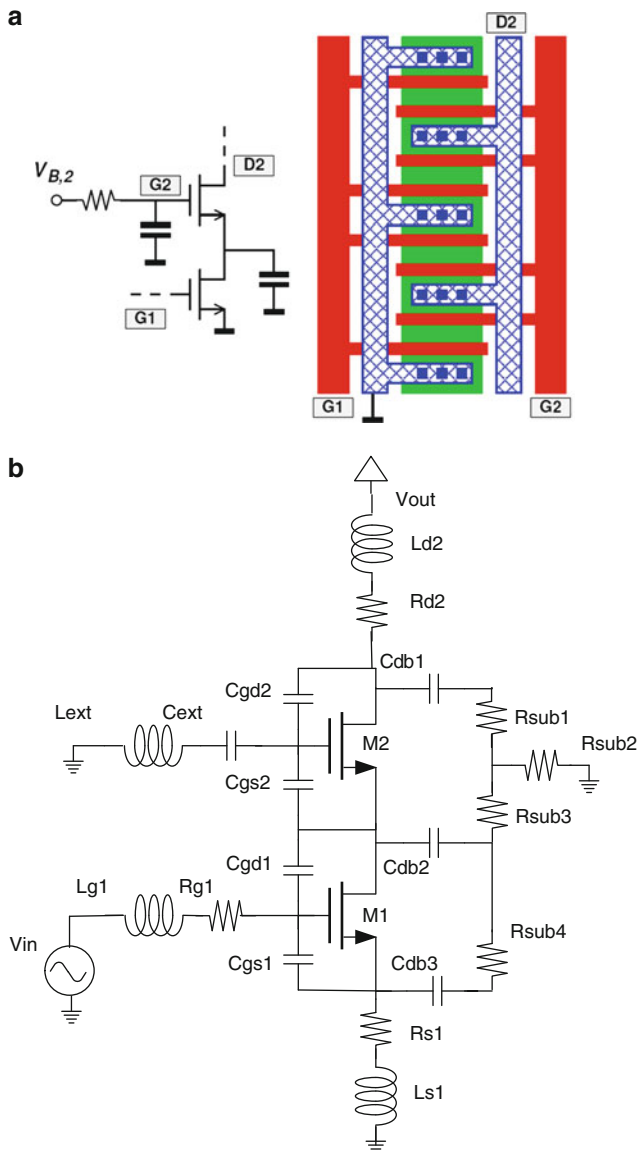
Figure 2.15 compares the result of the proposed modeling technique to the open-short de-embedding method. The difference can be best noticed by comparing  $Y$ -parameters. The de-embedded data is clearly noisy especially for frequencies in the millimeter-wave bands. For frequencies in the K and Ka bands, the two models give similar results. The discrepancy however gets significant for frequencies higher than 40 GHz showing the inaccuracy of open-short de-embedding for millimeter-wave applications. The error becomes specially significant in the imaginary parts of  $Y_{11}$  and  $Y_{22}$  and the real part of  $Y_{21}$ . These would result in major circuit performance degradations as we approach 100 GHz. The method was also tested with measured data up to 60 GHz and the predicted data at 100 GHz were compared to the actual measurement at this frequency and found to be in a good agreement. This indicates another important advantage of this modeling method that is its ability to extend beyond the measurement frequency without introducing significant error.

## 2.4 Cascode Modeling

Cascode devices are used extensively in mm-wave design. These devices could potentially provide higher gain compared to common-source devices and are usually unconditionally stable at these frequencies due to the isolation between



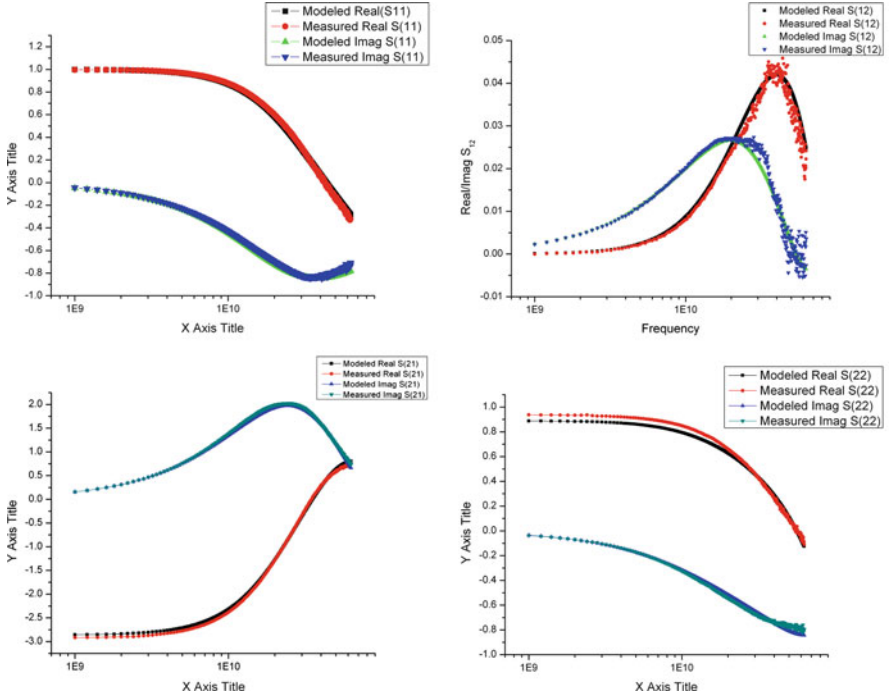
**Fig. 2.15** Comparison of the open/short versus recursive de-embedding/modeling approach for the  $Y$  parameters of a 40  $\mu\text{m}/90\text{nm}$



**Fig. 2.16** Equivalent circuit of a cascode device. The transistors can be replaced with a hybrid- $\pi$  model for small signal modeling

input and output [16]. To minimize the capacitance at the junction of the input and cascode device, a shared junction structure as shown in Fig. 2.16a is usually used.<sup>1</sup> Because of using this structure, cascode devices need special treatment in

<sup>1</sup>This is more explained in Chap. 5.



**Fig. 2.17** Comparison of measured and modeled device  $S$ -parameters

modeling and a simple connection of the two single transistor models does not accurately predict the device high frequency behavior and specifically can introduce substantial error in the  $Y_{22}$  of the device [3].

An equivalent circuit of a cascode transistor is shown in Fig. 2.16b. The model is essentially similar to the common-source model that was discussed earlier. One important difference is the way the substrate network is modeled. Because of the shared junction structure, the substrates of the two devices are shared and this needs to be considered in the equivalent circuit. This substrate can be a source of feedback between the output and input [10]. The second gate of the device is also connected to a bypass capacitor to ensure a high frequency ground to avoid oscillation. Because of the sensitivity of the cascode gate to parasitics, the proper equivalent model of the capacitor should be included on the cascode gate.

To test the accuracy of the model, a sample 40 $\mu\text{m}/90\text{nm}$  is measured and compared to the model using the proposed method. The close match between measured and modeled  $S$ -parameters up to 65 GHz as shown in Fig. 2.17 confirms the validity of the model as well as the modeling procedure.



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