

## Chapter 2

# Voltage and Current Multiplier Circuits

### 2.1 Mathematical Analysis for Synthesis of Multipliers

The synthesis of multiplier circuits [1–60] is based on the utilization of some elementary principles, each of them representing the starting point for designing a class of multiplier circuit.

Referring to the input variables, it can be identified two important classes of multiplier circuits:

- Voltage multipliers, having as input variables two single or differential voltages and generating an output current proportional with the product of these input voltages;
- Current multipliers, receiving as inputs two currents and producing an output current proportional with the product of the input currents.

Because the multiplying function uses the characteristic of MOS transistors biased in saturation region, most of mathematical principles are derived from a linear relation between squaring terms (having voltages or currents as variables). The notations used for revealing these principles are:  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$  represent the input potentials, while, usually, a constant voltage,  $V_O$ , is introduced for modeling a voltage shifting; for current multipliers,  $I_1$ ,  $I_2$  and  $I_3$  are the input currents and  $I_O$  represents a reference current. In both cases,  $I_{OUT}$  denotes the output current of the multiplier circuit.

### 2.1.1 Mathematical Analysis of Voltage Multiplier Circuits

#### 2.1.1.1 First Mathematical Principle (PR 2.1)

The first mathematical principle used for implementing voltage multiplier circuits is based on the following identity:

$$(V_1 + V_2 + V_O)^2 - (V_1 - V_2 + V_O)^2 + (-V_1 - V_2 + V_O)^2 - (-V_1 + V_2 + V_O)^2 = 2V_2(2V_1 + 2V_O) - 2V_2(-2V_1 + 2V_O) = 8V_1V_2 \quad (2.1)$$

The voltage multipliers based on the previous relation computes a current proportional with the product of two input voltages,  $V_1$  and  $V_2$ .

#### 2.1.1.2 Second Mathematical Principle (PR 2.2)

The mathematical relation that models this principle is

$$(V_1 + V_3 + V_O)^2 - (V_2 + V_3 + V_O)^2 + (V_2 + V_4 + V_O)^2 - (V_1 + V_4 + V_O)^2 = (V_1 - V_2)(V_1 + V_2 + 2V_3 + 2V_O) - (V_1 - V_2)(V_1 + V_2 + 2V_4 + 2V_O) = 2(V_1 - V_2)(V_3 - V_4) \quad (2.2)$$

The circuits that use this principle generates a current proportional with the product between two differential input voltages,  $V_1 - V_2$  and  $V_3 - V_4$ .

#### 2.1.1.3 Third Mathematical Principle (PR 2.3)

This principle is illustrated by the following mathematical relation:

$$(V_1 - V_3 + V_O)^2 - (V_1 - V_4 + V_O)^2 + (V_2 - V_4 + V_O)^2 - (V_2 - V_3 + V_O)^2 = (V_4 - V_3)(2V_1 - V_3 - V_4 + 2V_O) - (V_4 - V_3)(2V_2 - V_3 - V_4 + 2V_O) = 2(V_1 - V_2)(V_4 - V_3) \quad (2.3)$$

The multiplier circuits that implement this principle compute, also, an output current proportional with the product between two differential input voltages,  $V_1 - V_2$  and  $V_4 - V_3$ .

### 2.1.1.4 Fourth Mathematical Principle (PR 2.4)

The fourth mathematical principle is based on the following mathematical relation:

$$\begin{aligned} I_{OUT} &= a\sqrt{I_O}(V_1 - V_2) \\ I_O &= b(V_3 - V_4)^2 \end{aligned} \Rightarrow I_{OUT} = a\sqrt{b}(V_1 - V_2)(V_3 - V_4) \quad (2.4)$$

or

$$\begin{aligned} I_{OUT} &= a(\sqrt{I_1} - \sqrt{I_2})(V_1 - V_2) \\ (\sqrt{I_1} - \sqrt{I_2})^2 &= b(V_3 - V_4)^2 \end{aligned} \Rightarrow I_{OUT} = a\sqrt{b}(V_1 - V_2)(V_3 - V_4) \quad (2.5)$$

$a$  and  $b$  represent constant coefficients, depending on the particular implementation of the multiplier circuit based on this mathematical principle.

### 2.1.1.5 Fifth Mathematical Principle (PR 2.5)

The fifth mathematical principle represents the cancellation of a nonlinear dependence of an output current,  $I_{OUT}$ , on the input voltage,  $V_1$ :

$$I_{OUT} = KV_1 \sqrt{\frac{I_O + KV_1^2/4}{K} - \frac{V_1^2}{4}} = \sqrt{KI_O}V_1 \quad (2.6)$$

### 2.1.1.6 Sixth Mathematical Principle (PR 2.6)

The mathematical relation that models this principle is

$$\left(\frac{V_1 + V_2}{2} - V_O\right)^2 + V_O^2 - \left(\frac{V_1}{2} - V_O\right)^2 - \left(\frac{V_2}{2} - V_O\right)^2 = V_1V_2 \quad (2.7)$$

### 2.1.1.7 Seventh Mathematical Principle (PR 2.7)

The identity representing the basis of this mathematical relation is

$$(V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2 \quad (2.8)$$

### 2.1.1.8 Different Mathematical Principles for Voltage Multipliers (PR 2.Da)

A class of multipliers can be designed starting from different mathematical principles, that are useful for linearizing the behavior of the multiplier circuits.

## 2.1.2 Mathematical Analysis of Current Multiplier Circuits

### 2.1.2.1 Ninth Mathematical Principle (PR 2.9)

The ninth mathematical principle uses two square-rooting circuits in order to implement the multiplying function:

$$\begin{aligned} I_{O1} &= a\sqrt{I_O I_{OUT}} \\ I_{O2} &= a\sqrt{I_1 I_2} \quad \Rightarrow I_{OUT} = \frac{I_1 I_2}{I_O} \\ I_{O1} &= I_{O2} \end{aligned} \quad (2.9)$$

### 2.1.2.2 Tenth Mathematical Principle (PR 2.10)

The identity representing the basis of this mathematical relation is

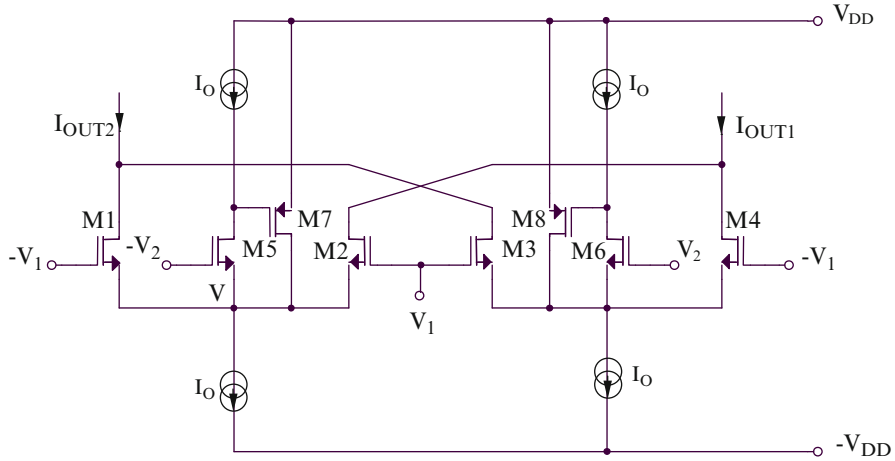
$$\left[ I_O + \frac{(I_1 + I_2)^2}{aI_O} \right] - \left[ I_O - \frac{(I_1 + I_2)^2}{aI_O} \right] = \frac{4I_1 I_2}{aI_O} \quad (2.10)$$

### 2.1.2.3 Eleventh Mathematical Principle (PR 2.11)

In order to implement the eleventh mathematical principle, the circuits use only MOS transistors biased in weak inversion region, the translinear loops that contain gate-source voltages generating the product between the input currents.

### 2.1.2.4 Different Mathematical Principles for Current Multipliers (PR 2.Db)

A class of multipliers can be designed starting from different mathematical principles that are useful for linearizing the behavior of the current multiplier circuits.



**Fig. 2.1** Multiplier circuit (1) based on PR 2.1

## 2.2 Analysis and Design of Multiplier Circuits

### 2.2.1 Design of Voltage Multiplier Circuits

Based on the previous presented mathematical analysis, the voltage multipliers can be clustered in eight important functional classes: circuits using PR 2.1–PR 2.7 elementary principle and a class containing multipliers based on different functional relations.

#### 2.2.1.1 Multiplier Circuits Based on the First Mathematical Principle (PR 2.1)

The multiplier structures using as functional basis PR 2.1 present the important advantage of using a symmetrical structure that minimizes the intrinsic linearity error of the designed circuits.

A circuit that implements the product between two input voltages using the PR 2.1 mathematical principle is presented in Fig. 2.1 [1].

The output current of the voltage multiplier can be expressed as a linear function of the currents,  $I_{OUT1}$  and  $I_{OUT2}$ :

$$I_{OUT} = I_{OUT1} - I_{OUT2} = (I_{D2} + I_{D4}) - (I_{D1} + I_{D3}) \quad (2.11)$$

The drain current of M1 transistor is

$$I_{D1} = \frac{K}{2} (-V_1 - V - V_T)^2 \quad (2.12)$$

The  $V$  potential is imposed by  $V_2$  potential and by the gate-source of M5 transistor (that is biased at a constant current,  $I_O$ ) to be equal with:

$$V = -V_2 - V_{GS5} = -V_2 - V_T - \sqrt{\frac{2I_O}{K}} \quad (2.13)$$

Replacing (2.13) in (2.12), it results the following dependence of  $I_{D1}$  current on  $V_1$ , and  $V_2$  input potentials:

$$I_{D1} = \frac{K}{2} \left( -V_1 + V_2 + \sqrt{\frac{2I_O}{K}} \right)^2 \quad (2.14)$$

Similarly, the drain currents of M2–M4 transistors can be expressed as

$$I_{D2} = \frac{K}{2} \left( V_1 + V_2 + \sqrt{\frac{2I_O}{K}} \right)^2 \quad (2.15)$$

$$I_{D3} = \frac{K}{2} \left( V_1 - V_2 + \sqrt{\frac{2I_O}{K}} \right)^2 \quad (2.16)$$

$$I_{D4} = \frac{K}{2} \left( -V_1 - V_2 + \sqrt{\frac{2I_O}{K}} \right)^2 \quad (2.17)$$

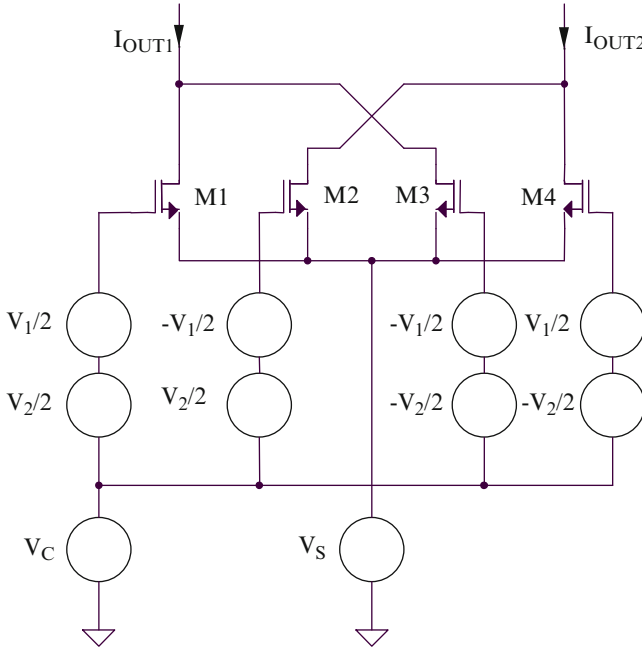
The expression of the output current as a function of input potentials can be obtained using relations (2.11) and (2.14)–(2.17):

$$I_{OUT} = \frac{K}{2} 2V_1 \left( 2V_2 + 2\sqrt{\frac{2I_O}{K}} \right) + \frac{K}{2} (-2V_1) \left( -2V_2 + 2\sqrt{\frac{2I_O}{K}} \right) = 4KV_1V_2 \quad (2.18)$$

Another multiplier structure based on the first mathematical principle (PR 2.1) is presented in Fig. 2.2 [2]. Its output current can be expressed as

$$I_{OUT} = (I_{D1} + I_{D3}) - (I_{D2} + I_{D4}) = (I_{D1} - I_{D2}) + (I_{D3} - I_{D4}) \quad (2.19)$$

For M1–M4 transistors, the gate potentials are imposed by the common-mode voltage  $V_C$  and by the differential components  $\pm V_1/2$  and  $\pm V_2/2$ .



**Fig. 2.2** Multiplier circuit (2) based on PR 2.1

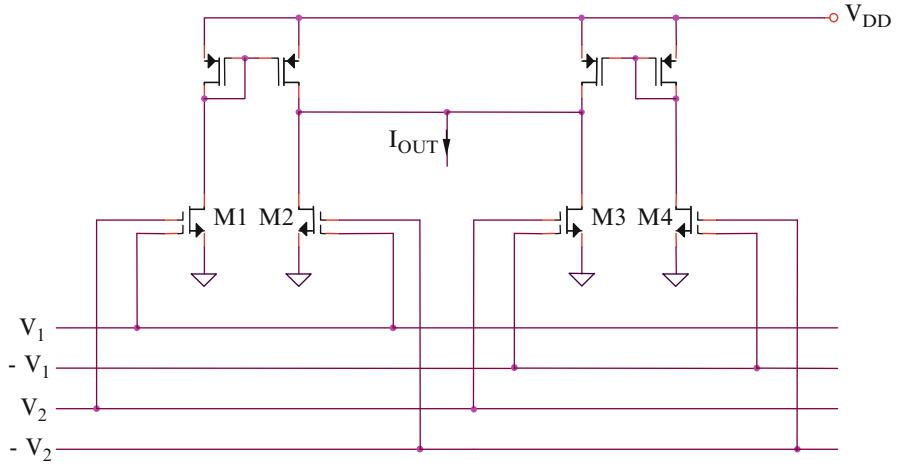
Replacing the expressions of the previous drain currents with their quadratic dependence on the gate-source voltages, it results:

$$\begin{aligned}
 I_{OUT} = I_{OUT1} - I_{OUT2} = & \frac{K}{2} \left( \frac{V_1 + V_2}{2} + V_C - V_S - V_T \right)^2 \\
 & + \frac{K}{2} \left( -\frac{V_1 + V_2}{2} + V_C - V_S - V_T \right)^2 - \frac{K}{2} \left( \frac{V_1 - V_2}{2} + V_C - V_S - V_T \right)^2 \\
 & - \frac{K}{2} \left( \frac{V_2 - V_1}{2} + V_C - V_S - V_T \right)^2 \quad (2.20)
 \end{aligned}$$

So, the output current will be proportional with the product between the differential-mode input voltages:

$$\begin{aligned}
 I_{OUT} = & \frac{K}{2} V_1 (V_2 + 2V_C - 2V_S - 2V_T) \\
 & + \frac{K}{2} (-V_1) (-V_2 + 2V_C - 2V_S - 2V_T) = KV_1 V_2 \quad (2.21)
 \end{aligned}$$

An alternate realization of a voltage multiplier circuit based on the first mathematical principle (PR 2.1) is presented in Fig. 2.3. In order to reduce the



**Fig. 2.3** Multiplier circuit (3) based on PR 2.1

circuit complexity, a part of classical MOS transistors have been replaced by FGMOS active devices with identical inputs.

The output current can be expressed as follows:

$$\begin{aligned}
 I_{OUT} &= (I_{D1} - I_{D2}) + (I_{D4} - I_{D3}) = \frac{K}{2} \left( \frac{V_1 + V_2}{2} - V_T \right)^2 \\
 &\quad - \frac{K}{2} \left( \frac{V_1 - V_2}{2} - V_T \right)^2 + \frac{K}{2} \left( -\frac{V_1 + V_2}{2} - V_T \right)^2 \\
 &\quad - \frac{K}{2} \left( \frac{V_2 - V_1}{2} - V_T \right)^2 = \frac{K}{2} V_2 (V_1 - 2V_T) \frac{K}{2} V_2 (-V_1 - 2V_T) = KV_1 V_2 \quad (2.22)
 \end{aligned}$$

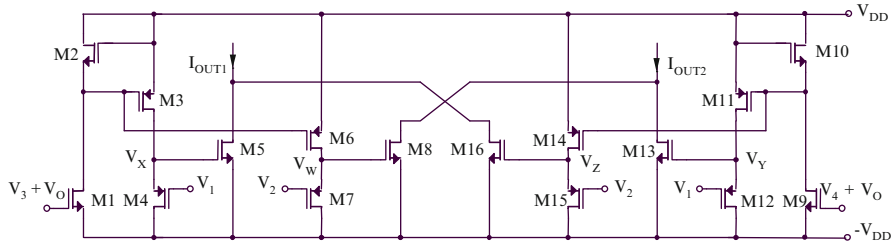
### 2.2.1.2 Multiplier Circuits Based on the Second Mathematical Principle (PR 2.2)

The multipliers based on PR 2.2 can be used in a large area of applications that require the implementation of the product between two differential voltages.

A voltage multiplier having as functional relation the second mathematical principle (PR 2.2) is presented in Fig. 2.4 [3].

All MOS transistors are biased in saturation region and  $V_O$  represents a constant voltage that is summed with  $V_3$  and  $V_4$  voltages. The expression of differential output current is

$$I_{OUT1} - I_{OUT2} = (I_{D5} + I_{D16}) - (I_{D8} + I_{D13}) \quad (2.23)$$



**Fig. 2.4** Multiplier circuit (1) based on PR 2.2

$$I_{D5} = \frac{K}{2}(V_X + V_{DD} - V_T)^2 \quad (2.24)$$

$$I_{D16} = \frac{K}{2}(V_Z + V_{DD} - V_T)^2 \quad (2.25)$$

$$I_{D8} = \frac{K}{2}(V_W + V_{DD} - V_T)^2 \quad (2.26)$$

$$I_{D13} = \frac{K}{2}(V_Y + V_{DD} - V_T)^2 \quad (2.27)$$

As a consequence of the circuit configuration, the gate-source voltages of M2 and M3 transistors are equal, resulting  $I_{D2} = I_{D3}$ . But  $I_{D3} = I_{D4}$  and  $I_{D1} = I_{D2}$ , so  $I_{D1} = I_{D4}$ . In conclusion, because M1 and M4 transistors are identical, it results  $V_{GS1} = V_{GS4}$ , equivalent with:

$$V_3 + V_O + V_{DD} = V_X - V_1 \quad (2.28)$$

Thus, the expression of  $V_X$  potential will be

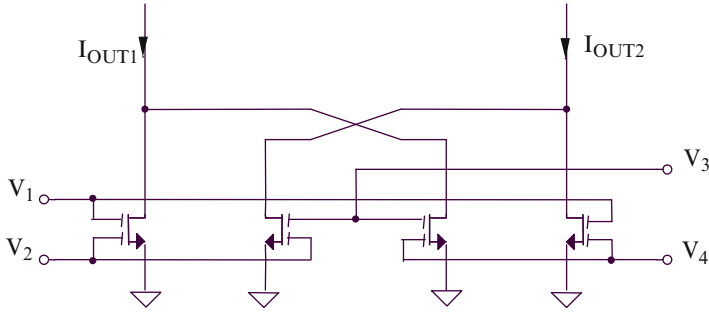
$$V_X = V_1 + V_3 + V_O + V_{DD} \quad (2.29)$$

Replacing (2.29) in (2.24), the drain current of M5 transistor will have the following expression:

$$I_{D5} = \frac{K}{2} [(V_1 + V_3) + (2V_{DD} + V_O - V_T)]^2 \quad (2.30)$$

Similarly, the expression of drain currents of M8, M13 and M16 transistor will be

$$I_{D8} = \frac{K}{2} [(V_2 + V_3) + (2V_{DD} + V_O - V_T)]^2 \quad (2.31)$$



**Fig. 2.5** Multiplier circuit (2) based on PR 2.2

$$I_{D13} = \frac{K}{2} [(V_1 + V_4) + (2V_{DD} + V_O - V_T)]^2 \quad (2.32)$$

$$I_{D16} = \frac{K}{2} [(V_2 + V_4) + (2V_{DD} + V_O - V_T)]^2 \quad (2.33)$$

Replacing (2.30)–(2.33) in (2.23), it results:

$$\begin{aligned} I_{OUT1} - I_{OUT2} &= \frac{K}{2} (V_1 - V_2)(V_1 + V_2 + 2V_3 + 4V_{DD} + 2V_O - 2V_T) \\ &\quad - \frac{K}{2} (V_1 - V_2)(V_1 + V_2 + 2V_4 + 4V_{DD} + 2V_O - 2V_T) \end{aligned} \quad (2.34)$$

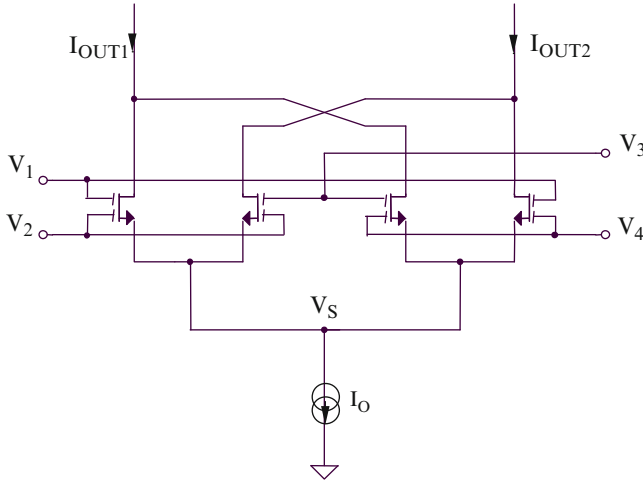
So

$$I_{OUT1} - I_{OUT2} = K(V_1 - V_2)(V_3 - V_4) \quad (2.35)$$

A possible implementation of a voltage multiplier based on the second mathematical principle (PR 2.2), using FGMOS transistors is presented in Fig. 2.5 [4].

Considering identical inputs for all FGMOS transistors, the differential output current of the voltage multiplier presented in Fig. 2.5 can be expressed as follows:

$$\begin{aligned} I_{OUT} = I_{OUT1} - I_{OUT2} &= \frac{K}{2} \left( \frac{V_1 + V_2}{2} - V_T \right)^2 + \frac{K}{2} \left( \frac{V_3 + V_4}{2} - V_T \right)^2 \\ &\quad - \frac{K}{2} \left( \frac{V_2 + V_3}{2} - V_T \right)^2 - \frac{K}{2} \left( \frac{V_1 + V_4}{2} - V_T \right)^2 = \frac{K}{4} (V_1 - V_3)(V_2 - V_4) \end{aligned} \quad (2.36)$$



**Fig. 2.6** Multiplier circuit (3) based on PR 2.2

An alternate implementation of a voltage multiplier using the second mathematical principle is presented in Fig. 2.6 [4].

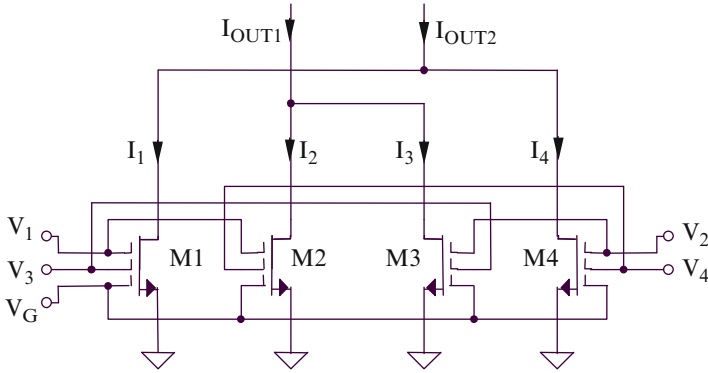
The differential output current of the voltage multiplier shown in Fig. 2.6 will have the following expression:

$$\begin{aligned}
 I_{OUT} = I_{OUT1} - I_{OUT2} &= \frac{K}{2} \left( \frac{V_1 + V_2}{2} - V_S - V_T \right)^2 \\
 &+ \frac{K}{2} \left( \frac{V_3 + V_4}{2} - V_S - V_T \right)^2 - \frac{K}{2} \left( \frac{V_2 + V_3}{2} - V_S - V_T \right)^2 \\
 &- \frac{K}{2} \left( \frac{V_1 + V_4}{2} - V_S - V_T \right)^2 = \frac{K}{4} (V_1 - V_3) (V_2 - V_4) \quad (2.37)
 \end{aligned}$$

The multiplier circuit presented in Fig. 2.7 [5] is based on the second mathematical principle (PR 2.2).

The output current of the voltage multiplier is implemented (using an additional current mirror, not shown in Fig. 2.7) to be the difference between  $I_{OUT2}$  and  $I_{OUT1}$  currents and it can be expressed as follows:

$$\begin{aligned}
 I_{OUT} = I_{OUT2} - I_{OUT1} &= (I_1 + I_4) - (I_2 + I_3) \\
 &= \frac{K}{2} \left( \frac{V_1 + V_3 + V_G}{3} - V_T \right)^2 + \frac{K}{2} \left( \frac{V_2 + V_4 + V_G}{3} - V_T \right)^2 \\
 &- \frac{K}{2} \left( \frac{V_1 + V_4 + V_G}{3} - V_T \right)^2 - \frac{K}{2} \left( \frac{V_2 + V_3 + V_G}{3} - V_T \right)^2 \quad (2.38)
 \end{aligned}$$



**Fig. 2.7** Multiplier circuit (4) based on PR 2.2

resulting:

$$I_{OUT} = \frac{K}{2} \frac{V_3 - V_4}{3} \left( \frac{2V_1 + V_3 + V_4 + 2V_G}{3} - 2V_T \right) - \frac{K}{2} \frac{V_3 - V_4}{3} \left( \frac{2V_2 + V_3 + V_4 + 2V_G}{3} - 2V_T \right) \quad (2.39)$$

So, the output current is proportional with the product between the differential input voltages:

$$I_{OUT} = \frac{K}{9} (V_3 - V_4) (V_1 - V_2) \quad (2.40)$$

### 2.2.1.3 Multiplier Circuits Based on the Third Mathematical Principle (PR 2.3)

Alternative implementations of multiplier circuits designed for differential input voltages uses the mathematical relations described by PR 2.3.

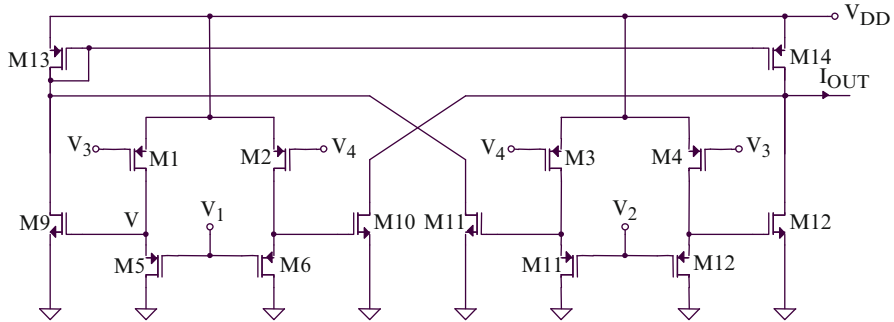
A combination of two differential amplifiers, M1–M2 and M3–M4, can implement the multiplying function (Fig. 2.8), the functional equations of this circuit being obtained using the third mathematical principle (PR 2.3) [6].

The gate-source voltages of M1 and M5 transistors are equal because they are identical and biased at the same drain current, resulting:

$$V_{DD} - V_3 = V - V_1 \quad (2.41)$$

equivalent with:

$$V = V_1 - V_3 + V_{DD} \quad (2.42)$$



The drain current of M9 transistor can be expressed as follows:

Similarly, the expressions of drain currents for M10, M11 and M12 transistors are:

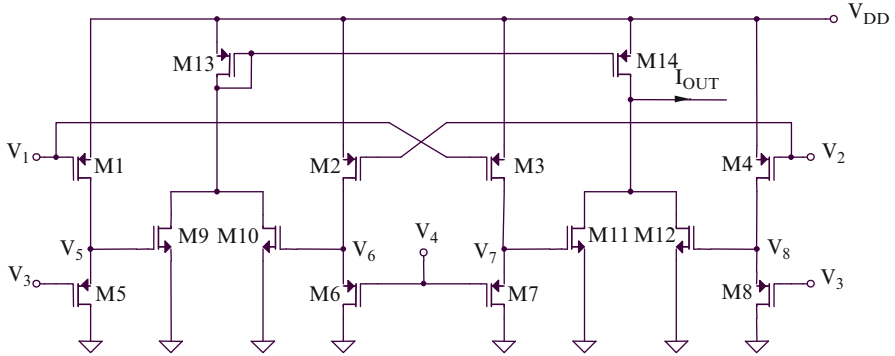
$$I_{D11} = \frac{K}{2} [(V_2 - V_4) + (V_{DD} - V_T)]^2 \quad (2.45)$$

The output current  $I_{OUT}$  of the multiplier will be expressed by

resulting:

or

$$I_{OUT} = K(V_2 - V_1)(V_3 - V_4) \quad (2.49)$$



**Fig. 2.9** Multiplier circuit (2) based on PR 2.3

The voltage multiplying function can be implemented using the third mathematical principle (PR 2.3) by the structure presented in Fig. 2.9 [7].

The circuit contains four pairs of transistors (M1–M5, M2–M6, M3–M7 and M4–M8) that implement voltage subtraction functions. Because M1 and M5 transistors are identical and biased at the same drain current, their gate-source voltages will be equal, so that:

$$V_{DD} - V_1 = V_5 - V_3 \quad (2.50)$$

resulting that  $V_5$  potential is given by the differential input voltage,  $V_3 - V_1$ :

$$V_5 = V_{DD} + (V_3 - V_1) \quad (2.51)$$

The  $V_5$  potential is applied on the gate of M9 transistor, its drain current being expressed using the squaring characteristic of the MOS transistor biased in saturation:

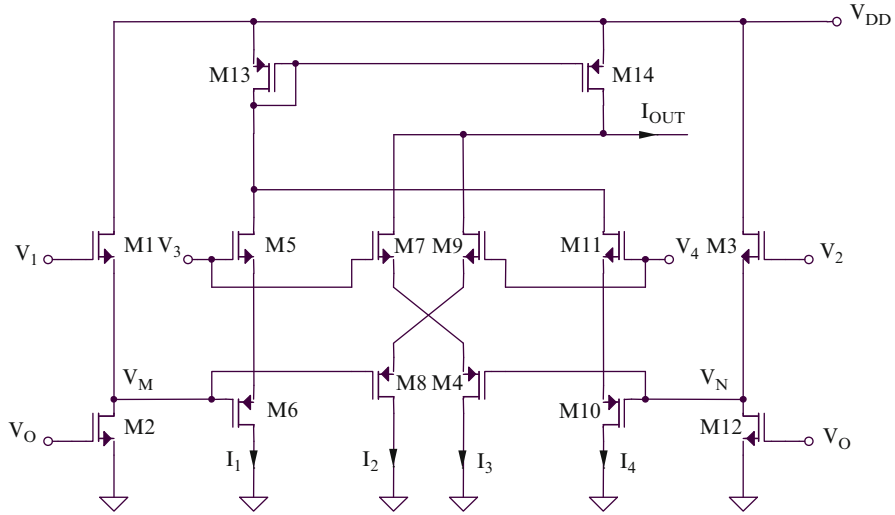
$$I_{D9} = \frac{K}{2} (V_5 - V_T)^2 = \frac{K}{2} [(V_{DD} - V_T) + (V_3 - V_1)]^2 \quad (2.52)$$

Similarly, the drain currents of M10, M11 and M12 transistors are

$$I_{D10} = \frac{K}{2} (V_6 - V_T)^2 = \frac{K}{2} [(V_{DD} - V_T) + (V_4 - V_2)]^2 \quad (2.53)$$

$$I_{D11} = \frac{K}{2} (V_7 - V_T)^2 = \frac{K}{2} [(V_{DD} - V_T) + (V_4 - V_1)]^2 \quad (2.54)$$

$$I_{D12} = \frac{K}{2} (V_8 - V_T)^2 = \frac{K}{2} [(V_{DD} - V_T) + (V_3 - V_2)]^2 \quad (2.55)$$



**Fig. 2.10** Multiplier circuit (3) based on PR 2.3

The output current of the voltage multiplier presented in Fig. 2.9 can be expressed as a linear relation using the previous currents:

$$I_{OUT} = I_{D9} + I_{D10} - I_{D11} - I_{D12} \quad (2.56)$$

resulting:

$$I_{OUT} = \frac{K}{2} (V_3 - V_4)(2V_{DD} - 2V_T + V_3 + V_4 - 2V_1) + \frac{K}{2} (V_4 - V_3)(2V_{DD} - 2V_T + V_3 + V_4 - 2V_2) \quad (2.57)$$

So, the circuit implements the voltage multiplying function:

$$I_{OUT} = K(V_3 - V_4)(V_2 - V_1) \quad (2.58)$$

A multiplier circuit using exclusively MOS transistors biased in saturation region, based on the third mathematical principle (PR 2.3), is presented in Fig. 2.10 [8].

The M1 and M2 transistors form a difference circuit that generates  $V_M$  potential. Considering identical transistors and because they are biased at the same drain current, it results equal gate-source voltages for these transistors. Thus,  $V_M$  potential will have the following expression:

$$V_M = V_1 - V_{GS1} = V_1 - V_{GS2} = V_1 - V_O \quad (2.59)$$

The gate-source voltage of M5 transistor can be obtained using the equality between gate-sources of M5 and M6 transistors:

$$V_3 - V_M = 2V_{GS5} \quad (2.60)$$

resulting:

$$V_{GS5} = \frac{V_3 - V_M}{2} = \frac{V_3 - V_1 + V_O}{2} \quad (2.61)$$

Thus, the expression of  $I_1$  current will be

$$I_1 = \frac{K}{2} (V_{GS5} - V_T)^2 = \frac{K}{2} \left( \frac{V_3 - V_1 + V_O}{2} - V_T \right)^2 \quad (2.62)$$

Similarly, it is possible to determine the expressions of  $I_2$ ,  $I_3$  and  $I_4$  currents:

$$I_2 = \frac{K}{2} \left( \frac{V_4 - V_1 + V_O}{2} - V_T \right)^2 \quad (2.63)$$

$$I_3 = \frac{K}{2} \left( \frac{V_3 - V_2 + V_O}{2} - V_T \right)^2 \quad (2.64)$$

$$I_4 = \frac{K}{2} \left( \frac{V_4 - V_2 + V_O}{2} - V_T \right)^2 \quad (2.65)$$

The output current can be expressed as a linear function of the previous currents:

$$I_{OUT} = I_1 + I_4 - I_2 - I_3 \quad (2.66)$$

resulting:

$$\begin{aligned} I_{OUT} = & \frac{K}{2} \frac{V_2 - V_1}{2} \left( \frac{2V_3 - V_1 - V_2 + 2V_O}{2} - 2V_T \right) \\ & - \frac{K}{2} \frac{V_2 - V_1}{2} \left( \frac{2V_4 - V_1 - V_2 + 2V_O}{2} - 2V_T \right) \end{aligned} \quad (2.67)$$

So

$$I_{OUT} = \frac{K}{4} (V_2 - V_1) (V_3 - V_4) \quad (2.68)$$

The multiplier circuit presented in Fig. 2.11 [9] implements the same mathematical principle PR 2.3 and it is composed from two differential amplifiers, M1–M4



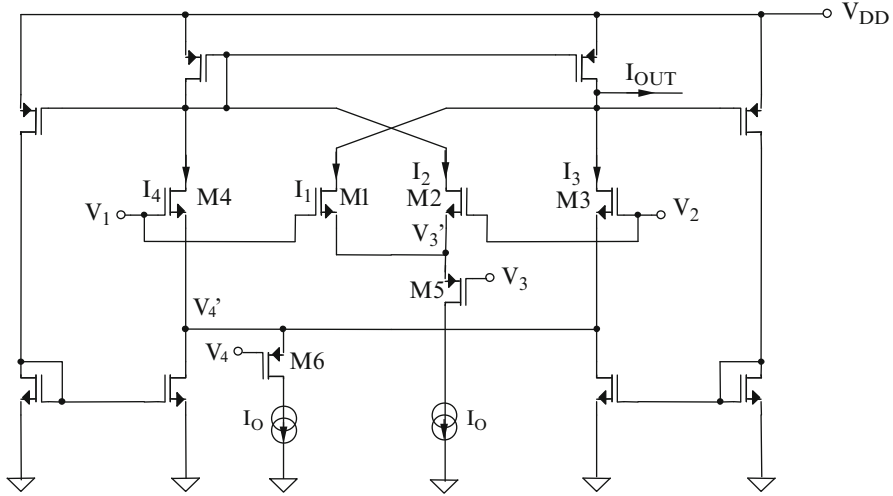


Fig. 2.12 Multiplier circuit (5) based on PR 2.3

Because M3 and M7 transistors are biased at a constant current,  $I_O$ , imposed by external current generators, the  $V$  and  $V'$  potentials can be expressed as follows:

$$V = V_3 + V_{SG3} = V_3 + V_T + \sqrt{\frac{2I_O}{K}} \quad (2.73)$$

and

$$V' = V_4 + V_{SG7} = V_4 + V_T + \sqrt{\frac{2I_O}{K}} \quad (2.74)$$

From (2.72), (2.73) and (2.74), it results the multiplying function implemented by the circuit from Fig. 2.11:

$$I_{OUT1} - I_{OUT2} = K(V_2 - V_1)(V_3 - V_4) \quad (2.75)$$

A possible realization of a voltage multiplier, based on the third mathematical principle (PR 2.3) is presented in Fig. 2.12 [10]. The core of the circuit is represented by the group of M1–M4 transistors. Using identical devices, their drain currents will have the following expressions:

$$I_1 = \frac{K}{2}(V_1 - V_3' - V_T)^2 \quad (2.76)$$

$$I_2 = \frac{K}{2}(V_2 - V_3' - V_T)^2 \quad (2.77)$$

$$I_3 = \frac{K}{2}(V_2 - V_4' - V_T)^2 \quad (2.78)$$

$$I_4 = \frac{K}{2}(V_1 - V_4' - V_T)^2 \quad (2.79)$$

As a result of using additional current mirrors, the output current of the differential structure will have a linear variation with respect to  $I_1 - I_4$  currents:

$$I_{OUT} = (I_2 - I_1) + (I_4 - I_3) \quad (2.80)$$

resulting:

$$\begin{aligned} I_{OUT} &= \frac{K}{2}(V_2 - V_1)(V_1 + V_2 - 2V_3' - 2V_T) \\ &+ \frac{K}{2}(V_1 - V_2)(V_1 + V_2 - 2V_4' - 2V_T) = K(V_1 - V_2)(V_3' - V_4') \end{aligned} \quad (2.81)$$

Because M5 and M6 transistors are biased at the constant current,  $I_O$ , they will introduce a voltage shifting between  $V_3$  and  $V_3'$  and, respectively, between  $V_4$  and  $V_4'$  potentials, as follows:

$$V_3' = V_3 + V_{SG5} = V_3 + V_T + \sqrt{\frac{2I_O}{K}} \quad (2.82)$$

and

$$V_4' = V_4 + V_{SG6} = V_4 + V_T + \sqrt{\frac{2I_O}{K}} \quad (2.83)$$

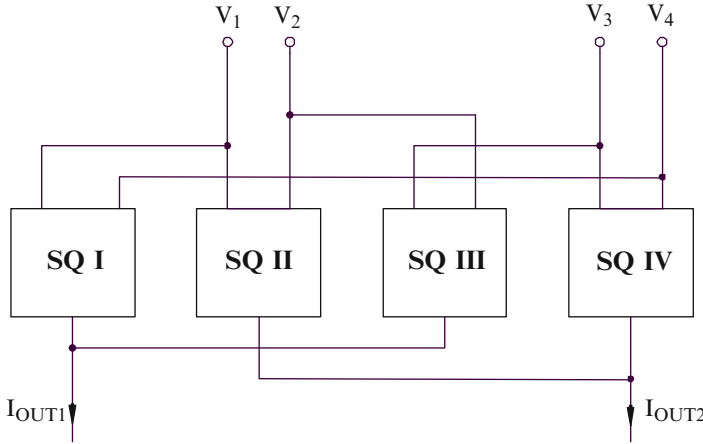
From the previous relations, it results the following expression of the output current:

$$I_{OUT} = K(V_1 - V_2)(V_3 - V_4) \quad (2.84)$$

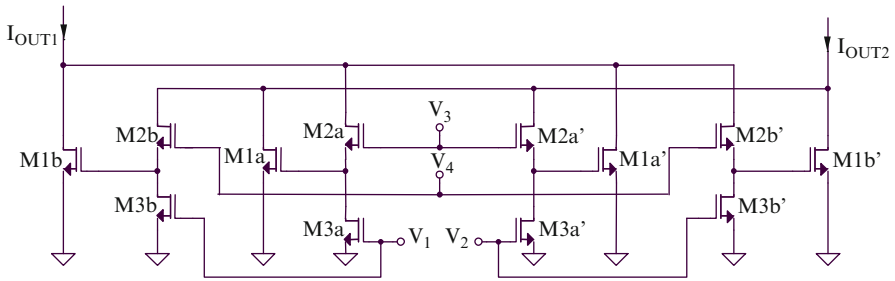
A voltage multiplier can be designed using 4 v squaring circuits (Fig. 2.13).

Considering that the output current of the voltage squaring circuits is equal with  $K\Delta V^2/2$   $\Delta V$  being its differential input voltage, the differential output current of the multiplier presented in Fig. 2.13 will have the following expression:

$$\begin{aligned} I_{OUT1} - I_{OUT2} &= \frac{K}{2}(V_1 - V_4)^2 + \frac{K}{2}(V_2 - V_3)^2 \\ &- \frac{K}{2}(V_1 - V_2)^2 - \frac{K}{2}(V_3 - V_4)^2 \end{aligned} \quad (2.85)$$



**Fig. 2.13** Multiplier circuit (6) based on PR 2.3 – block diagram



**Fig. 2.14** Multiplier circuit (7) based on PR 2.3

resulting:

$$I_{OUT1} - I_{OUT2} = K(V_1 - V_3)(V_2 - V_4) \quad (2.86)$$

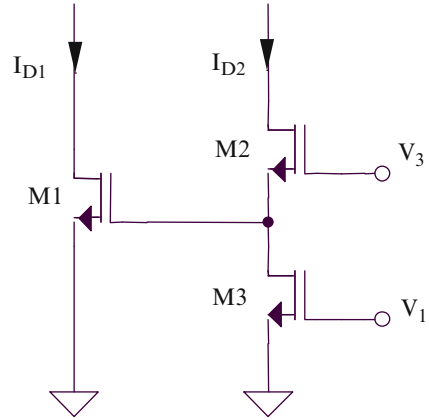
A voltage multiplier that illustrates the third mathematical principle PR 2.3 can be implemented using the symmetrical structure presented in Fig. 2.14 [11].

The circuit is derived from the core shown in Fig. 2.15 [11].

For this circuit core, the  $I_{D1} - I_{D2}$  differential output current can be computed replacing the expressions of drain currents by their squaring dependencies on the gate-source voltages (all MOS transistors are supposed to be biased in saturation region).

$$I_{D1} - I_{D2} = \frac{K}{2}(V_{GS1} - V_T)^2 - \frac{K}{2}(V_{GS3} - V_T)^2 \quad (2.87)$$

**Fig. 2.15** The core of the multiplier circuit (7) based on PR 2.3



The expression of the gate-source voltage of M1 transistor can be obtained using the equality between the gate-source voltages (if M2 and M3 transistors are identical and biased at the same drain current), resulting:

$$V_{GS1} = V_3 - V_{GS2} = V_3 - V_{GS3} = V_3 - V_1 \quad (2.88)$$

Replacing (2.88) in (2.87), the expression of the output differential current for the circuit presented in Fig. 2.14 can be expressed as follows:

$$\begin{aligned} I_{D1} - I_{D2} &= \frac{K}{2}(V_3 - V_1 - V_T)^2 - \frac{K}{2}(V_1 - V_T)^2 \\ &= \frac{K}{2}(V_3 - 2V_T)(V_3 - 2V_1) \end{aligned} \quad (2.89)$$

In order to implement a voltage multiplier circuit, two identical cores from Fig. 2.15 have to be used (Fig. 2.16 [11]), the input voltages for each of them being  $V_1$  and  $V_3$  and, respectively,  $V_2$  and  $V_3$ .

For simplifying the analysis of the circuit presented in Fig. 2.16, (2.89) relation can be used, the differential output current of the circuit from Fig. 2.16 being, practically, the difference between two differential output currents of two identical cores, excited using different input voltages:

$$I_L - I_R = (I_{D1}' + I_{D2}') - (I_{D2} + I_{D1}') = (I_{D1} - I_{D2}) - (I_{D1}' - I_{D2}') \quad (2.90)$$

Particularizing (2.89) relation for each circuit core, it results:

$$\begin{aligned} I_L - I_R &= \frac{K}{2}(V_3 - 2V_T)(V_3 - 2V_1) - \frac{K}{2}(V_3 - 2V_T)(V_3 - 2V_2) \\ &= K(V_2 - V_1)(V_3 - 2V_T) \end{aligned} \quad (2.91)$$



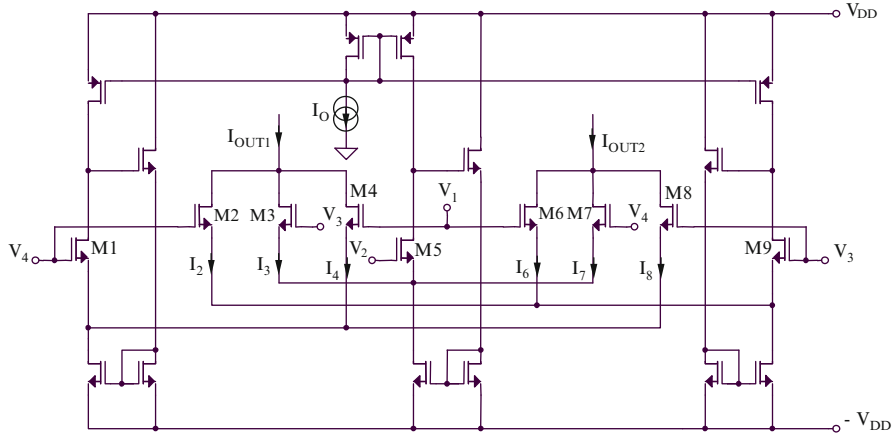


Fig. 2.17 Multiplier circuit (8) based on PR 2.3

$$V_{GS4} - V_{GS1} = V_1 - V_4 = \sqrt{\frac{2}{K}}(\sqrt{I_4} - \sqrt{I_O}) \quad (2.96)$$

$$V_{GS6} - V_{GS9} = V_1 - V_3 = \sqrt{\frac{2}{K}}(\sqrt{I_6} - \sqrt{I_O}) \quad (2.97)$$

$$V_{GS7} - V_{GS5} = V_4 - V_2 = \sqrt{\frac{2}{K}}(\sqrt{I_7} - \sqrt{I_O}) \quad (2.98)$$

and

$$V_{GS8} - V_{GS1} = V_3 - V_4 = \sqrt{\frac{2}{K}}(\sqrt{I_8} - \sqrt{I_O}) \quad (2.99)$$

resulting:

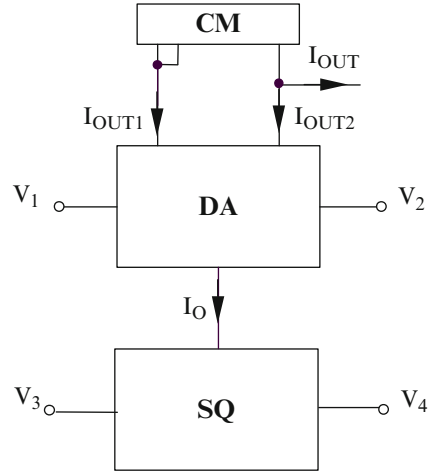
$$I_3 = I_O + \frac{K}{2}(V_3 - V_2)^2 + \sqrt{2KI_O}(V_3 - V_2) \quad (2.100)$$

$$I_4 = I_O + \frac{K}{2}(V_1 - V_4)^2 + \sqrt{2KI_O}(V_1 - V_4) \quad (2.101)$$

$$I_6 = I_O + \frac{K}{2}(V_1 - V_3)^2 + \sqrt{2KI_O}(V_1 - V_3) \quad (2.102)$$

$$I_7 = I_O + \frac{K}{2}(V_4 - V_2)^2 + \sqrt{2KI_O}(V_4 - V_2) \quad (2.103)$$

**Fig. 2.18** Multiplier circuit  
(1) based on PR 2.4 – general  
block diagram



and

$$I_8 = I_O + \frac{K}{2} (V_3 - V_4)^2 + \sqrt{2KI_O} (V_3 - V_4) \quad (2.104)$$

The differential output current for the multiplier circuit presented in Fig. 2.17 will have the following expression:

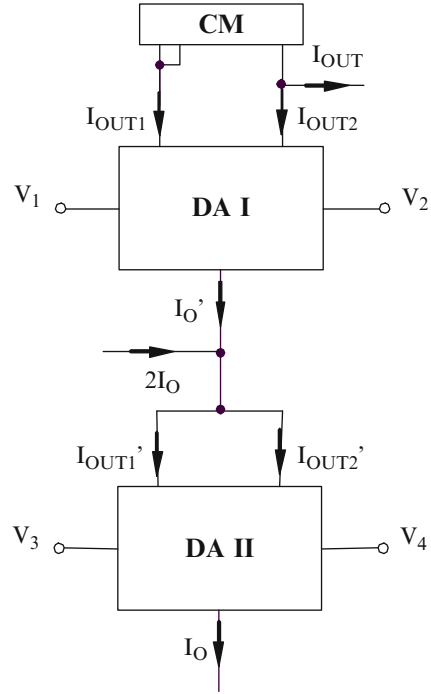
$$\begin{aligned} I_{OUT} &= I_{OUT1} - I_{OUT2} = I_2 + I_3 + I_4 - I_6 - I_7 - I_8 \\ &= K(V_1 - V_2)(V_3 - V_4) \end{aligned} \quad (2.105)$$

#### 2.2.1.4 Multiplier Circuits Based on the Fourth Mathematical Principle (PR 2.4)

This class of multiplier circuits presents the important advantage of generating, using the same circuit core, multiple circuit functions: amplifying, multiplying, squaring or simulating both positive and negative equivalent resistances.

A method for designing a voltage multiplier using the fourth mathematical principle (PR 2.4) is illustrated by the block diagram presented in Fig. 2.18, the biasing current of the first differential amplifier (with  $V_1 - V_2$  differential input voltage) being generated by a voltage squaring circuit having as input another differential voltage  $V_3 - V_4$ . Supposing that the  $G_m$  transconductance of the differential core is proportional with the square-root of the biasing current,  $I_O$  (an usual relation for a large class of differential amplifiers), the output current of the multiplier circuit will be proportional with the product between the input voltages of the differential amplifier and voltage squarer circuit.

**Fig. 2.19** Multiplier circuit  
(1) based on PR 2.4 – block  
diagram with SQ circuit  
implementation



The implementation of a voltage multiplier circuit can be simplified for a particular realization of the differential amplifier, having the transfer characteristic linearized using the method of constant sum of gate-source voltages. In this case, the squarer circuit from Fig. 2.18 can be implemented using the same differential amplifier, the sum of its output currents being proportional with the square of the differential voltage applied on the input pins. The block diagram presented in Fig. 2.18 can be re-drawn replacing the general voltage squarer with its particular implementation based on a differential amplifier (Fig. 2.19). The  $I_O$  current from Fig. 2.18 has been replaced with a  $I_O'$  current, linearly dependent on the output current of a squaring circuit from Fig. 2.19, having as input the  $V_3 - V_4$  differential voltage, as follows:

$$I_O' = I_{OUT1}' + I_{OUT2}' - 2I_O \quad (2.106)$$

A possible realization of the differential amplifier linearized using the previous principle is shown in Fig. 2.20 [13].

Considering a biasing in saturation of MOS transistors, the  $I_{OUT1}$  and  $I_{OUT2}$  output currents of the differential amplifier from Fig. 2.20 can be expressed as follows:

$$I_{OUT1} = \frac{K}{2} (V_{GS1} - V_T)^2 \quad (2.107)$$



In the particular case of implementing each  $V_O$  voltage source from Fig. 2.20 using a gate-source voltage of a MOS transistor biased in saturation region, it results:

$$V_O = V_T + \sqrt{\frac{2I_O}{K}} \quad (2.115)$$

so

$$I_{OUT} = \sqrt{8KI_O} (V_1 - V_2) \quad (2.116)$$

The sum of the output currents of the differential amplifier will have the following expression:

$$I_{OUT1} + I_{OUT2} = K(V_O - V_T)^2 + K(V_1 - V_2)^2 = 2I_O + K(V_1 - V_2)^2 \quad (2.117)$$

In conclusion, using in the block diagram of the voltage multiplier from Fig. 2.19 the particular implementation of the differential amplifier shown in Fig. 2.20, it is possible to write:

$$I_{OUT} = I_{OUT1} - I_{OUT2} = \sqrt{8KI_O'} (V_1 - V_2) \quad (2.118)$$

where  $I_O'$  current is linearly dependent on the sum of the output currents of the second differential amplifier:

$$I_O' = I_{OUT1}' + I_{OUT2}' - 2I_O = K(V_3 - V_4)^2 \quad (2.119)$$

Replacing (2.119) in (2.118), it results:

$$I_{OUT} = \sqrt{8K} (V_1 - V_2) (V_3 - V_4) \quad (2.120)$$

The complete implementation of the principle illustrated in the block diagram presented in Fig. 2.19 and the utilization of the method of realization shown in Fig. 2.20 allows many possible configurations.

The differential amplifier presented in Fig. 2.21 [14] is realized using M1 and M2 transistors and implements the  $V_O$  voltage sources from Fig. 2.20 using the gate-source voltages of M3 and M5 transistors, biased at the same constant current,  $I_O$ . So, the differential output current of the differential structure from Fig. 2.21,  $I_{OUT} = I_{OUT1} - I_{OUT2}$ , will be expressed by (2.116).

The realization of the multiplier circuit based on the block diagram from Fig. 2.19, using the differential amplifier presented in Fig. 2.21 [14] is shown in Fig. 2.22, the expression of the output current of the voltage multiplier shown in Fig. 2.22 being given by (2.120).

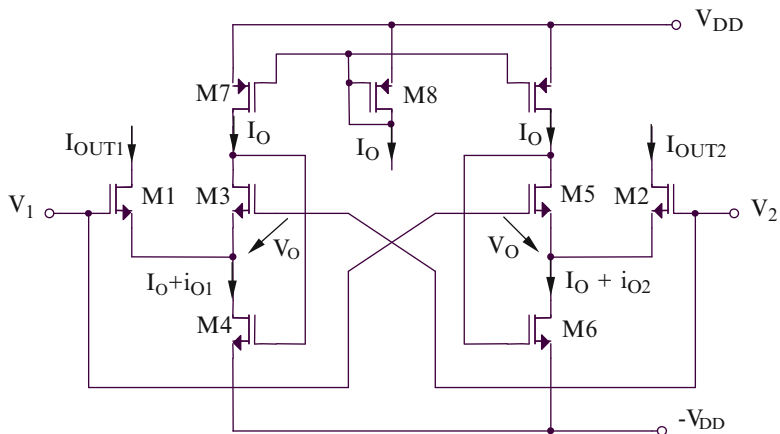


Fig. 2.21 Multiplier circuit (1) based on PR 2.4 – first implementation of DA block

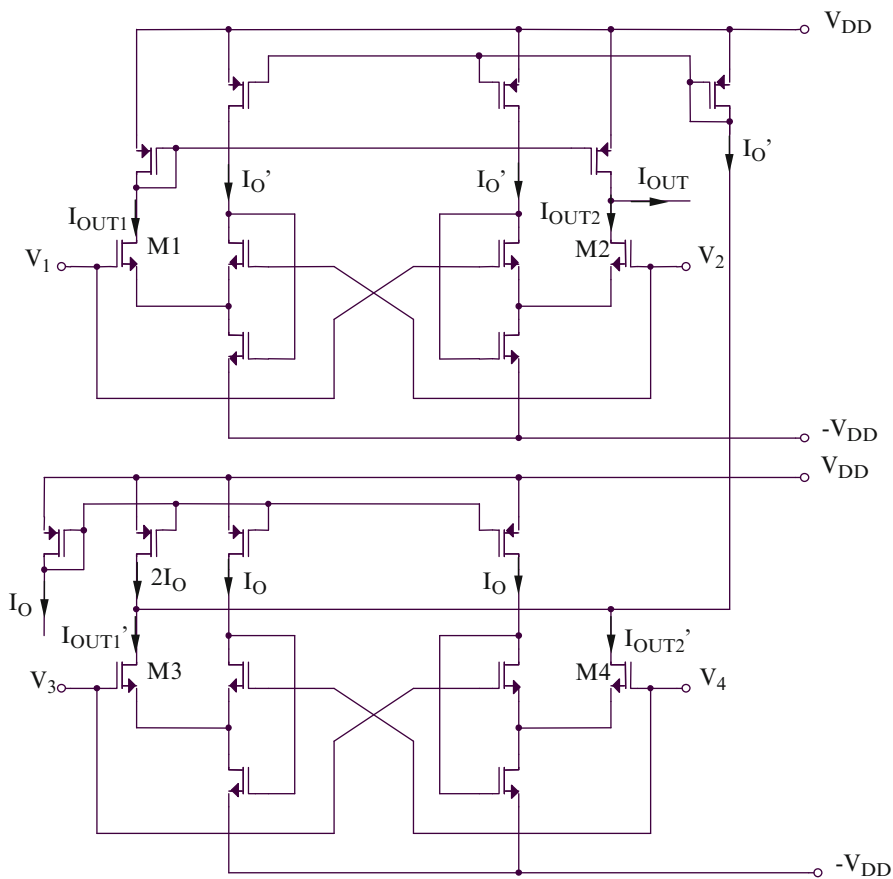
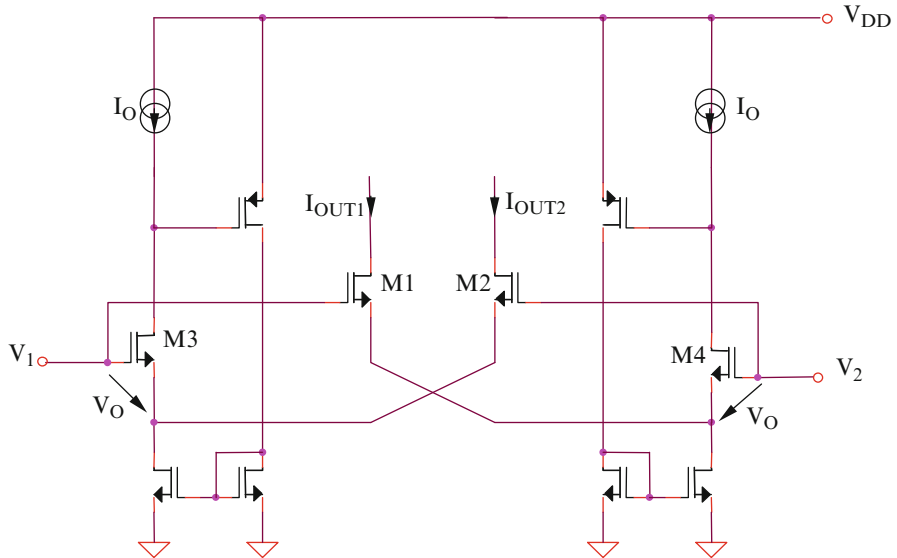


Fig. 2.22 Complete circuit of the multiplier from Fig. 2.19 using the first implementation of DA block



**Fig. 2.23** Multiplier circuit (1) based on PR 2.4 – second implementation of DA block

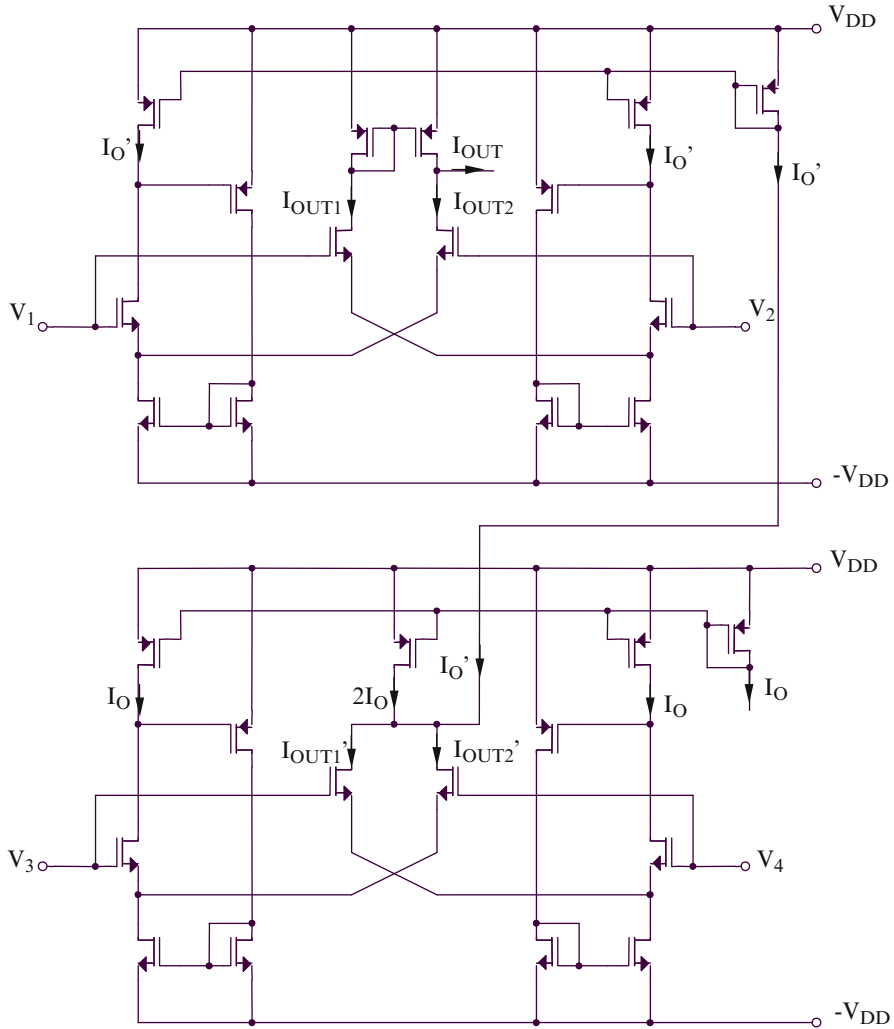
The second possible implementation of the previous presented principle uses as differential amplifier the circuit presented in Fig. 2.23 [14], the  $V_O$  voltage sources from Fig. 2.20 being realized using the gate-source voltages of M3 and M4 transistors, biased at the same constant current,  $I_O$ , while the differential amplifier is realized with M1 and M2 transistors. The output current of this differential amplifier is expressed by (2.116).

The complete realization of the voltage multiplier is shown in Fig. 2.24, the expression of its output current being given by (2.120).

The third implementation of a differential amplifier based on the principle shown in Fig. 2.20 is presented in Fig. 2.25 [13, 15], the  $V_O$  voltage sources from Fig. 2.20 being realized using the gate-source voltages of M3 and M4 transistors, biased at the same constant current,  $I_O$ . The output current of this differential amplifier (which is implemented using M1 and M2 transistors) is expressed by (2.116). The disadvantage of this realization of the differential amplifier comparing with the other proposals consists in a biasing of transistors M3 and M4 at variable currents.

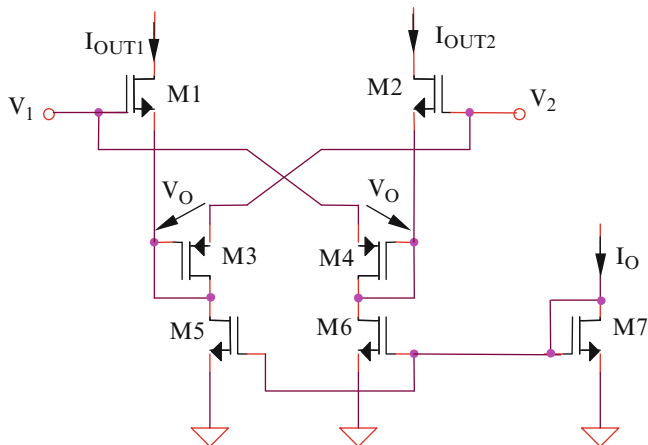
The complete realization of the voltage multiplier is shown in Fig. 2.26 [15], the expression of its output current being also given by (2.120).

The fourth implementation of a differential amplifier based on the principle shown in Fig. 2.20 is presented in Fig. 2.27 [16], the  $V_O$  voltage sources from Fig. 2.20 being realized using the gate-source voltages of M3a and M3b transistors, biased at the same constant current  $I_O$  (because  $I$  and  $I'$  currents are zero as a result of the circuit configuration). The output current of this differential amplifier is expressed by (2.116).

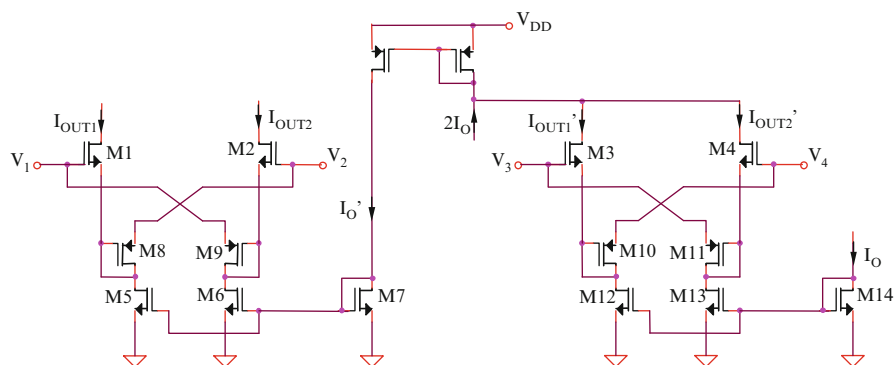


**Fig. 2.24** Complete circuit of the multiplier from Fig. 2.19 using the second implementation of DA block

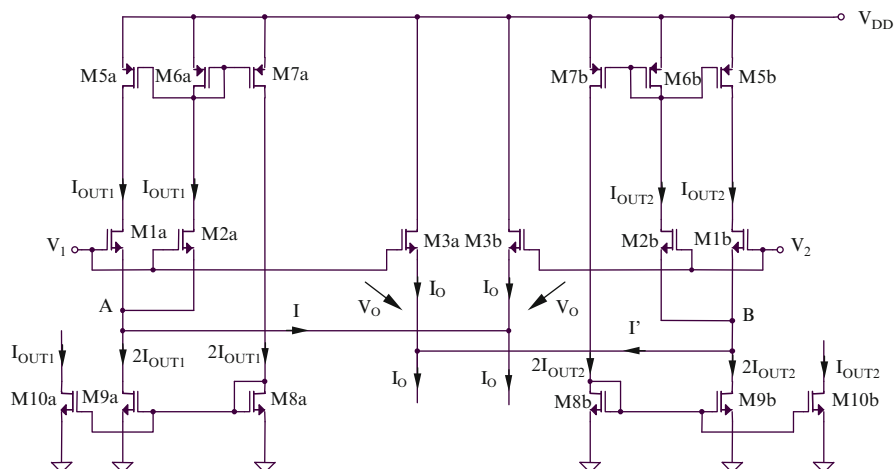
The fifth implementation of a differential amplifier based on the principle shown in Fig. 2.20 is presented in Fig. 2.28 [17], the  $V_O$  voltage sources from Fig. 2.20 being realized using the gate-source voltages of M3 and M4 transistors, biased at the same constant current,  $I_O$  (because  $I$  and  $I'$  currents are zero as a result of the circuit configuration). The output current of this differential amplifier (realized with M1 and M2 transistors) is expressed by (2.116).



**Fig. 2.25** Multiplier circuit (1) based on PR 2.4 – third implementation of DA block



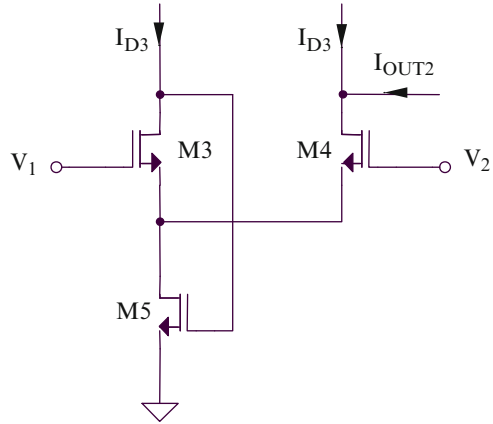
**Fig. 2.26** Complete circuit of the multiplier from Fig. 2.19 using the third implementation of DA block



**Fig. 2.27** Multiplier circuit (1) based on PR 2.4 – fourth implementation of DA block



**Fig. 2.30** Replicated core of the multiplier circuit (2) based on PR 2.4



Replacing the square-root dependence of the gate-source voltage on the drain current for a MOS transistor biased in saturation and considering identical transistors, it results:

$$V_1 - V_2 = \sqrt{\frac{2I_{D1}}{K}} - \sqrt{\frac{2I_{D2}}{K}} \quad (2.122)$$

equivalent with:

$$\sqrt{I_{D2}} = \sqrt{I_{D1}} - \sqrt{\frac{K}{2}}(V_1 - V_2) \quad (2.123)$$

Squaring the previous relation, it can be obtained that:

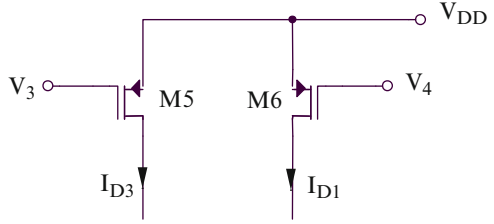
$$I_{D2} = I_{D1} - \sqrt{2KI_{D1}}(V_1 - V_2) + \frac{K}{2}(V_1 - V_2)^2 \quad (2.124)$$

Thus, the output current of the differential core presented in Fig. 2.29,  $I_{OUT1}$ , will have the following expression:

$$I_{OUT1} = I_{D2} - I_{D1} = -\sqrt{2KI_{D1}}(V_1 - V_2) + \frac{K}{2}(V_1 - V_2)^2 \quad (2.125)$$

In order to implement the multiplying function, the first linear dependent on the differential input voltage term from the previous relation will be used. The same core permits to realize also the squaring function using the second term from the same relation. The simplest way to remove the last quadratic term is to use a similar structure with the circuit from Fig. 2.29 (presented in Fig. 2.30) [18] and having the  $I_{D1}$  current replaced with another current,  $I_{D3}$ . As the quadratic term from (2.125) does not depend on  $I_{D1}$  and  $I_{D3}$  currents, the consideration

**Fig. 2.31** Differential amplifier for generating  $I_{D3}$  and  $I_{D1}$  currents



of the difference between the output currents of these similar structures will cancel out the undesired term.

Similarly with the previous analysis, the output current of the circuit from Fig. 2.30 will have the following expression:

$$I_{OUT2} = I_{D4} - I_{D3} = -\sqrt{2KI_{D3}}(V_1 - V_2) + \frac{K}{2}(V_1 - V_2)^2 \quad (2.126)$$

The difference between the output currents  $I_{OUT1}$  and  $I_{OUT2}$  will be

$$I_{OUT} = I_{OUT1} - I_{OUT2} = \sqrt{2K}(\sqrt{I_{D3}} - \sqrt{I_{D1}})(V_1 - V_2) \quad (2.127)$$

The  $I_{D3}$  and  $I_{D1}$  currents are generated by another differential amplifier M5–M6, having  $V_3 - V_4$  as differential input voltage (Fig. 2.31).

For this structure, considering that its composing transistors are biased in saturation, it is possible to write:

$$\sqrt{I_{D3}} - \sqrt{I_{D1}} = \sqrt{\frac{K}{2}}[(V_{DD} - V_3 - V_T) - (V_{DD} - V_4 - V_T)] = \sqrt{\frac{K}{2}}(V_4 - V_3) \quad (2.128)$$

Replacing (2.128) in (2.127) it results the multiplying function:

$$I_{OUT} = K(V_1 - V_2)(V_4 - V_3) \quad (2.129)$$

The complete circuit of the multiplier is presented in Fig. 2.32 [18]. The differential amplifier from Fig. 2.31 is replaced with two parallel-connected differential amplifiers M5, M5'–M6, M6' because  $I_{D1}$  and  $I_{D3}$  currents must be duplicated for biasing the differential amplifiers, M1–M2 and M3–M4.

Another possible implementation of a voltage multiplier uses the symmetrical structure presented in Fig. 2.33.

The multiplier is composed from two self-biased differential amplifiers (M5–M6 and M8–M9, respectively), their active loads being represented by

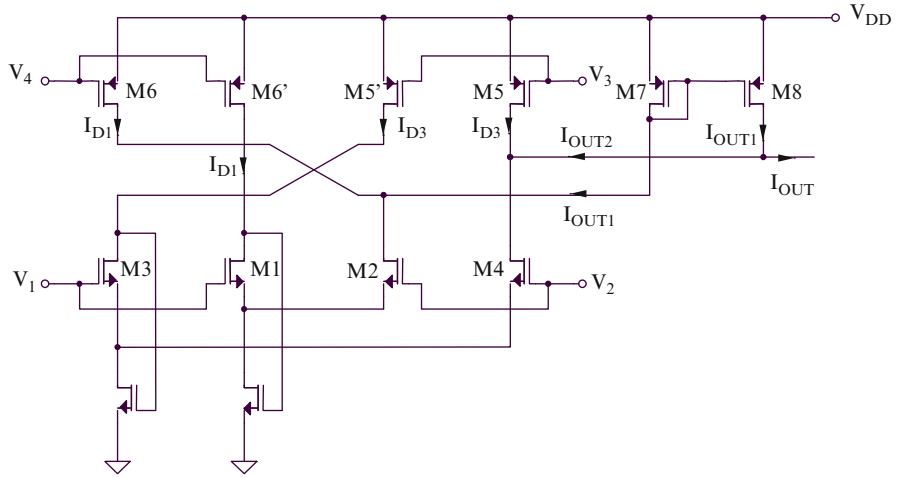


Fig. 2.32 The complete implementation of the multiplier circuit (2) based on PR 2.4

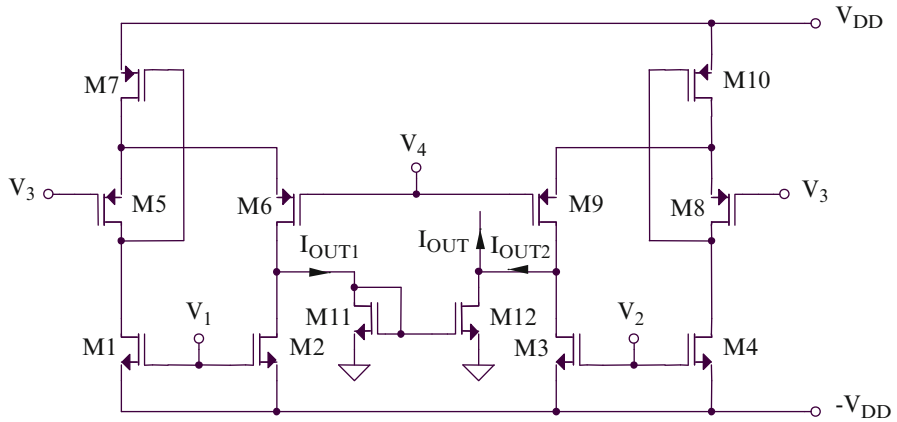


Fig. 2.33 Multiplier circuit (3) based on PR 2.4

M1–M2 and M3–M4 current mirrors. Analyzing the M5–M6 differential amplifier, the  $V_3 - V_4$  differential voltage can be expressed as a difference between two gate-source voltages:

$$V_3 - V_4 = V_{SG6} - V_{SG5} \quad (2.130)$$

Replacing the square-root dependence of the gate-source voltage on the drain current for a MOS transistor biased in saturation and considering identical transistors, it results:

$$V_3 - V_4 = \sqrt{\frac{2I_{D6}}{K}} - \sqrt{\frac{2I_{D1}}{K}} \quad (2.131)$$

The  $I_{D6}$  current can be expressed from the previous relation as follows:

$$\sqrt{I_{D6}} = \sqrt{I_{D1}} + \sqrt{\frac{K}{2}}(V_3 - V_4) \quad (2.132)$$

resulting:

$$I_{D6} = I_{D1} + \sqrt{2KI_{D1}}(V_3 - V_4) + \frac{K}{2}(V_3 - V_4)^2 \quad (2.133)$$

The differential output current of the M5–M6 differential amplifier will be:

$$I_{OUT1} = I_{D6} - I_{D1} = \sqrt{2KI_{D1}}(V_3 - V_4) + \frac{K}{2}(V_3 - V_4)^2 \quad (2.134)$$

Similarly, the differential output current of the M8–M9 differential amplifier will have the following expression:

$$I_{OUT2} = \sqrt{2KI_{D4}}(V_3 - V_4) + \frac{K}{2}(V_3 - V_4)^2 \quad (2.135)$$

The M11–M12 current mirror computes the  $I_{OUT}$  output current of the entire multiplier structure from Fig. 2.33:

$$I_{OUT} = I_{OUT2} - I_{OUT1} = \sqrt{2K}(V_3 - V_4)(\sqrt{I_{D4}} - \sqrt{I_{D1}}) \quad (2.136)$$

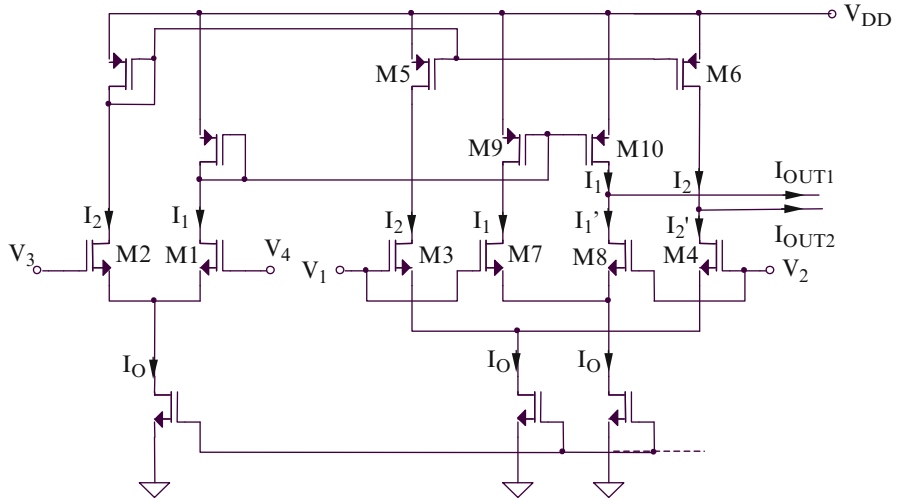
Using the squaring dependence of the drain current on the gate-source voltage for a MOS transistor biased in saturation, it is possible to write:

$$\begin{aligned} I_{OUT} &= \sqrt{2K}(V_3 - V_4) \left[ \sqrt{\frac{K}{2}}(V_2 + V_{DD} - V_T) - \sqrt{\frac{K}{2}}(V_1 + V_{DD} - V_T) \right] \\ &= K(V_3 - V_4)(V_2 - V_1) \end{aligned} \quad (2.137)$$

A voltage multiplier based on the compensation of the squaring characteristic of the MOS transistor biased in saturation region using two square-root circuits is presented in Fig. 2.34 [19].

The differential input voltage can be expressed as follows:

$$V_1 - V_2 = V_{GS3} - V_{GS4} = \sqrt{\frac{2}{K}}(\sqrt{I_2} - \sqrt{I_2'}) \quad (2.138)$$



**Fig. 2.34** Multiplier circuit (4) based on PR 2.4

resulting:

$$I_2' = I_2 + \frac{K}{2}(V_1 - V_2)^2 - \sqrt{2K}(V_1 - V_2)\sqrt{I_2} \quad (2.139)$$

The output current of the square-rooting circuit is:

$$I_{OUT2} = I_2 - I_2' = -\frac{K}{2}(V_1 - V_2)^2 + \sqrt{2K}(V_1 - V_2)\sqrt{I_2} \quad (2.140)$$

Similarly:

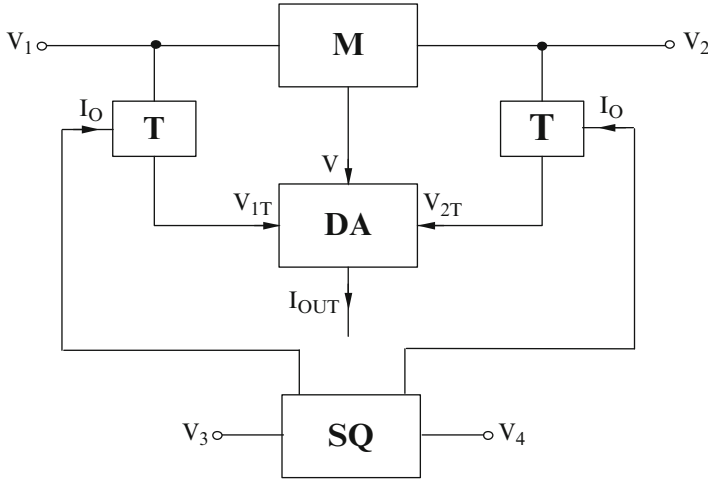
$$I_{OUT1} = I_1 - I_1' = -\frac{K}{2}(V_1 - V_2)^2 + \sqrt{2K}(V_1 - V_2)\sqrt{I_1} \quad (2.141)$$

so:

$$I_{OUT} = I_{OUT2} - I_{OUT1} = \sqrt{2K}(V_1 - V_2)(\sqrt{I_2} - \sqrt{I_1}) \quad (2.142)$$

The differential input voltage of M1–M2 differential amplifier will have the following expression:

$$V_3 - V_4 = V_{GS2} - V_{GS1} = \sqrt{\frac{2}{K}}(\sqrt{I_2} - \sqrt{I_1}) \quad (2.143)$$



**Fig. 2.35** Multiplier circuit (5) based on PR 2.4 – block diagram

resulting:

$$I_{OUT} = K(V_1 - V_2)(V_3 - V_4) \quad (2.144)$$

A possible implementation of a voltage multiplier has the block diagram presented in Fig. 2.35. The “DA” block represents a classical active-load differential amplifier, having the common-sources point biased at a  $V$  potential fixed by the circuit “M”. This circuit computes the arithmetical mean of input potentials, having the goal of obtaining a very good linearity of the entire structure, with the contribution of “T” blocks (which are used for introducing a translation of input potentials). A squaring circuit, “SQ”, is used for generating the biasing current of the two translation blocks,  $I_O$ .

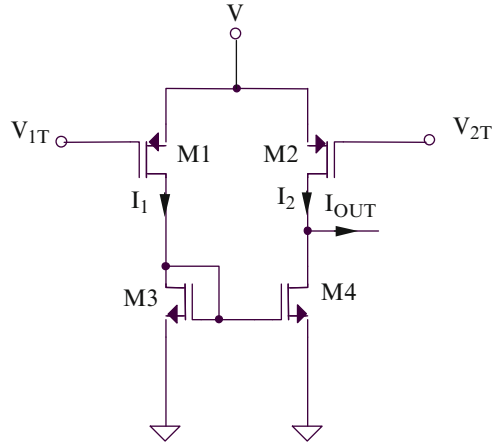
The “DA” (Differential Amplifier) block

The “DA” block is implemented as a classical active-load differential amplifier, having the concrete realization presented in Fig. 2.36 [20].

Considering a biasing in saturation of the MOS devices from Fig. 2.36, the output current of the differential amplifier can be expressed as follows:

$$I_{OUT} = I_2 - I_1 = \frac{K}{2}(V_{SG2} - V_T)^2 - \frac{K}{2}(V_{SG1} - V_T)^2 \quad (2.145)$$

**Fig. 2.36** Multiplier circuit  
(5) based on PR 2.4 –  
implementation of DA block



equivalent with:

$$I_{OUT} = \frac{K}{2} (V_{SG2} - V_{SG1}) (V_{SG1} + V_{SG2} - 2V_T) \quad (2.146)$$

Because:

$$V_{SG1} = V - V_{1T} \quad (2.147)$$

and:

$$V_{SG2} = V - V_{2T} \quad (2.148)$$

it results:

$$I_{OUT} = \frac{K}{2} (V_{1T} - V_{2T}) (2V - V_{1T} - V_{2T} - 2V_T) \quad (2.149)$$

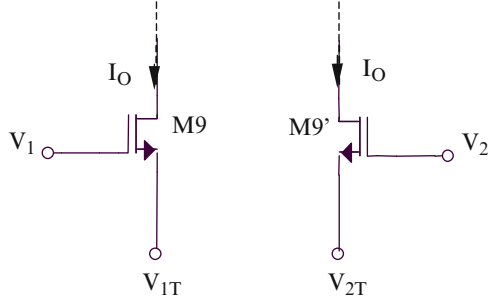
In order to obtain a linear transfer characteristic  $I_{OUT}(V_{1T} - V_{2T})$ , it is necessary that the second parenthesis from (2.149) to be constant with respect to the differential input voltage,  $V_{1T} - V_{2T}$ :

$$2V - V_{1T} - V_{2T} - 2V_T = A = ct. \quad (2.150)$$

resulting the necessity of implementing a  $V$  voltage equal with:

$$V = \frac{V_{1T} + V_{2T}}{2} + V_T + \frac{A}{2} \quad (2.151)$$

**Fig. 2.37** Multiplier circuit  
(5) based on PR 2.4 –  
implementation of T block



### The “T” (Translation) Block

The translation of the  $V$  potential by  $V_T + A/2$  (relation (2.151)) can be obtained using “T” block, having the implementation presented in Fig. 2.37 [20].

Because the same  $I_O$  current is passing through all transistors from Fig. 2.37, it is possible to write that:

$$V_1 = V_{1T} + V_T + \sqrt{\frac{2I_O}{K}} \quad (2.152)$$

and:

$$V_2 = V_{2T} + V_T + \sqrt{\frac{2I_O}{K}} \quad (2.153)$$

So, both  $V_1$  and  $V_2$  input potentials are DC shifted with the same amount,  $V_T + \sqrt{2I_O/K}$ .

### The “M” (Arithmetic Mean) Block

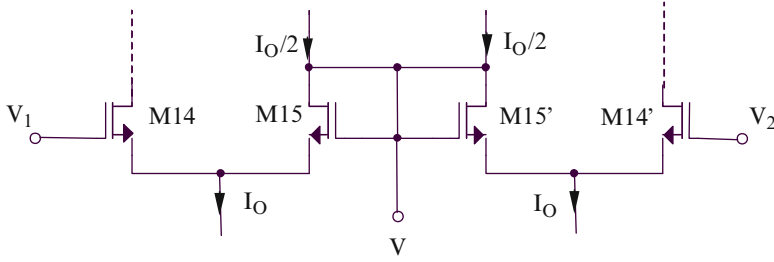
In order to obtain the arithmetic mean of input potentials expressed by relation (2.151), the circuit from Fig. 2.38 [20] can be used, having the advantage of using only MOS transistors, biased in saturation region.

The expression of the  $V$  potential is:

$$V = \frac{V_1 + V_2}{2} \quad (2.154)$$

Replacing (2.152) and (2.153) in (2.156), it can be obtained:

$$V = \frac{V_{1T} + V_{2T}}{2} + V_T + \sqrt{\frac{2I_O}{K}} \quad (2.155)$$



**Fig. 2.38** Multiplier circuit (1) based on PR 2.4 – implementation of M block

Comparing relations (2.151) and (2.157), it results that  $A = 2\sqrt{2I_O/K}$ , so:

$$I_{OUT} = \frac{K}{2} (V_{1T} - V_{2T}) 2\sqrt{\frac{2I_O}{K}} \quad (2.156)$$

or:

$$I_{OUT} = \sqrt{2KI_O} (V_{1T} - V_{2T}) \quad (2.157)$$

equivalently (using (2.152) and (2.153)) with:

$$I_{OUT} = \sqrt{2KI_O} (V_1 - V_2) = G_m (V_1 - V_2) \quad (2.158)$$

resulting:

$$I_{OUT} = \sqrt{2KI_O} (V_1 - V_2) = G_m (V_1 - V_2) \quad (2.159)$$

$G_m = \sqrt{2KI_O}$  being the equivalent transconductance of the differential amplifier.

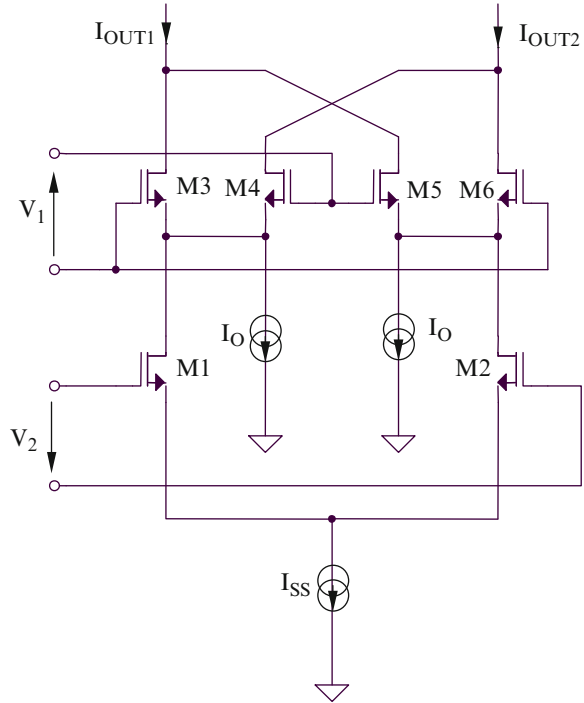
Because  $I_O$  biasing currents of the translation blocks “T” from Fig. 2.37 are generated by a voltage squaring circuit having as input a differential voltage,  $V_3 - V_4$ , it results a multiplier circuit with a very good linearity. So, replacing in (2.159) the expression of  $I_O$  current:

$$I_O = \frac{K}{4} (V_3 - V_4)^2 \quad (2.160)$$

it results:

$$I_{OUT} = \frac{K}{\sqrt{2}} (V_1 - V_2) (V_3 - V_4) \quad (2.161)$$

**Fig. 2.39** Multiplier circuit  
(1) based on PR 2.5



### 2.2.1.5 Multiplier Circuits Based on the Fifth Mathematical Principle (PR 2.5)

A method for linearizing the characteristic of a voltage multiplier using the fifth mathematical principle consists in the extension of the linearization technique designed for the CMOS differential amplifier, based on the biasing of the differential structure at a current that is the sum between a constant current and a component proportional with the square of the differential input voltage. The relatively simple implementation of multiplier circuits based on this mathematical principle impose them for a large area of applications in VLSI designs. The expression of the differential output current of the classical CMOS differential amplifier is:

$$I_{OUT} = KV_I \sqrt{\frac{I_{SS}}{K} - \frac{V_I^2}{4}} \quad (2.162)$$

$V_I$  representing the differential input voltage and  $I_{SS}$  being the biasing current of the differential amplifier.

The multiplier with linear characteristic based on the previous presented principle is presented in Fig. 2.39 [21].

The output current of the previous voltage multiplier can be expressed as:

$$\begin{aligned} I_{OUT} &= I_{OUT1} - I_{OUT2} = (I_{D3} + I_{D5}) - (I_{D4} + I_{D6}) \\ &= (I_{D3} - I_{D4}) - (I_{D6} - I_{D5}) \end{aligned} \quad (2.163)$$

The differential output currents of the differential amplifiers M3–M4 and M5–M6 can be obtained using the general relation (2.162):

$$I_{D3} - I_{D4} = KV_1 \sqrt{\frac{I_{D1} + I_O}{K} - \frac{V_1^2}{4}} \quad (2.164)$$

and:

$$I_{D6} - I_{D5} = K V_1 \sqrt{\frac{I_{D2} + I_O}{K} - \frac{V_1^2}{4}} \quad (2.165)$$

The linearization technique is based on the utilization of a current  $I_O$  proportional with the squaring of the differential input voltage  $V_1$ :

$$I_O = \frac{KV_1^2}{4} \quad (2.166)$$

Replacing (2.164), (2.165) and (2.166) in (2.163), it results the following expression of the output current of the voltage multiplier:

$$I_{OUT} = \sqrt{K}V_1(\sqrt{I_{D1}} - \sqrt{I_{D2}}) \quad (2.167)$$

Analyzing M1–M2 differential amplifier, the  $V_2$  differential input voltage can be expressed as follows:

$$\begin{aligned} V_2 &= V_{GS1} - V_{GS2} = \left( V_T + \sqrt{\frac{2I_{D1}}{K}} \right) - \left( V_T + \sqrt{\frac{2I_{D2}}{K}} \right) \\ &= \sqrt{\frac{2}{K}}(\sqrt{I_{D1}} - \sqrt{I_{D2}}) \end{aligned} \quad (2.168)$$

From (2.168) and (2.167), it results the expression of the  $I_{OUT}$  output current as a function on the differential input voltages,  $V_1$  and  $V_2$ :

$$I_{OUT} = \frac{K}{\sqrt{2}} V_1 V_2 \quad (2.169)$$

A similar method, useful for low-voltage operation, is presented in Fig. 40 [21]. In order to reduce the minimal value of the supply voltage, the stacked architecture is replaced with a folded structure.

The  $I_{OUT1} - I_{OUT2}$  differential output current of the folded voltage multiplier is:

$$\begin{aligned} I_{OUT1} - I_{OUT2} &= (I_{D3} + I_{D5}) - (I_{D4} + I_{D6}) \\ &= (I_{D3} - I_{D4}) - (I_{D6} - I_{D5}) \end{aligned} \quad (2.170)$$

The differential output currents of the differential amplifiers M3–M4 and M5–M6 can be obtained using the general relation (2.162):

$$I_{D3} - I_{D4} = KV_1 \sqrt{\frac{I_{SS} + I_O - I_{D1}}{K} - \frac{V_1^2}{4}} \quad (2.171)$$

and:

$$I_{D6} - I_{D5} = KV_1 \sqrt{\frac{I_{SS} + I_O - I_{D2}}{K} - \frac{V_1^2}{4}} \quad (2.172)$$

The linearization technique is based on the utilization of a  $I_O$  current, proportional with the square of the differential input voltage  $V_1$ :

$$I_O = \frac{KV_1^2}{4} \quad (2.173)$$

Replacing (2.171), (2.172) and (2.173) in (2.170), it results the following expression of the output current of the voltage multiplier:

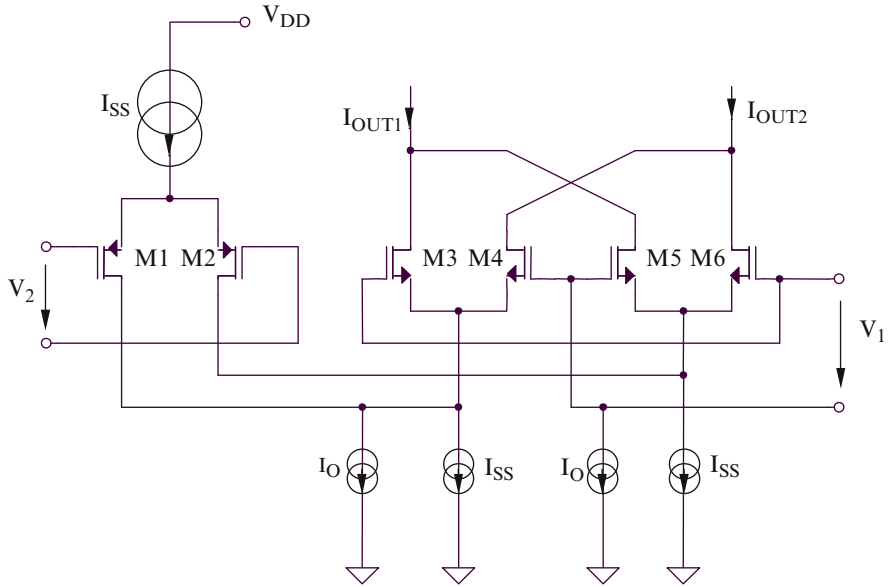
$$I_{OUT} = \sqrt{K}V_1 \left( \sqrt{I_{SS} - I_{D1}} - \sqrt{I_{SS} - I_{D2}} \right) \quad (2.174)$$

The M1–M2 differential amplifier is biased at the constant current,  $I_{SS}$ , so  $I_{D1} + I_{D2} = I_{SS}$ . The previous relation can be rewritten as:

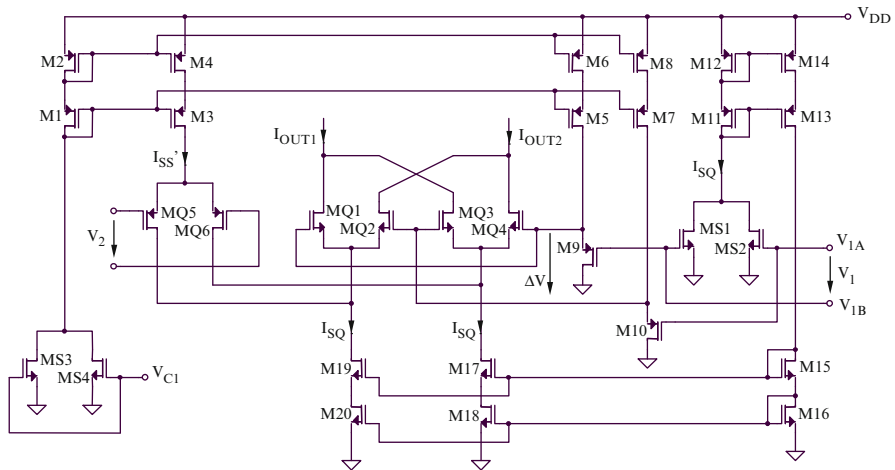
$$I_{OUT} = \sqrt{K}V_1 (\sqrt{I_{D2}} - \sqrt{I_{D1}}) \quad (2.175)$$

Similarly with the previous voltage multiplier, it results the following expression of the  $I_{OUT}$  output current as a function on  $V_1$  and  $V_2$  differential input voltages:

$$I_{OUT} = \frac{K}{\sqrt{2}} V_1 V_2 \quad (2.176)$$



**Fig. 2.40** Multiplier circuit (1) based on PR 2.5 – circuit core of the folded version



**Fig. 2.41** Multiplier circuit (1) based on PR 2.5 – complete implementation of the folded version

The complete implementation of the folded voltage multiplier from Fig. 2.40 is presented in Fig. 2.41 [21].

The M1 and M2 transistors from Fig. 2.40 have been replaced in Fig. 2.41 with MQ5 and MQ6, while the differential amplifiers, M3–M4 and M5–M6 from Fig. 2.40 were renamed MQ1–MQ2 and MQ3–MQ4, respectively. Noting with  $I_{SQ}$  the drain

currents of transistors M11–M20 and considering that the cascode current mirrors implemented using M11–M20 transistors are not affected by the channel-length modulation, the  $I_{SQ}$  current will have the following expression:

$$I_{SQ} = I_{DMS1} + I_{DMS2} \quad (2.177)$$

For simplifying the computations, the differential input voltage  $V_1 = V_{1A} - V_{1B}$ , can be expressed using a linear relation between the common-mode and the differential-mode input voltages,  $V_{C1}$  and  $v_1$ :

$$V_{1A} = V_{C1} - \frac{v_1}{2} \quad (2.178)$$

and:

$$V_{1B} = V_{C1} + \frac{v_1}{2} \quad (2.179)$$

Using this expression of  $V_1$  voltage, the  $I_{SQ}$  current can be expressed as follows:

$$\begin{aligned} I_{SQ} &= \frac{K}{2}(V_{1A} - V_T)^2 + \frac{K}{2}(V_{1B} - V_T)^2 \\ &= \frac{K}{2}\left(V_{C1} - \frac{v_1}{2} - V_T\right)^2 + \frac{K}{2}\left(V_{C1} + \frac{v_1}{2} - V_T\right)^2 \end{aligned} \quad (2.180)$$

resulting:

$$I_{SQ} = K(V_{C1} - V_T)^2 + \frac{K}{4}v_1^2 \quad (2.181)$$

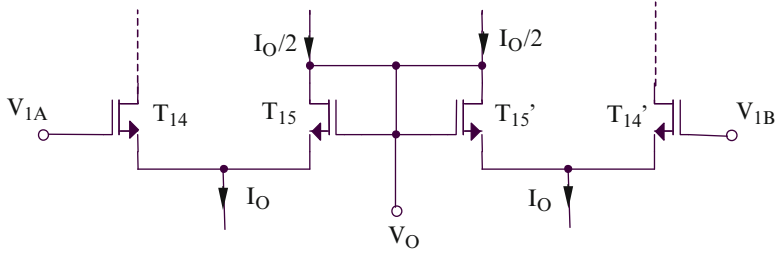
Comparing Fig. 2.40 with Fig. 2.41, it results that  $I_{SQ}$  current from Fig. 2.41 must be equal with a sum between a constant current,  $I_{SS}$  and a  $I_O$  current, proportional with the squaring of the input voltage:

$$I_{SS} = K(V_{C1} - V_T)^2 \quad (2.182)$$

and:

$$I_O = \frac{K}{4}v_1^2 \quad (2.183)$$

For a proper operation of the folded multiplier, the  $I_{SS}'$  biasing current of the differential amplifier MQ5–MQ6 must be equal with  $I_{SS}$ . This  $I_{SS}'$  current is



**Fig. 2.42** Arithmetical mean circuit

generated by the MS3–MS4 pair, each transistor being biased at the common-mode component of the input voltage  $V_1$ :

$$I_{SS}' = I_{DMS3} + I_{DMS4} \quad (2.184)$$

resulting:

$$I_{SS}' = 2 \frac{K}{2} (V_{C1} - V_T)^2 = K (V_{C1} - V_T)^2 = I_{SS} \quad (2.185)$$

The M9 and M10 transistors are used for transferring the differential input voltage,  $V_1$ , on the input of cross-connected differential amplifiers MQ1–MQ2 and MQ3–MQ4:

$$\Delta V = (V_{1B} + V_{SG9}) - (V_{1A} + V_{SG10}) \quad (2.186)$$

The M9 and M10 transistors being identical and working at the same drain current, it results  $V_{SG9} = V_{SG10}$ . So:

$$\Delta V = V_{1B} - V_{1A} = -V_1 \quad (2.187)$$

Concluding that the circuits presented in Fig. 2.40 and Fig. 2.41 are functionally identical, the  $I_{OUT}$  output current of the complete implementation of the folded voltage multiplier circuit can be obtained replacing in (2.176)  $V_1$  with  $-V_1$ :

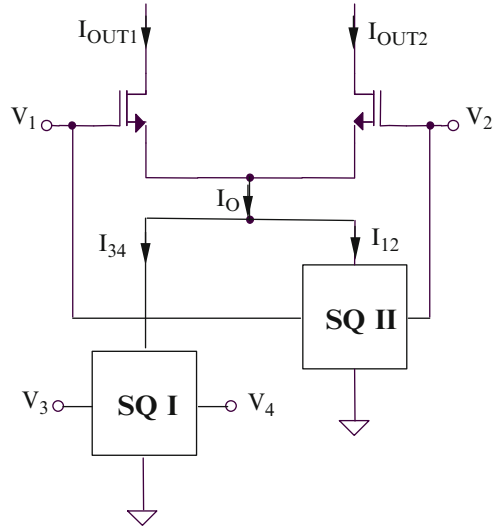
$$I_{OUT} = I_{OUT1} - I_{OUT2} = -\frac{K}{\sqrt{2}} V_1 V_2 \quad (2.188)$$

An arithmetical mean circuit (Fig. 2.42) [22] must be used for extracting the common-mode component  $V_{C1}$  of the input voltage  $V_1$ .

The  $V_O$  output voltage for this circuit will be:

$$V_O = \frac{V_{1A} + V_{1B}}{2} = V_{C1} \quad (2.189)$$

**Fig. 2.43** Multiplier circuit  
(2) based on PR 2.5



The voltage multiplier presented in Fig. 2.43 [23], using the fifth mathematical principle (PR 2.5) is derived from a differential amplifier with linear transfer characteristic.

The differential output current,  $I_{OUT}$ , for the circuit presented in Fig. 2.43 will present a strong nonlinear dependence on the  $V_1 - V_2$  differential input voltage, that can be expressed as:

$$I_{OUT} = I_{OUT1} - I_{OUT2} = I_O \sqrt{\frac{K(V_1 - V_2)^2}{I_O} - \frac{K^2(V_1 - V_2)^4}{4I_O^2}} \quad (2.190)$$

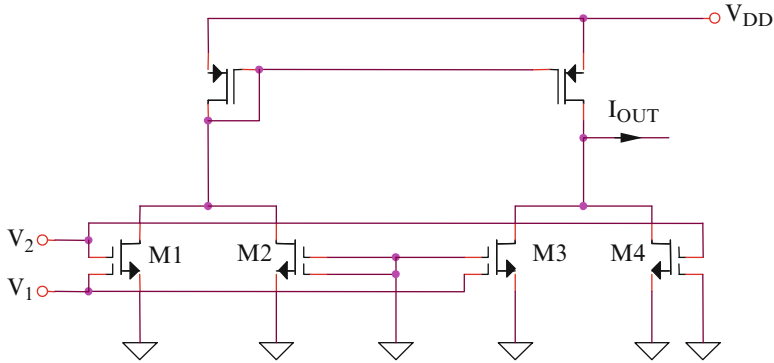
equivalent with:

$$I_{OUT} = \frac{V_1 - V_2}{2} \sqrt{4KI_O - K^2(V_1 - V_2)^2} \quad (2.191)$$

$I_O$  being the biasing current of the differential structure. So, superior-order distortions will characterize the behavior of this structure, imposing the design of a linearization technique for removing the superior-order terms from the transfer characteristic. The method for obtaining a linear transfer characteristic is to obtain the  $I_O$  bias current of the entire differential structure as a sum of two terms:  $I_{12}$ , proportional with the squaring of the  $V_1 - V_2$  differential input voltage and  $I_{34}$ , proportional with the squaring of another differential voltage,  $V_3 - V_4$ :

$$I_O = I_{12} + I_{34} = \frac{K}{4}(V_1 - V_2)^2 + \frac{K}{4}(V_3 - V_4)^2 \quad (2.192)$$





**Fig. 2.45** Multiplier circuit (2) based on PR 2.6

$$I_4 = \frac{K}{2} \left( \frac{V_2}{2} - V_T \right)^2 \quad (2.198)$$

For the previous mathematical relations, it results a perfect linear dependence of the output current on the input voltages:

$$I_{OUT} = \frac{K}{2} V_1 V_2 \quad (2.199)$$

Another possible implementation of a voltage multiplier circuit using the sixth mathematical principle (PR 2.6) is presented in Fig. 2.45.

The output current of the voltage multiplier can be expressed as follows:

$$I_{OUT} = (I_{D1} + I_{D2}) - (I_{D3} + I_{D4}) \quad (2.200)$$

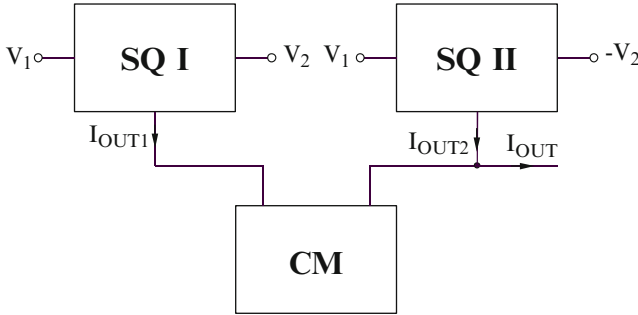
where:

$$I_{D1} = \frac{K}{2} \left( \frac{V_1 + V_2}{2} - V_T \right)^2 \quad (2.201)$$

$$I_{D2} = \frac{K}{2} V_T^2 \quad (2.202)$$

$$I_{D3} = \frac{K}{2} \left( \frac{V_1}{2} - V_T \right)^2 \quad (2.203)$$

$$I_{D4} = \frac{K}{2} \left( \frac{V_2}{2} - V_T \right)^2 \quad (2.204)$$



**Fig. 2.46** Multiplier circuit (1) based on PR 2.7 – block diagram

From the previous mathematical relations it results a perfect linear dependence of the output current on the input voltages:

$$I_{OUT} = \frac{K}{2} V_1 V_2 \quad (2.205)$$

### 2.2.1.7 Multiplier Circuits Based on the Seventh Mathematical Principles (PR 2.7)

Practically derived from the implementation of voltage squaring circuits, the multiplier structures that use as functional basis PR 2.7 find many applications in analog signal processing.

A similar approach of a voltage multiplier uses 2 v squaring circuit, connected as it is shown in Fig. 2.46.

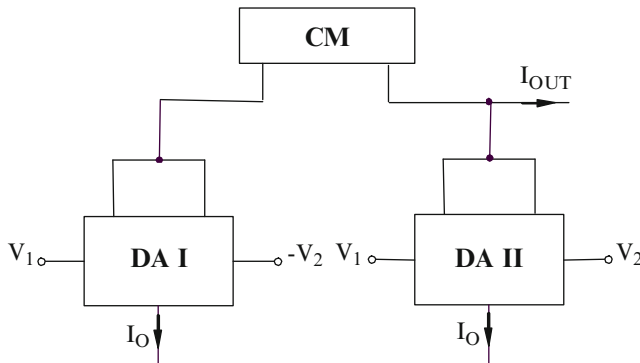
Considering that the squaring circuits have an output current proportional with  $K\Delta V^2/2$ ,  $\Delta V$  being the differential input voltage, the output current of the circuit presented in Fig. 2.46 will have the following expression:

$$I_{OUT} = I_{OUT2} - I_{OUT1} = \frac{K}{2} (V_1 + V_2)^2 - \frac{K}{2} (V_1 - V_2)^2 = 2KV_1 V_2 \quad (2.206)$$

In order to obtain the multiplying function using two squaring circuits, a similar method is proposed in Fig. 2.47. The squaring circuits from Fig. 2.46 have been replaced in Fig. 2.47 with two particular implementations of a differential amplifier (presented in Fig. 2.20).

The implementation of the voltage multiplier is shown in Fig. 2.28 [13]. The  $I_{OUT}$  output current will have the following expression:

$$I_{OUT} = \left[ 2I_O + K(V_1 + V_2)^2 \right] - \left[ 2I_O + K(V_1 - V_2)^2 \right] = 4KV_1 V_2 \quad (2.207)$$



**Fig. 2.47** Multiplier circuit (2) based on PR 2.7 – block diagram

Two complete realizations of the previous circuit, using specific implementations of  $V_O$  sources from Fig. 2.48, are shown in Fig. 2.49 [13] and Fig. 2.50 [13], respectively.

A multiplier circuit can be designed starting from a squaring characteristic implemented using a classical differential amplifier (Fig. 2.51) [18].

The differential input voltage for the circuit presented in Fig. 2.51 can be expressed as follows:

$$V_1 - V_2 = \sqrt{\frac{2}{K}}(\sqrt{I} - \sqrt{I_O}) \quad (2.208)$$

resulting:

$$I = I_O + \frac{K}{2}(V_1 - V_2)^2 + \sqrt{2KI_O}(V_1 - V_2) \quad (2.209)$$

In order to obtain the multiplying function, four differential amplifiers from Fig. 2.51 can be connected as it is shown in Fig. 2.52.

The output current of the multiplier circuit will have the following expression:

$$I_{OUT} = I_1 + I_2 - I_3 - I_4 \quad (2.210)$$

resulting:

$$\begin{aligned} I_{OUT} &= \frac{K}{2}(-V_1 - V_2)^2 + \frac{K}{2}(V_1 + V_2)^2 \\ &- \frac{K}{2}(-V_1 + V_2)^2 - \frac{K}{2}(V_1 - V_2)^2 = 4KV_1V_2 \end{aligned} \quad (2.211)$$

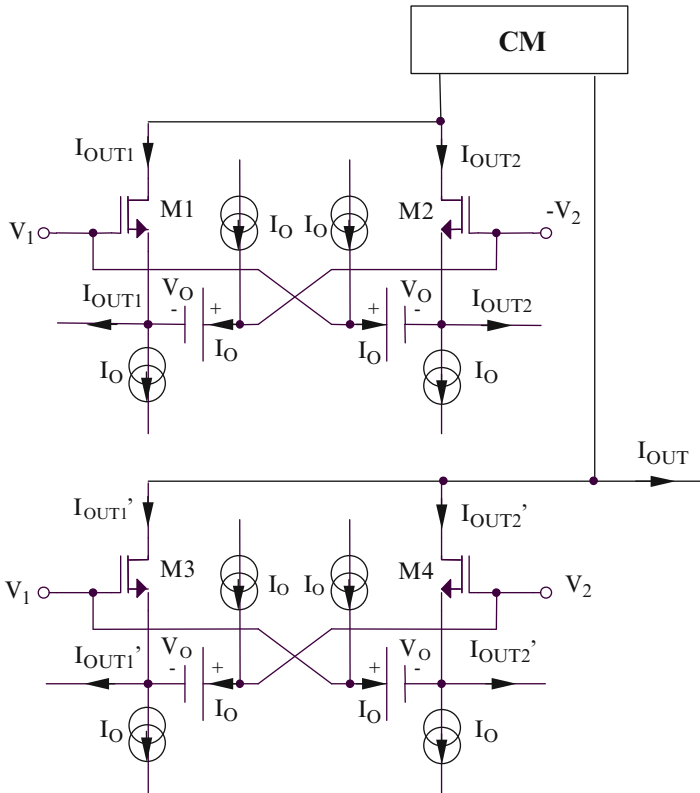


Fig. 2.48 Multiplier circuit (2) based on PR 2.7 – principle implementation

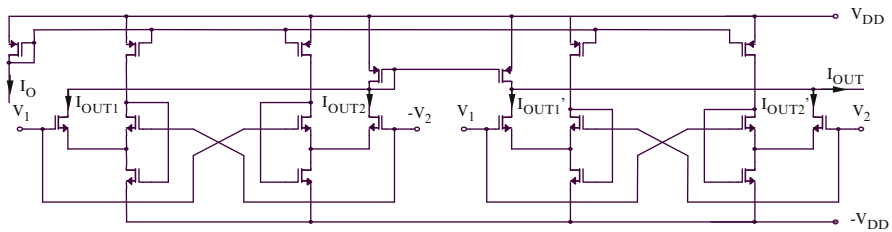
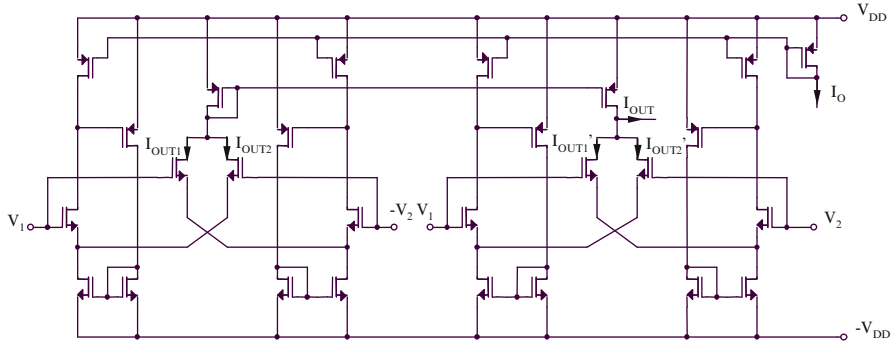


Fig. 2.49 Multiplier circuit (2) based on PR 2.7 – first implementation

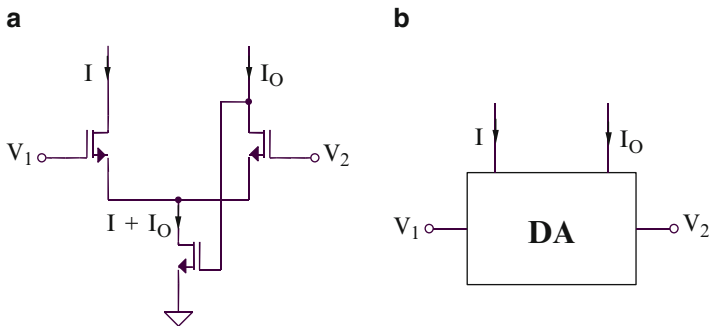
The circuit presented in Fig. 2.53 [12] represents a four-quadrant multiplier with balanced inputs.

The difference between the gate-source voltages of M1 and M3 transistors can be expressed as follows:

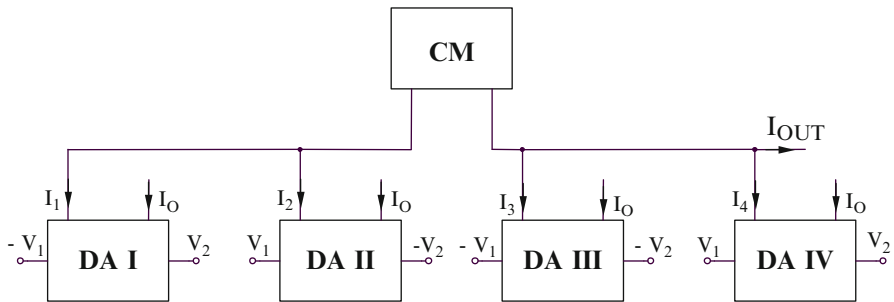
$$V_1 - V_2 = V_{GS1} - V_{GS3} \quad (2.212)$$



**Fig. 2.50** Multiplier circuit (2) based on PR 2.7 – second implementation



**Fig. 2.51** Multiplier circuit (3) based on PR 2.7 – circuit core



**Fig. 2.52** Multiplier circuit (3) based on PR 2.7 – block diagram

For a biasing in saturation of all MOS transistors from Fig. 2.53, it results:

$$V_1 - V_2 = \sqrt{\frac{2}{K}} (\sqrt{I_1} - \sqrt{I_O}) \quad (2.213)$$

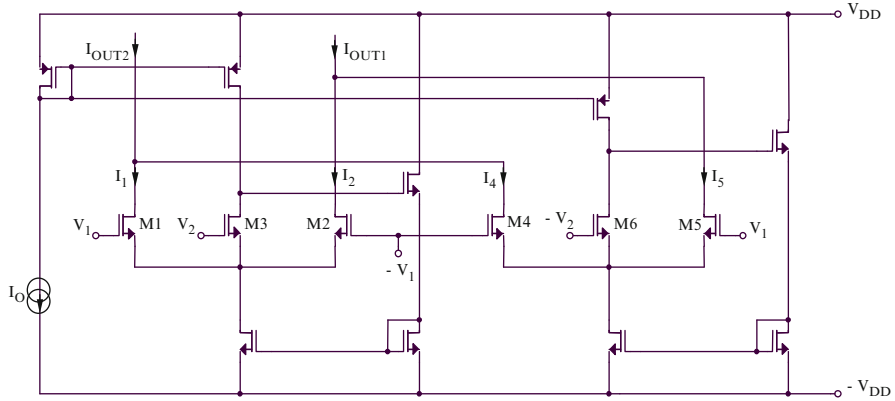


Fig. 2.53 Multiplier circuit (4) based on PR 2.7

So, the expression of  $I_1$  current will be:

$$I_1 = I_O + \frac{K}{2}(V_1 - V_2)^2 + \sqrt{2KI_O}(V_1 - V_2) \quad (2.214)$$

Similarly, computing the difference between the gate-source voltages of M2–M3 transistors, it results:

$$I_2 = I_O + \frac{K}{2}(-V_1 - V_2)^2 + \sqrt{2KI_O}(-V_1 - V_2) \quad (2.215)$$

The  $I_1 - I_2$  differential current will have the following expression:

$$I_1 - I_2 = 2V_1\sqrt{2KI_O} - 2KV_1V_2 \quad (2.216)$$

Similarly, for the structure implemented using M4–M6 transistors, the differential output current can be expressed as follows:

$$I_4 - I_5 = -2V_1\sqrt{2KI_O} - 2KV_1V_2 \quad (2.217)$$

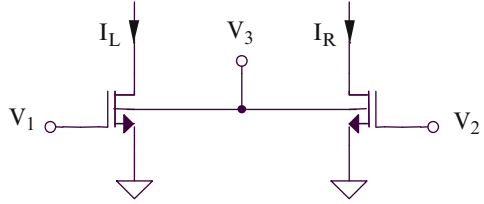
The differential output current for the entire multiplier structure presented in Fig. 2.53 will be:

$$I_{OUT} = I_{OUT1} - I_{OUT2} = I_2 + I_5 - I_1 - I_4 = 4KV_1V_2 \quad (2.218)$$

### 2.2.1.8 Multiplier Circuits Based on Different Mathematical Principles (PR 2.Da)

Alternate implementations of the previous presented multiplier circuits are based on different mathematical principles. The utilization of the bulk as an active terminal

**Fig. 2.54** Multiplier circuit  
(1) based on PR 2.Da – circuit core



gives the possibility of reducing the complexity of a multiplier circuit. The core of the following presented multiplier is presented in Fig. 2.54 [11].

A model of the MOS transistor biased in saturation that includes the dependence of the drain current on the bulk-source voltage is expressed by the following relation:

$$I_D = \frac{K}{2} (V_{GS} - V_T - AV_{BS} - BV_{BS}^2)^2 \quad (2.219)$$

$A$  and  $B$  being constants. The differential output current of the multiplier core from Fig. 2.54,  $I_L - I_R$ , will be:

$$I_L - I_R = \frac{K}{2} (V_1 - V_T - AV_3 - BV_3^2)^2 - \frac{K}{2} (V_2 - V_T - AV_3 - BV_3^2)^2 \quad (2.220)$$

resulting:

$$I_L - I_R = \frac{K}{2} (V_1 - V_2) (V_1 + V_2 - 2V_T - 2AV_3 - 2BV_3^2) \quad (2.221)$$

In order to obtain the multiplying function, two circuits from Fig. 2.54 can be cross-connected, resulting the multiplier presented in Fig. 2.55 [11].

For this circuit, the differential output current can be expressed as the difference between the differential output currents of each core:

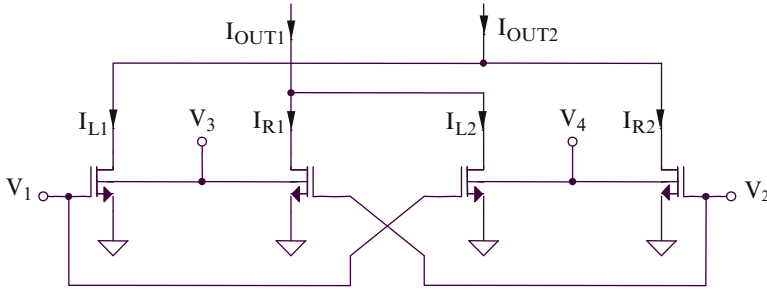
$$I_{OUT1} - I_{OUT2} = (I_{L2} + I_{R1}) - (I_{L1} + I_{R2}) = (I_{L2} - I_{R2}) - (I_{L1} - I_{R1}) \quad (2.222)$$

Replacing (2.221) in (2.222), it results:

$$\begin{aligned} I_{OUT1} - I_{OUT2} &= \frac{K}{2} (V_1 - V_2) (V_1 + V_2 - 2V_T - 2AV_4 - 2BV_4^2) \\ &\quad - \frac{K}{2} (V_1 - V_2) (V_1 + V_2 - 2V_T - 2AV_3 - 2BV_3^2) \end{aligned} \quad (2.223)$$

equivalent with:

$$\begin{aligned} I_{OUT1} - I_{OUT2} &= K(V_1 - V_2) [A(V_3 - V_4) + B(V_3^2 - V_4^2)] \\ &= K(V_1 - V_2)(V_3 - V_4)[A + B(V_3 + V_4)] \end{aligned} \quad (2.224)$$



**Fig. 2.55** Multiplier circuit (1) based on PR 2.Da – complete implementation

If the  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$  input voltages contain common-mode terms ( $V_{12}$  and  $V_{34}$ ) and differential-mode terms ( $v_{12}$  and  $v_{34}$ ) as follows:

$$V_1 = V_{12} + \frac{v_{12}}{2} \quad (2.225)$$

$$V_2 = V_{12} - \frac{v_{12}}{2} \quad (2.226)$$

$$V_3 = V_{34} + \frac{v_{34}}{2} \quad (2.227)$$

$$V_4 = V_{34} - \frac{v_{34}}{2} \quad (2.228)$$

it results:

$$I_{OUT1} - I_{OUT2} = K v_{12} v_{34} (A + 2B V_{34}) \quad (2.229)$$

so, the differential output current of the voltage multiplier presented in Fig. 2.55 will be proportional with the product of the differential-mode components of input voltages.

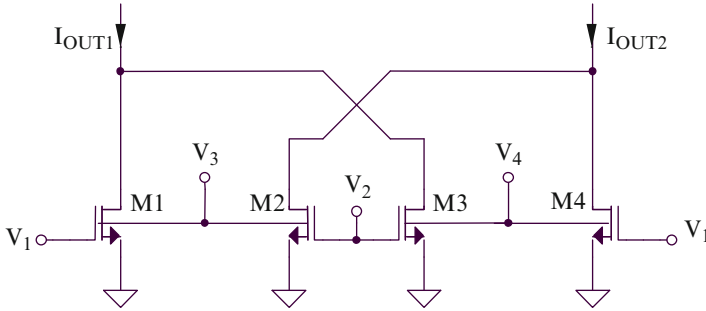
An alternate approach of a voltage multiplier, based on bulk-driven MOS devices using another model for the dependence of the threshold voltage  $V_T$  on the biasing of the bulk ( $V_{BS}$ ), is shown in Fig. 2.56 [26].

The differential output current of this multiplier can be expressed as follows:

$$I_{OUT1} - I_{OUT2} = (I_{D1} + I_{D3}) - (I_{D2} + I_{D4}) = (I_{D1} - I_{D2}) + (I_{D3} - I_{D4}) \quad (2.230)$$

where it is considered that the drain current of a MOS transistor depends on the gate-source voltage following a quadratic law (2.231) and on the bulk-source voltage as a consequence of the bulk effect using the mathematical relation (2.232):

$$I_D = \frac{K}{2} (V_{GS} - V_T)^2 \quad (2.231)$$



**Fig. 2.56** Multiplier circuit (2) based on PR 2.Da

$$V_T = V_{T0} + \gamma \left( \sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F} \right) \quad (2.232)$$

$V_T$  being the threshold voltage of the MOS transistor biased at a bulk-source voltage equal with  $V_{BS}$ ,  $\gamma$  is a model parameter and  $\Phi_F$  represents the Fermi potential. Replacing (2.232) in (2.231) and using the fact that  $V_{T1} = V_{T2}$  and  $V_{T3} = V_{T4}$  (because  $V_{BS1} = V_{BS2} = V_3$  and  $V_{BS3} = V_{BS4} = V_4$ ), it results the following expression of the output current:

$$I_{OUT1} - I_{OUT2} = \frac{K}{2} (V_1 - V_2) (V_1 + V_2 - 2V_{T1}) + \frac{K}{2} (V_2 - V_1) (V_1 + V_2 - 2V_{T3}) \quad (2.233)$$

so:

$$I_{OUT1} - I_{OUT2} = K(V_1 - V_2) (V_{T3} - V_{T1}) \quad (2.234)$$

Using the (2.232) relation that models the bulk effect, the previous expression of the output current can be rewritten as follows:

$$\begin{aligned} I_{OUT1} - I_{OUT2} &= K(V_1 - V_2) \gamma \left( \sqrt{2\Phi_F - V_4} - \sqrt{2\Phi_F - V_3} \right) \\ &= K(V_1 - V_2) \gamma \sqrt{2\Phi_F} \left( \sqrt{1 - \frac{V_4}{2\Phi_F}} - \sqrt{1 - \frac{V_3}{2\Phi_F}} \right) \end{aligned} \quad (2.235)$$

For  $V_3$  and  $V_4$  input signals much smaller than the Fermi potential, it is possible to use the first-order Taylor expansion  $\sqrt{1+x} \cong 1 + x/2$ , for  $x \ll 1$ , the expression of the output current becoming proportional with the product between the differential input voltages:

$$\begin{aligned} I_{OUT1} - I_{OUT2} &= K(V_1 - V_2) \gamma \sqrt{2\Phi_F} \left( \frac{V_3}{4\Phi_F} - \frac{V_4}{4\Phi_F} \right) \\ &= \frac{\gamma K}{2\sqrt{2\Phi_F}} (V_1 - V_2) (V_3 - V_4) \end{aligned} \quad (2.236)$$

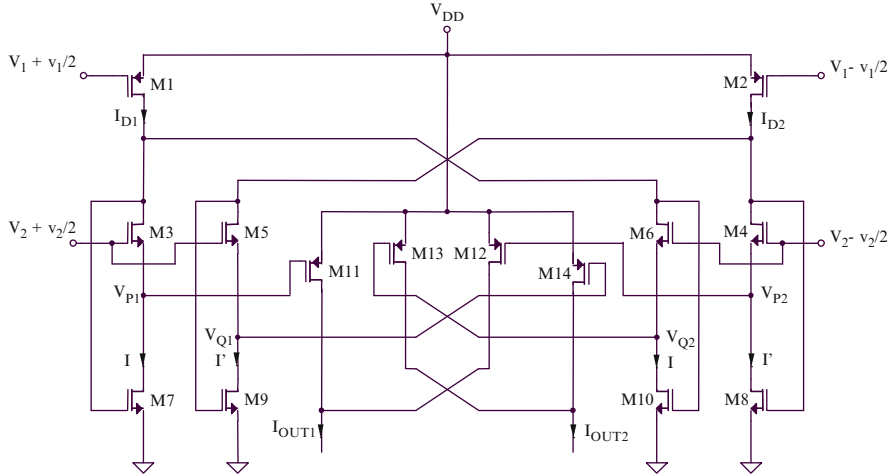


Fig. 2.57 Multiplier circuit (3) based on PR 2.Da

A symmetrical implementation of a voltage multiplier circuit is presented in Fig. 2.57 [27]. In order to improve the frequency response, all MOS transistors are biased in saturation region.

The differential output current of the voltage multiplier can be expressed as follows:

$$I_{OUT} = I_{OUT1} - I_{OUT2} = (I_{D11} + I_{D12}) - (I_{D13} + I_{D14}) \quad (2.237)$$

resulting:

$$I_{OUT} = \frac{K}{2}(V_{DD} - V_{P1} - V_T)^2 - \frac{K}{2}(V_{DD} - V_{Q1} - V_T)^2 + \frac{K}{2}(V_{DD} - V_{P2} - V_T)^2 - \frac{K}{2}(V_{DD} - V_{Q2} - V_T)^2 \quad (2.238)$$

or:

$$I_{OUT} = \frac{K}{2}(V_{Q2} - V_{P1})(2V_{DD} - V_{P1} - V_{Q2} - 2V_T) + \frac{K}{2}(V_{Q1} - V_{P2})(2V_{DD} - V_{P2} - V_{Q1} - 2V_T) \quad (2.239)$$

As a result of the connections between circuit transistors, the gate-source voltages of M7 and M10 transistors are equal. Additionally, because the same current  $I$  is passing through M3, M6, M7 and M10 transistors, all their gate-source voltages will be also equal. The identity  $V_{GS3} = V_{GS6}$  can be written as:

$$V_2 + \frac{v_2}{2} - V_{P1} = V_2 - \frac{v_2}{2} - V_{Q2} \quad (2.240)$$

It results:

$$V_{P1} - V_{Q2} = v_2 \quad (2.241)$$

and, similarly:

$$V_{Q1} - V_{P2} = v_2 \quad (2.242)$$

Replacing (2.241) and (2.242) in (2.239), the expression of the output current becomes:

$$I_{OUT} = \frac{K}{2} v_2 (V_{P1} - V_{P2} + V_{Q2} - V_{Q1}) \quad (2.243)$$

For evaluating the linear expression  $V_{P1} - V_{P2} + V_{Q2} - V_{Q1}$ , it is necessary to consider the squaring dependence of the drain current on the gate-source voltage for M3 and M5 transistors:

$$I = \frac{K}{2} (V_{GS3} - V_T)^2 = \frac{K}{2} \left( V_2 + \frac{v_2}{2} - V_{P1} - V_T \right)^2 \quad (2.244)$$

and:

$$I' = \frac{K}{2} (V_{GS5} - V_T)^2 = \frac{K}{2} \left( V_2 + \frac{v_2}{2} - V_{Q1} - V_T \right)^2 \quad (2.245)$$

resulting:

$$V_2 + \frac{v_2}{2} - V_{P1} - V_T = \sqrt{\frac{2I}{K}} \quad (2.246)$$

and:

$$V_2 + \frac{v_2}{2} - V_{Q1} - V_T = \sqrt{\frac{2I'}{K}} \quad (2.247)$$

Summing (2.246) and (2.247), it results:

$$2V_2 + v_2 - V_{P1} - V_{Q1} - 2V_T = \sqrt{\frac{2}{K}} (\sqrt{I} + \sqrt{I'}) \quad (2.248)$$

A similar analysis for M4 and M6 transistors will conclude to:

$$2V_2 - v_2 - V_{P2} - V_{Q2} - 2V_T = \sqrt{\frac{2}{K}} (\sqrt{I} + \sqrt{I'}) \quad (2.249)$$

Because  $I_{D1} = I_{D3} + I_{D6}$  and  $I_{D3} = I_{D6} = I$ , it results  $I_{D1} = 2I$  and, similarly,  $I_{D2} = 2I'$ . So:

$$\sqrt{\frac{2}{K}}(\sqrt{I} + \sqrt{I'}) = \sqrt{\frac{1}{K}}(\sqrt{I_{D1}} + \sqrt{I_{D2}}) = \sqrt{\frac{1}{K}}\sqrt{\frac{K}{2}}(V_{SG1} + V_{SG2} - 2V_T) \quad (2.250)$$

The source-gate voltages of M1 and M2 transistors can be expressed as  $V_{SG1} = V_{DD} - V_1 - v_1/2$ , and  $V_{SG2} = V_{DD} - V_1 + v_1/2$ , so:

$$\sqrt{\frac{2}{K}}(\sqrt{I} + \sqrt{I'}) = \sqrt{2}(V_{DD} - V_1 - V_T) \quad (2.251)$$

Replacing (2.251) in (2.248) and (2.249), it results:

$$\begin{aligned} 2V_2 + v_2 - V_{P1} - V_{Q1} - 2V_T &= 2V_2 - v_2 - V_{P2} - V_{Q2} - 2V_T \\ &= \sqrt{2}(V_{DD} - V_1 - V_T) \end{aligned} \quad (2.252)$$

The M1 and M2 transistors form a differential amplifier, its differential output current having the following expression:

$$\begin{aligned} I_{D1} - I_{D2} &= \frac{K}{2} \left( V_{DD} - V_1 - \frac{v_1}{2} - V_T \right)^2 - \frac{K}{2} \left( V_{DD} - V_1 + \frac{v_1}{2} - V_T \right)^2 \\ &= -Kv_1(V_{DD} - V_1 - V_T) \end{aligned} \quad (2.253)$$

As function on  $V_2$  and  $v_2$  input voltages,  $I_{D1}$  and  $I_{D2}$  currents could be expressed as follows:

$$I_{D1} = I_{D3} + I_{D6} = \frac{K}{2} \left( V_2 + \frac{v_2}{2} - V_{P1} - V_T \right)^2 + \frac{K}{2} \left( V_2 - \frac{v_2}{2} - V_{Q2} - V_T \right)^2 \quad (2.254)$$

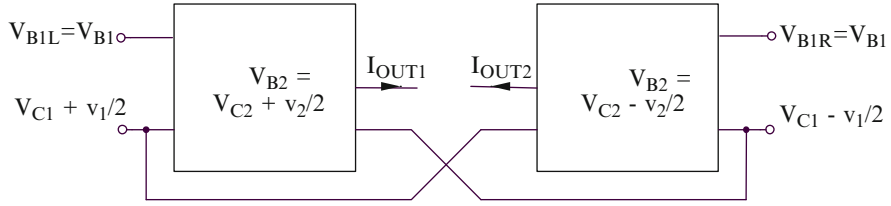
and:

$$I_{D2} = I_{D4} + I_{D5} = \frac{K}{2} \left( V_2 - \frac{v_2}{2} - V_{P2} - V_T \right)^2 + \frac{K}{2} \left( V_2 + \frac{v_2}{2} - V_{Q1} - V_T \right)^2 \quad (2.255)$$

resulting:

$$\begin{aligned} I_{D1} - I_{D2} &= \frac{K}{2} (V_{Q1} - V_{P1}) (2V_2 + v_2 - V_{P1} - V_{Q1} - 2V_T) \\ &\quad + \frac{K}{2} (V_{P2} - V_{Q2}) (2V_2 - v_2 - V_{P2} - V_{Q2} - 2V_T) \end{aligned} \quad (2.256)$$





**Fig. 2.59** Multiplier circuit (4) based on PR 2.Da – block diagram

As M3a and M5a and, respectively, M4a and M6a transistors are identical and biased at the same drain current, their gate-source voltages are equal,  $V_{GS3a} = V_{GS5a}$  and  $V_{SG4a} = V_{SG6a}$ , so:

$$\begin{aligned} V_{DS1} = V_{SG5a} - V_{SG6a} &= (V_{DD} - V_{B1}) - (V_{DD} - V_{B2}) \\ &= V_{B2} - V_{B1} = V_{C2} + \frac{v_2}{2} - V_{B1} \end{aligned} \quad (2.262)$$

From (2.260), (2.261) and (2.262), it results the following expression of the output current for the circuit presented in Fig. 2.58:

$$I_{OUT1} = K(V_{GS1a} - V_{GS1b})V_{DS1} = Kv_1V_{DS1} = Kv_1\left(V_{C2} + \frac{v_2}{2} - V_{B1}\right) \quad (2.263)$$

because  $V_{GS1a} = V_{C1} + v_1/2$ ,  $V_{GS1b} = V_{C1} - v_1/2$ .

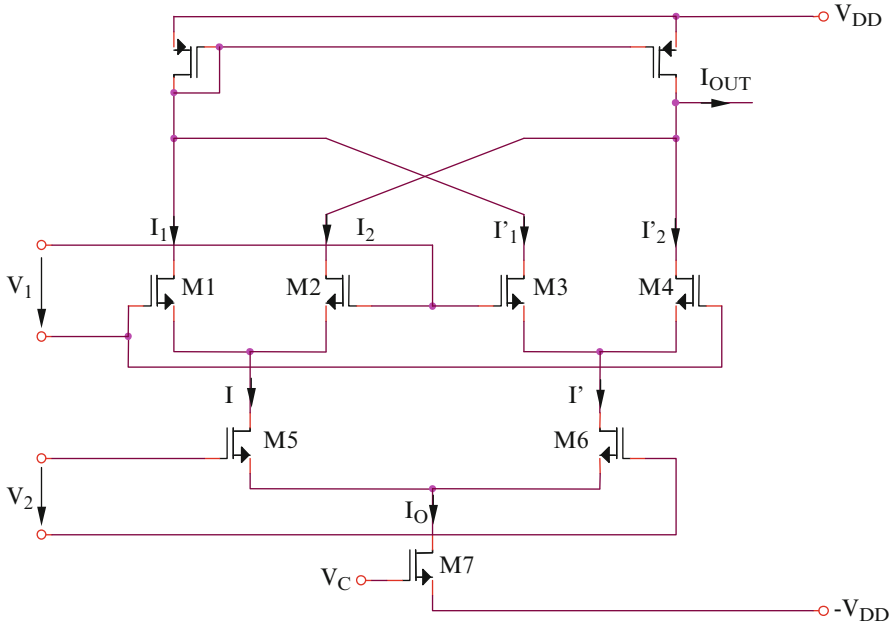
In order to obtain the multiplying function, two similar circuits from Fig. 2.58 must be used, the difference between them being the value of  $V_{B2}$  potential:  $V_{B2} = V_{C2} + v_2/2$  for the left structure from Fig. 2.59 [28] and  $V_{B2} = V_{C2} - v_2/2$  for the right structure.

The expression of the output current of the multiplier circuit presented in Fig. 2.59 will be:

$$I_{OUT1} - I_{OUT2} = Kv_1\left(V_{C2} + \frac{v_2}{2} - V_{B1}\right) - Kv_1\left(V_{C2} - \frac{v_2}{2} - V_{B1}\right) = Kv_1v_2 \quad (2.264)$$

Another possible realization of the voltage multiplier circuit is designed with the main goal of reducing the total harmonic distortions coefficient (THD).

Because of the quadratic characteristic of a MOS transistor biased in saturation, the linearity of the basic multiplier presented in Fig. 2.60 [29, 31] is rather poor. The core of this circuit is a modified Gilbert cell, extended to implement with good linearity the multiplication function.



**Fig. 2.60** Multiplier circuit (5) based on PR 2.Da

Considering a biasing in saturation of all transistors from Fig. 2.60, the expressions of the drain currents for M1–M4 transistors are:

$$I_{1,2} = \frac{I}{2} \left( 1 \pm \sqrt{\frac{KV_1^2}{I} - \frac{K^2 V_1^4}{4I^2}} \right); \quad I'_{2,1} = \frac{I'}{2} \left( 1 \pm \sqrt{\frac{KV_1^2}{I'} - \frac{K^2 V_1^4}{4(I')^2}} \right) \quad (2.265)$$

The output current expression is:

$$I_{OUT} = (I_1 - I_2) + (I'_1 - I'_2) = V_1 \left( \sqrt{KI - \frac{K^2}{4} V_1^4} - \sqrt{KI' - \frac{K^2}{4} V_1^4} \right) \quad (2.266)$$

Similarly, the drain currents of M5 and M6 transistors will have the following expressions:

$$I = \frac{I_O}{2} \left( 1 + \sqrt{\frac{KV_2^2}{I_O} - \frac{K^2 V_2^4}{4I_O^2}} \right) \quad (2.267)$$

$$I' = \frac{I_O}{2} \left( 1 - \sqrt{\frac{KV_2^2}{I_O} - \frac{K^2 V_2^4}{4I_O^2}} \right) \quad (2.268)$$

All transistors from Fig. 2.60 are supposed to be identical. Considering the limited expansion  $\sqrt{1+x} \cong 1+x/2$ , from the previous relations, it results the approximate expression of the basic multiplier output current:

$$I_{OUT} \cong \frac{K}{\sqrt{2}} V_1 V_2 - \frac{K^2}{8\sqrt{2}I_O} V_1 V_2^3 \quad (2.269)$$

Thus, the total harmonic distortions coefficient introduced by the circuit (approximated with the third-order one) will be expressed as:

$$THD_3 \cong \frac{KV_2^2}{8I_O} = \frac{1}{4} \left( \frac{V_2}{V_C + V_{DD} - V_T} \right)^2 \quad (2.270)$$

In conclusion,  $THD_3$  is directly proportional with the ratio between  $V_2$  input signal amplitude and the effective gate-source voltage of the biasing transistor.

In order to improve the circuit linearity, the modified multiplier presented in Fig. 2.61 [29] replaces the differential amplifier M5–M6 from Fig. 2.60 with a cross-connected one, M5–M8 from Fig. 2.61. The output current expression for the multiplier with improved linearity has the same form (2.266), but the expressions of  $I$  and  $I'$  currents become:

$$I = I_{p1} + I'_{p1} \quad (2.271)$$

$$I' = I_{p2} + I'_{p2} \quad (2.272)$$

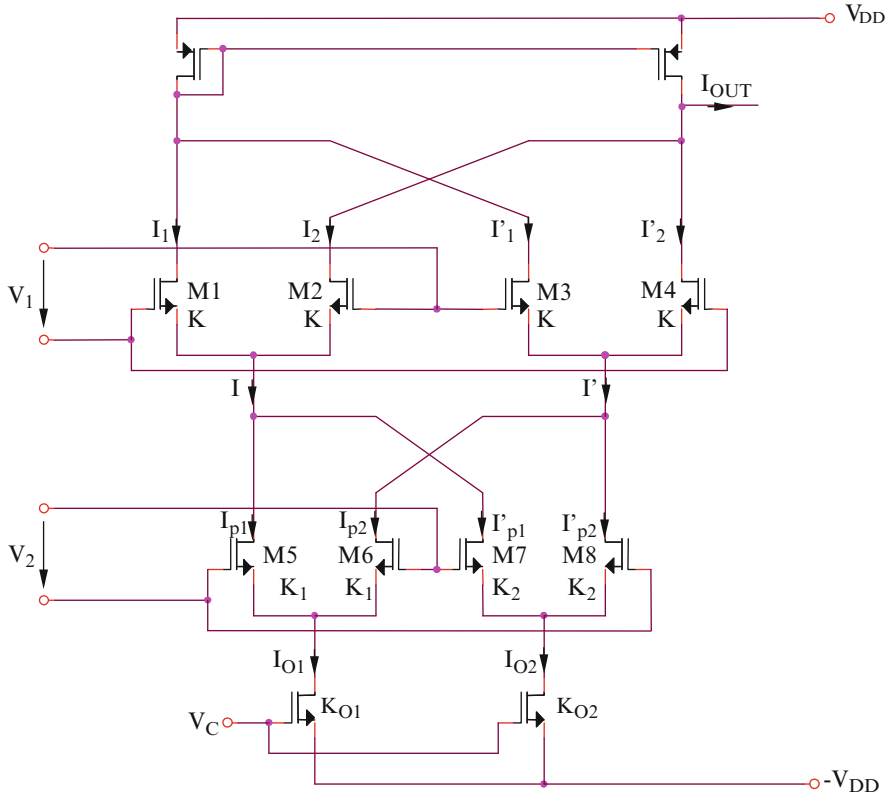
where:

$$I_{p1,2} = \frac{I_{O1}}{2} \left( 1 \pm \sqrt{\frac{K_1 V_2^2}{I_{O1}} - \frac{K_1^2 V_2^4}{4I_{O1}^2}} \right) \quad (2.273)$$

$$I'_{p1,2} = \frac{I_{O2}}{2} \left( 1 \mp \sqrt{\frac{K_2 V_2^2}{I_{O2}} - \frac{K_2^2 V_2^4}{4I_{O2}^2}} \right) \quad (2.274)$$

Similarly with the basic circuit analysis, considering the more accurate expansion  $\sqrt{1+x} \cong 1+x/2 - x^2/4$ , the output current of the multiplier from Fig. 2.61 will have the following expression:

$$I_{OUT} \cong V_1 \sqrt{\frac{K}{a}} (bV_2 + cV_2^3 + dV_2^5) \quad (2.275)$$



**Fig. 2.61** Multiplier circuit (6) based on PR 2.Da

where  $b$ ,  $c$  and  $d$  are constants, expressed as follows:

$$b = \frac{K_1^{1/2} I_{O1}^{1/2} - K_2^{1/2} I_{O2}^{1/2}}{2} \quad (2.276)$$

$$c = \frac{K_2^{3/2} I_{O2}^{-1/2} - K_1^{3/2} I_{O1}^{-1/2}}{16} \quad (2.277)$$

$$d = \frac{K_1^{5/2} I_{O1}^{-3/2} - K_2^{5/2} I_{O2}^{-3/2}}{128} \quad (2.278)$$

Because the main nonlinearity from the output current expression is caused by the third-order term of relation (2.242), the proposed linearization technique is

referring to the cancellation of the third-order distortions ( $c = 0$ ), equivalent with the following design condition:

$$\frac{I_{O2}}{I_{O1}} = \left(\frac{K_2}{K_1}\right)^3 \quad (2.279)$$

and, in consequence:

$$b = \frac{(K_1 I_{O1})^{1/2}}{2} \left[ 1 - \left(\frac{K_2}{K_1}\right)^2 \right] \quad (2.280)$$

$$d = \frac{K_1^{5/2} I_{O1}^{-3/2}}{128} \left[ 1 - \left(\frac{K_1}{K_2}\right)^2 \right] \quad (2.281)$$

The total harmonic distortions for the multiplier circuit with improved linearity (Fig. 2.61), approximated with the fifth-order one, will be:

$$THD_5 = \left(\frac{K_1^2}{8K_2 I_{O1}}\right)^2 V_2^4 = \left(\frac{K_1^2}{4K_2 K_{O1}}\right)^2 \left(\frac{V_2}{V_C + V_{DD} - V_T}\right)^4 \quad (2.282)$$

Considering the particular case that  $K_2 = K_{O1}$  and  $K_1/K_2 = 1/2$ , it results:

$$THD_5 = \frac{1}{256} \left(\frac{V_2}{V_C + V_{DD} - V_T}\right)^4 \quad (2.283)$$

Thus, the linearity improvement from the circuit presented in Fig. 2.61 with respect to the basic multiplier presented in Fig. 2.60 is about two orders of magnitude:

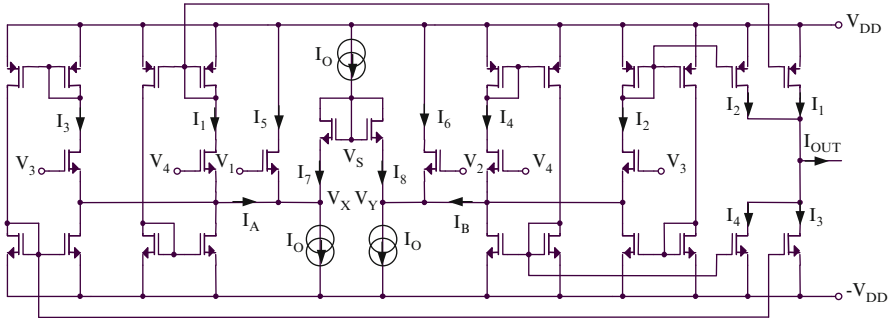
$$\frac{THD_3}{THD_5} = 64 \left(\frac{V_C + V_{DD} - V_T}{V_2}\right)^2 \quad (2.284)$$

For the multiplier circuit presented in Fig. 2.62 [32], the expression of the output current is:

$$I_{OUT} = I_1 + I_2 - I_3 - I_4 \quad (2.285)$$

or:

$$\begin{aligned} I_{OUT} = & \frac{K}{2} (V_4 - V_X - V_T)^2 + \frac{K}{2} (V_3 - V_Y - V_T)^2 \\ & - \frac{K}{2} (V_3 - V_X - V_T)^2 - \frac{K}{2} (V_4 - V_Y - V_T)^2 \end{aligned} \quad (2.286)$$



**Fig. 2.62** Multiplier circuit (7) based on PR 2.Da

resulting:

$$I_{OUT} = \frac{K}{2} (V_4 - V_3)(V_3 + V_4 - 2V_X - 2V_T) + \frac{K}{2} (V_3 - V_4)(V_3 + V_4 - 2V_Y - 2V_T) \quad (2.287)$$

So:

$$I_{OUT} = K(V_3 - V_4)(V_X - V_Y) \quad (2.288)$$

Because of the current mirrors from the circuit,  $I_A = I_B = 0$ , so between the currents from the circuit will exist the following linear relations:

$$I_7 + I_5 = I_O \quad (2.289)$$

$$I_7 + I_8 = I_O \quad (2.290)$$

and:

$$I_8 + I_6 = I_O \quad (2.291)$$

resulting  $I_5 = I_8$  and  $I_6 = I_7$ . So:

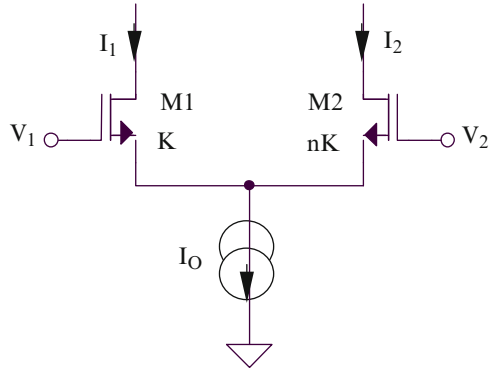
$$V_1 - V_X = V_S - V_Y \quad (2.292)$$

and:

$$V_2 - V_Y = V_S - V_X \quad (2.293)$$

equivalent with:

$$V_X - V_Y = V_1 - V_S \quad (2.294)$$

**Fig. 2.63** Asymmetrical differential structure

and:

$$V_X - V_Y = V_S - V_2 \quad (2.295)$$

It results:

$$V_S = \frac{V_1 + V_2}{2} \quad (2.296)$$

and:

$$V_X - V_Y = V_1 - \frac{V_1 + V_2}{2} = \frac{V_1 - V_2}{2} \quad (2.297)$$

Replacing (2.297) in (2.288), the output current will be proportional with the square of the differential input voltage:

$$I_{OUT} = \frac{K}{2} (V_1 - V_2) (V_3 - V_4) \quad (2.298)$$

A possible realization of a voltage multiplier circuit is based on a particular implementation of a voltage squaring circuit. The method for designing such a voltage squaring circuit uses a differential amplifier (Fig. 2.63) [17, 33] having a controllable asymmetry between the geometries of its two composing transistors. This difference between the aspect ratios of MOS transistors will introduce in the output currents of the differential amplifier a term proportional with the square of the differential input voltage.

Noting with  $V = V_1 - V_2$  the differential input voltage, it can be expressed as follows:

$$V = V_{GS1} - V_{GS2} = \sqrt{\frac{2I_1}{K}} - \sqrt{\frac{2(I_O - I_1)}{nK}} \quad (2.299)$$

resulting:

$$\frac{K}{2}V^2 = I_1 + \frac{I_O - I_1}{n} - 2\sqrt{\frac{I_1(I_O - I_1)}{n}} \quad (2.300)$$

The expression of the unknown current,  $I_1$ , can be obtained solving the following second-order equation, derived from (2.300):

$$I_1^2 \left[ \left( \frac{n-1}{n} \right)^2 + \frac{4}{n} \right] + I_1 \left[ 2\frac{n-1}{n} \left( \frac{I_O}{n} - \frac{KV^2}{2} \right) - \frac{4I_O}{n} \right] + \left( \frac{I_O}{n} - \frac{KV^2}{2} \right)^2 = 0 \quad (2.301)$$

So:

$$I_1 = \frac{I_O}{n+1} + \frac{n(n-1)}{2(n+1)^2}KV^2 + \frac{nV}{(n+1)^2} \sqrt{2KI_O(n+1) - K^2nV^2} \quad (2.302)$$

and:

$$I_2 = I_O - I_1 = \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2}KV^2 - \frac{nV}{(n+1)^2} \sqrt{2KI_O(n+1) - K^2nV^2} \quad (2.303)$$

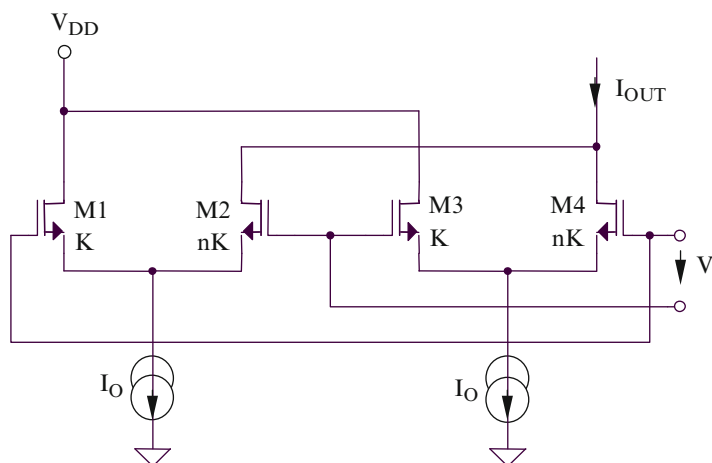
The complete realization of a voltage squaring circuit uses a cross-coupling of two differential amplifier having controllable asymmetries between their geometries, M1–M2 and M3–M4 (Fig. 2.64) [17, 33].

Using (2.302) and (2.303), it results:

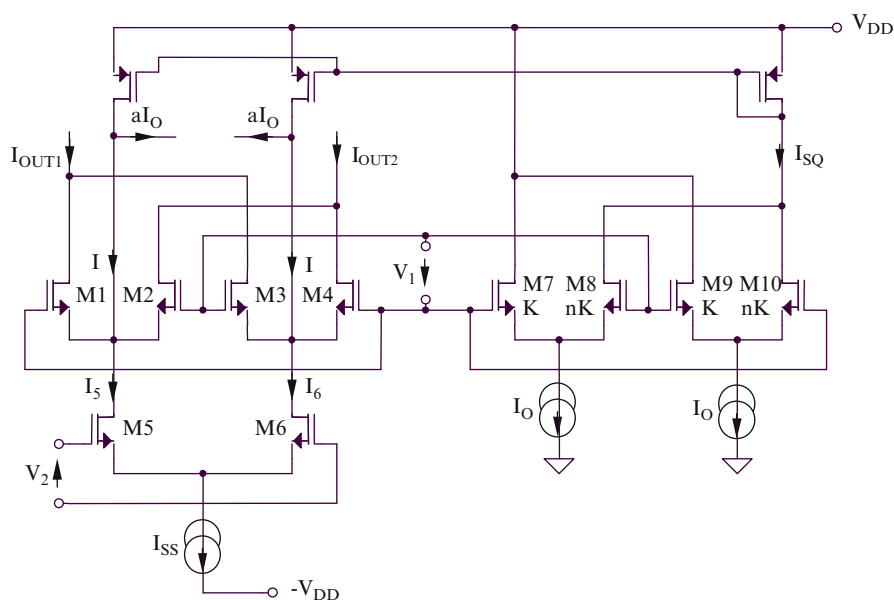
$$\begin{aligned} I_{OUT} = I_{D2} + I_{D4} &= \left[ \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2}KV^2 - \frac{nV}{(n+1)^2} \sqrt{2KI_O(n+1) - K^2nV^2} \right] \\ &+ \left[ \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2}KV^2 + \frac{nV}{(n+1)^2} \sqrt{2KI_O(n+1) - K^2nV^2} \right] \\ &= \frac{2nI_O}{n+1} - \frac{n(n-1)}{(n+1)^2}KV^2 \end{aligned} \quad (2.304)$$

An application of the previous presented voltage squarer circuit is represented by a voltage multiplier with linear characteristic (Fig. 2.65).

The method of designing the multiplying function is to use two cross-connected M1–M2 and M3–M4 differential amplifiers, each of them being biased at a drain



**Fig. 2.64** Voltage squaring circuit



**Fig. 2.65** Multiplier circuit (8) based on PR 2.Da

current equal with the difference between a drain current of another differential amplifier, M5–M6 ( $I_5$  and, respectively,  $I_6$ ) and a current,  $I$ , which must have a term proportional with the square of the first differential input voltage, in order to compensate the intrinsic nonlinearity of the differential amplifiers. Because M1–M4 transistors are identical, the dependencies of their drain currents on

$V_1$  differential input voltage, can be obtained particularizing relations (2.302) and (2.303) for  $n = 1$ :

$$I_{D1} = \frac{I_5 - I}{2} - \frac{KV_1}{4} \sqrt{\frac{4(I_5 - I)}{K} - V_1^2} \quad (2.305)$$

$$I_{D2} = \frac{I_5 - I}{2} + \frac{KV_1}{4} \sqrt{\frac{4(I_5 - I)}{K} - V_1^2} \quad (2.306)$$

$$I_{D3} = \frac{I_6 - I}{2} + \frac{KV_1}{4} \sqrt{\frac{4(I_6 - I)}{K} - V_1^2} \quad (2.307)$$

$$I_{D4} = \frac{I_6 - I}{2} - \frac{KV_1}{4} \sqrt{\frac{4(I_6 - I)}{K} - V_1^2} \quad (2.308)$$

The expression of the differential output current of the entire structure will be:

$$I_{OUT1} - I_{OUT2} = (I_{D1} + I_{D3}) - (I_{D2} + I_{D4}) = (I_{D1} - I_{D2}) - (I_{D4} - I_{D3}) \quad (2.309)$$

resulting:

$$I_{OUT1} - I_{OUT2} = -\frac{KV_1}{2} \sqrt{\frac{4(I_5 - I)}{K} - V_1^2} + \frac{KV_1}{2} \sqrt{\frac{4(I_6 - I)}{K} - V_1^2} \quad (2.310)$$

In order to cancel the nonlinear dependence of the differential output current on the differential input voltage, the  $I$  current must be proportional with the squaring of the differential input voltage:

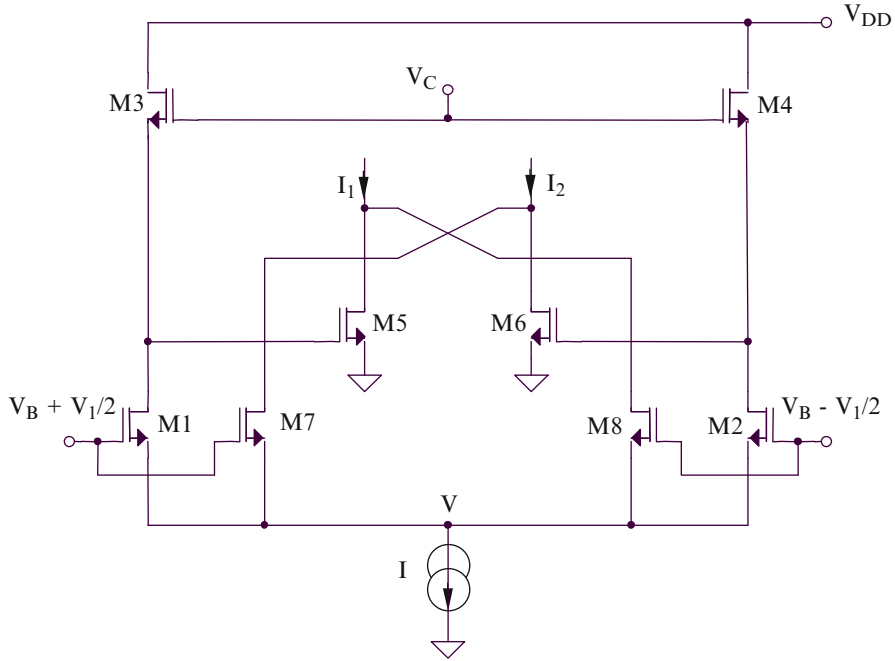
$$I = -\frac{K}{4} V_1^4 \quad (2.311)$$

For this particular current,  $I$ , the expression of the differential output current becomes:

$$I_{OUT1} - I_{OUT2} = \sqrt{K} V_1 (\sqrt{I_6} - \sqrt{I_5}) \quad (2.312)$$

Considering the squaring dependencies of the drain currents of M5–M6 differential amplifier on the gate-source voltages of their composing transistors, it results:

$$I_{OUT1} - I_{OUT2} = \sqrt{K} V_1 \left[ \sqrt{\frac{K}{2}} (V_{GS6} - V_{GS5}) \right] = \frac{1}{\sqrt{2}} K V_1 V_2 \quad (2.313)$$



**Fig. 2.66** Multiplier circuit (9) based on PR 2.Da – circuit core

So, the differential output current is proportional with the product between the input voltages. The implementation of the  $I$  current having the (2.311) expression is realized using M7–M10 transistors, representing a voltage squaring circuit, similar with the structure presented in Fig. 2.64. Comparing (2.304) with (2.311), it results the following condition that must be imposed to the constant  $n$ :

$$\frac{n(n-1)}{(n+1)^2} = \frac{1}{4} \quad (2.314)$$

So  $n = 2.15$  and:

$$I_{SQ} = 1.36I_O - \frac{K}{4}V_1^2 \quad (2.315)$$

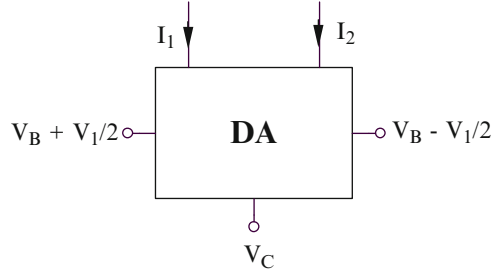
Because  $I = I_{SQ} - aI_O$ , the expression (2.311) of  $I$  current can be obtained for  $a = 1.36$ .

Another possible implementation of a multiplier circuit is based on the differential amplifier presented in Fig. 2.66 [34].

The expression of the first output current is:

$$I_1 = \frac{K}{2}(V_{GS5} - V_T)^2 + \frac{K}{2}(V_{GS8} - V_T)^2 \quad (2.316)$$

**Fig. 2.67** Multiplier circuit (9) based on PR 2.Da – symbolic representation of the circuit core



equivalently with:

$$I_1 = \frac{K}{2}(V_C - V_{GS3} - V_T)^2 + \frac{K}{2}(V_{GS8} - V_T)^2 \quad (2.317)$$

Because M1 and M3 transistors are identical and biased at the same drain current, their gate-source voltages will be equal, so:

$$I_1 = \frac{K}{2}(V_C - V_{GS1} - V_T)^2 + \frac{K}{2}(V_{GS8} - V_T)^2 \quad (2.318)$$

or:

$$I_1 = \frac{K}{2}\left(V_C - V_B + V - V_T - \frac{V_1}{2}\right)^2 + \frac{K}{2}\left(V_B - V - V_T - \frac{V_1}{2}\right)^2 \quad (2.319)$$

Similarly, the second output current,  $I_{OUT2}$ , will have the following expression:

$$I_2 = \frac{K}{2}\left(V_C - V_B + V - V_T + \frac{V_1}{2}\right)^2 + \frac{K}{2}\left(V_B - V - V_T + \frac{V_1}{2}\right)^2 \quad (2.320)$$

The differential output current can be expressed as follows:

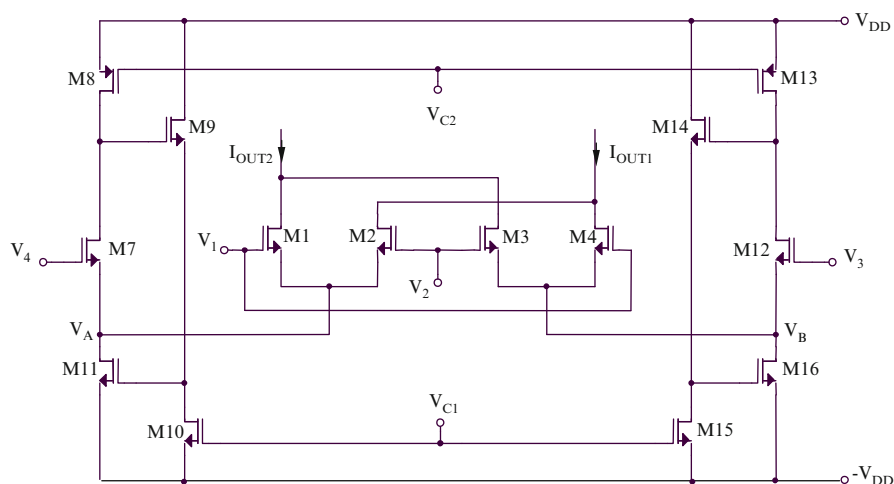
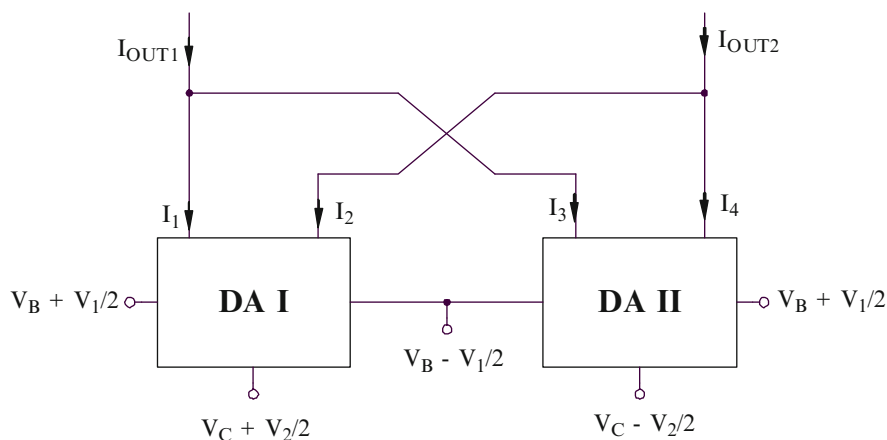
$$I_2 - I_1 = KV_1(V_C - V_B + V - V_T) + KV_1(V_B - V - V_T) = K(V_C - 2V_T)V_1 \quad (2.321)$$

The symbolic representation of the circuit is shown in Fig. 2.67.

A voltage multiplier can be realized using two previous presented differential amplifiers having the  $V_C$  voltage sources replaced by two voltages that are dependent on a second input voltage,  $V_2$ . The complete multiplier circuit is shown in Fig. 2.68.

The differential output current of the voltage multiplier presented in Fig. 2.68 can be expressed as follows:

$$I_{OUT1} - I_{OUT2} = (I_1 + I_3) - (I_2 + I_4) = (I_1 - I_2) + (I_3 - I_4) \quad (2.322)$$



**Fig. 2.69** Multiplier circuit (10) based on PR 2.Da

$$I_{OUT1} - I_{OUT2} = K \left[ \left( V_C + \frac{V_2}{2} \right) - 2V_T \right] V_1 + K \left[ \left( V_C - \frac{V_2}{2} \right) - 2V_T \right] (-V_1) = KV_1 V_2 \quad (2.323)$$

The differential output current of the structure is:

$$I_{OUT1} - I_{OUT2} = I_{D2} + I_{D4} - I_{D1} - I_{D3} \quad (2.324)$$

equivalent with:

$$\begin{aligned} I_{OUT1} - I_{OUT2} = & \frac{K}{2}(V_2 - V_A - V_T)^2 + \frac{K}{2}(V_1 - V_B - V_T)^2 \\ & - \frac{K}{2}(V_1 - V_A - V_T)^2 - \frac{K}{2}(V_2 - V_B - V_T)^2 \end{aligned} \quad (2.325)$$

So:

$$I_{OUT1} - I_{OUT2} = K(V_1 - V_2)(V_A - V_B) \quad (2.326)$$

The  $V_A - V_B$  differential voltage can be expressed as follows:

$$V_A - V_B = (V_4 - V_{GS7}) - (V_3 - V_{GS12}) = (V_4 - V_3) + (V_{GS12} - V_{GS7}) \quad (2.327)$$

Because  $I_{D7} = I_{D8}$  and  $I_{D12} = I_{D13}$ , it results  $V_{GS7} = V_{SG8}$  and  $V_{GS12} = V_{SG13}$ . So:

$$V_A - V_B = (V_4 - V_3) + (V_{SG13} - V_{SG8}) = V_4 - V_3 \quad (2.328)$$

Replacing (2.328) in (2.326), it results:

$$I_{OUT1} - I_{OUT2} = K(V_1 - V_2)(V_4 - V_3) \quad (2.329)$$

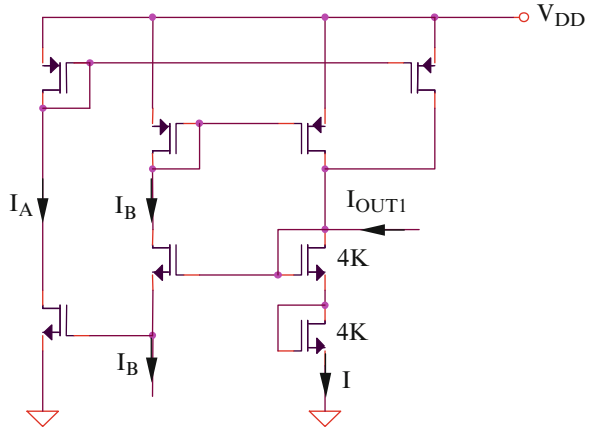
## 2.2.2 Design of Current Multiplier Circuits

Another class of multiplier circuits is represented by the current multipliers, the output current of these circuits being proportional with the product between two input currents. The current-mode operation of the multiplier circuits has the important advantage of increasing the frequency response of the designed structures.

### 2.2.2.1 Multiplier Circuits Based on the Ninth Mathematical Principle (PR 2.9)

A possibility of designing a current multiplier uses as circuit cores two current square-root circuits (Fig. 2.70) [36].

**Fig. 2.70** CMOS square-root circuit for the multiplier circuit (1) based on PR 2.9



For a biasing in saturation of all the MOS transistors from Fig. 2.70, it is possible to write that:

$$\left( V_T + \sqrt{\frac{2I_A}{K}} \right) + \left( V_T + \sqrt{\frac{2I_B}{K}} \right) = 2 \left( V_T + \sqrt{\frac{2I}{4K}} \right) \quad (2.330)$$

equivalent with:

$$I = I_A + I_B + 2\sqrt{I_A I_B} \quad (2.331)$$

Implementing the following linear relation between the previous current of the square-root circuit:

$$I_{OUT1} = I - I_A - I_B \quad (2.332)$$

the output current of the circuit from Fig. 2.70 will be proportional with the square-root of the input current:

$$I_{OUT1} = 2\sqrt{I_A I_B} \quad (2.333)$$

The multiplier circuit can be obtained using two square-root circuits from Fig. 2.70 connected as it is shown in Fig. 2.71. The computed functions are  $I_{OUT1} = 2\sqrt{I_{OUT} I_O}$  and  $I_{OUT2} = 2\sqrt{I_1 I_2}$ . Because  $I_{OUT1} = I_{OUT2}$ , the function implemented by the circuit from Fig. 2.71 [36] will be:

$$I_{OUT} = \frac{I_1 I_2}{I_O} \quad (2.334)$$

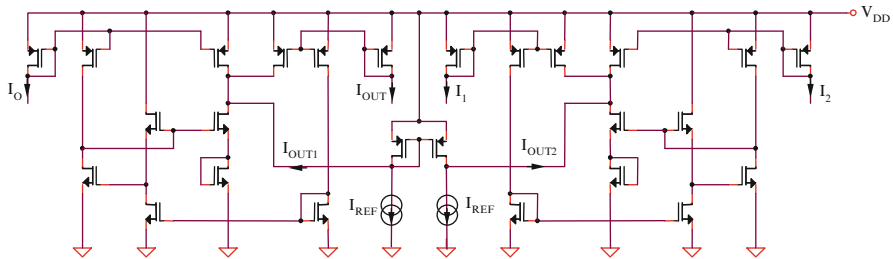


Fig. 2.71 Multiplier circuit (1) based on PR 2.9

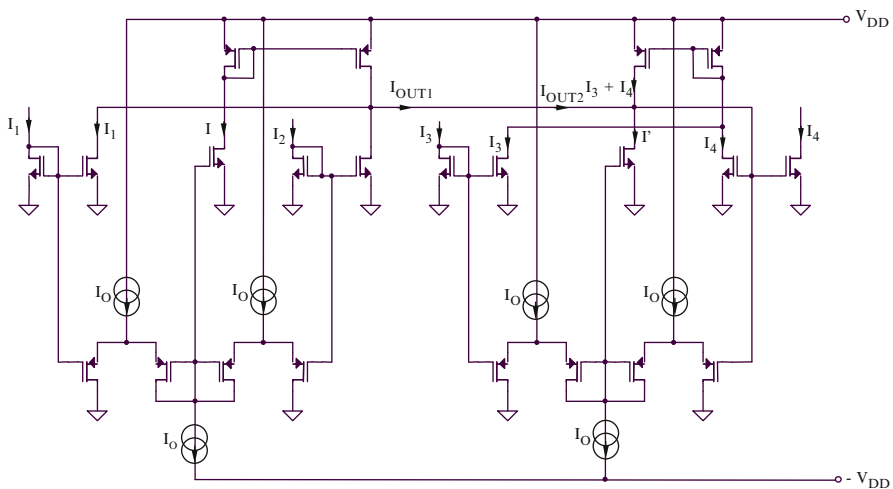


Fig. 2.72 Multiplier circuit (2) based on PR 2.9

The design of a multiplier/divider circuit can be done using two square-root circuits, as it is shown in Fig. 2.72 [37].

The square-root circuits have the implementation presented in Fig. 2. The output currents of these circuits have the following expressions:

$$I_{OUT1} = 2\sqrt{I_1 I_2} \quad (2.335)$$

and:

$$I_{OUT2} = 2\sqrt{I_3 I_4} \quad (2.336)$$

Imposing by design  $I_{OUT1} = I_{OUT2}$ , it results:

$$I_4 = \frac{I_1 I_2}{I_3} \quad (2.337)$$

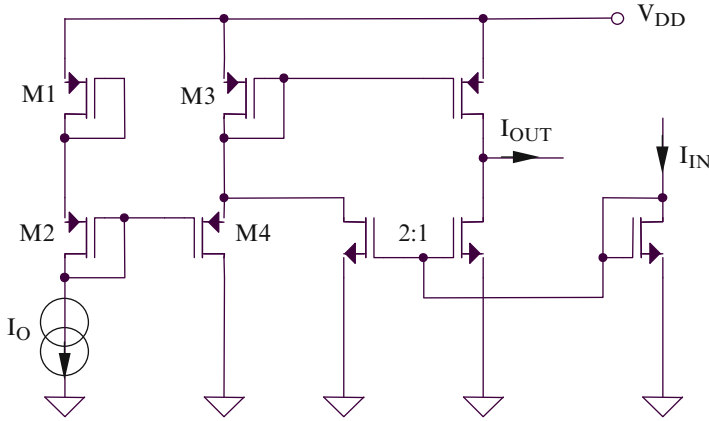


Fig. 2.73 CMOS squaring circuit for the multiplier circuit (1) based on PR 2.10

### 2.2.2.2 Multiplier circuits based on the tenth mathematical principle (PR 2.10)

The following multiplier structure (Fig. 2.74) is derived from the squaring circuit presented in Fig. 2.73 [38].

The characteristic equation of the translinear loop including M1–M4 transistors is:

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \quad (2.338)$$

resulting:

$$2\sqrt{I_{D1}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \quad (2.339)$$

equivalent with:

$$2\sqrt{I_O} = \sqrt{I_{OUT} + I_{IN}} + \sqrt{I_{OUT} - I_{IN}} \quad (2.340)$$

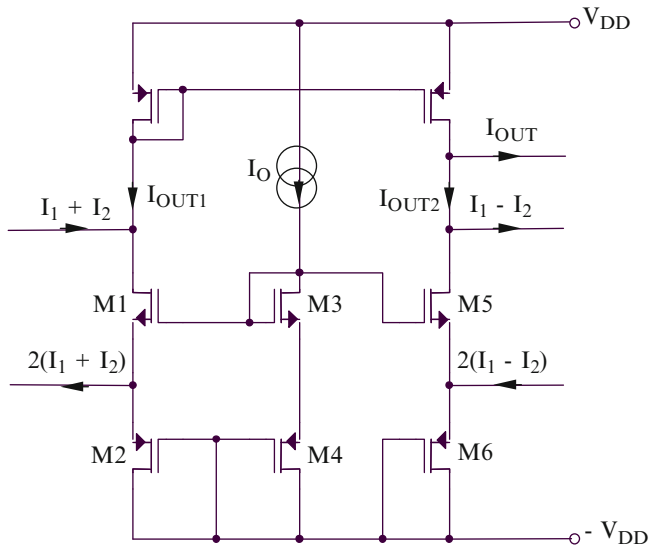
The expression of the output current will be:

$$I_{OUT} = I_O + \frac{I_{IN}^2}{4I_O} \quad (2.341)$$

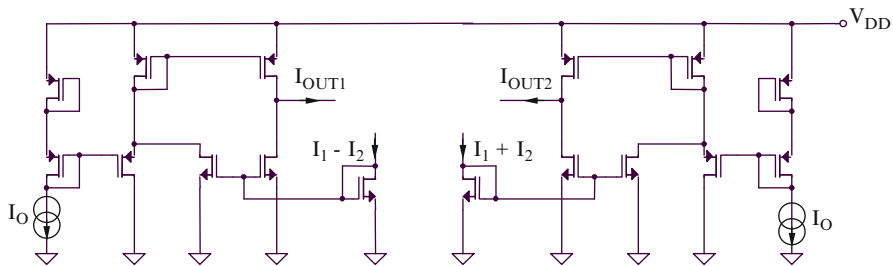
Using the squaring circuit presented in Fig. 2.73, it is possible to design a current multiplier structure (Fig. 2.74) [38].

The output current of the multiplier circuit can be expressed as follows:

$$I_{OUT} = I_{OUT2} - I_{OUT1} = \left[ I_O + \frac{(I_1 + I_2)^2}{4I_O} \right] - \left[ I_O - \frac{(I_1 + I_2)^2}{4I_O} \right] = \frac{I_1 I_2}{I_O} \quad (2.342)$$



**Fig. 2.75** Multiplier circuit (2) based on PR 2.10



**Fig. 2.74** Multiplier circuit (1) based on PR 2.10

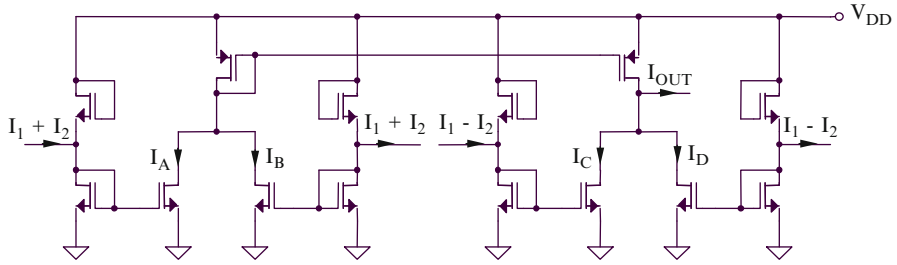
The multiplier/divider circuit presented in Fig. 2.75 [39] uses two translinear loops implemented with M1–M4 and M3–M6 transistors, respectively.

The characteristic equation of the first translinear loop is:

$$V_{GS3} + V_{SG4} = V_{GS1} + V_{SG2} \quad (2.343)$$

Considering a biasing in saturation of all MOS transistors from Fig. 2.75, it results:

$$2\sqrt{I_O} = \sqrt{I_{OUT1} + (I_1 + I_2)} + \sqrt{I_{OUT1} - (I_1 + I_2)} \quad (2.344)$$



**Fig. 2.76** Multiplier circuit (2) based on PR 2.10

The  $I_{OUT1}$  current will be expressed as follows:

$$I_{OUT1} = I_O + \frac{(I_1 + I_2)^2}{4I_O} \quad (2.345)$$

Similarly, analyzing the characteristic equation for the second translinear loop, it results:

$$2\sqrt{I_O} = \sqrt{I_{OUT1} + (I_1 - I_2)} + \sqrt{I_{OUT1} - (I_1 - I_2)} \quad (2.346)$$

So, the expression of  $I_{OUT2}$  current will be:

$$I_{OUT2} = I_O + \frac{(I_1 - I_2)^2}{4I_O} \quad (2.347)$$

The output current of the multiplier/divider circuit presented in Fig. 2.75 will have the following expression:

$$I_{OUT} = I_{OUT1} - I_{OUT2} = \frac{I_1 I_2}{I_O} \quad (2.348)$$

The most important advantage of the multiplier is the independence of the circuit performances on technological errors.

A current multiplier circuit (Fig. 2.76) [40] can be designed using four current squaring circuits.

Because:

$$V_{DD} = V_{GS}(I_A) + V_{GS}(I_A - I_1 - I_2) \quad (2.349)$$

it results:

$$\sqrt{I_A} + \sqrt{I_A - (I_1 + I_2)} = \sqrt{\frac{K}{2}}(V_{DD} - 2V_T) \quad (2.350)$$

Thus,  $I_A$  current can be expressed as follows:

$$I_A = \frac{I_1 + I_2}{2} + \frac{K(V_{DD} - 2V_T)^2}{8} + \frac{(I_1 + I_2)^2}{2K(V_{DD} - 2V_T)^2} \quad (2.351)$$

Similarly:

$$I_B = -\frac{I_1 + I_2}{2} + \frac{K(V_{DD} - 2V_T)^2}{8} + \frac{(I_1 + I_2)^2}{2K(V_{DD} - 2V_T)^2} \quad (2.352)$$

$$I_C = \frac{I_1 - I_2}{2} + \frac{K(V_{DD} - 2V_T)^2}{8} + \frac{(I_1 - I_2)^2}{2K(V_{DD} - 2V_T)^2} \quad (2.353)$$

$$I_D = -\frac{I_1 - I_2}{2} + \frac{K(V_{DD} - 2V_T)^2}{8} + \frac{(I_1 - I_2)^2}{2K(V_{DD} - 2V_T)^2} \quad (2.354)$$

The output current of the multiplier circuit presented in Fig. 2.76 will have the following expression:

$$I_{OUT} = I_A + I_B - I_C - I_D = \frac{4I_1I_2}{K(V_{DD} - 2V_T)^2} \quad (2.355)$$

Comparing with the previous circuit, the operation of this multiplier structure is affected by technological errors (both  $K$  and  $V_T$  technological parameters appear in the expression of the output current).

The current multiplier circuit presented in Fig. 2.77 [41] contains two current squaring circuits.

The expressions of the output current for these circuits are:

$$I_{OUT1} = 2I_O + \frac{(I_1 + I_2)^2}{8I_O} \quad (2.356)$$

and:

$$I_{OUT2} = 2I_O + \frac{(I_1 - I_2)^2}{8I_O} \quad (2.357)$$

The output current of the multiplier circuit presented in Fig. 2.77 will have the following expression:

$$I_{OUT} = I_{OUT1} - I_{OUT2} = \frac{I_1I_2}{2I_O} \quad (2.358)$$

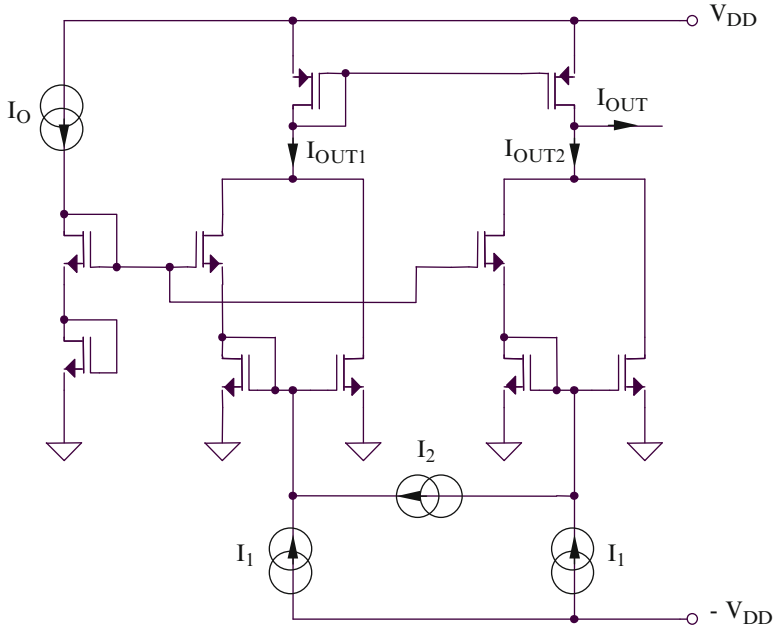


Fig. 2.77 Multiplier circuit (4) based on PR 2.10

### 2.2.2.3 Multiplier Circuits Based on the Eleventh Mathematical Principle (PR 2.11)

The following multiplier structures are designed for low-power applications, the reducing of their current consumptions being obtained by a biasing in weak inversion of all MOS active devices.

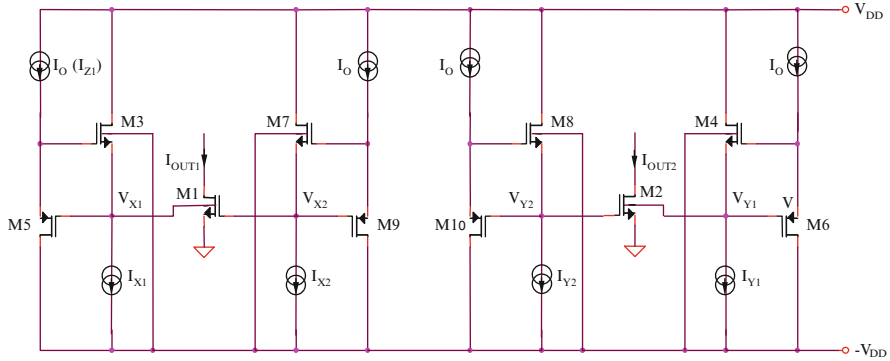
A current multiplier/divider using bulk-driven subthreshold-operated MOS transistors is presented in Fig. 2.78 [42, 43]. The double drive of the MOS devices (on gate and on bulk) allows the reduction of the computational circuit complexity. Unfortunately, the possibility of implementation in silicon is limited to CMOS technologies with independent wells. Imposing a weak inversion of all MOS transistors from Fig. 2.78, it is possible to write:

$$I_{OUT1} = I_{DO} \exp\left(\frac{V_{GS1} + (n-1)V_{BS1}}{nV_{th}}\right) \quad (2.359)$$

$$I_{OUT2} = I_{DO} \exp\left(\frac{V_{GS2} + (n-1)V_{BS2}}{nV_{th}}\right) \quad (2.360)$$

So:

$$\frac{I_{OUT1}}{I_{OUT2}} = \exp\left(\frac{V_{X2} - V_{Y2}}{nV_{th}}\right) \exp\left[\frac{n-1}{nV_{th}}(V_{X1} - V_{Y1})\right] \quad (2.361)$$



**Fig. 2.78** Multiplier circuit (1) based on PR 2.11

Because  $V_{GS3} = V_{GS5}$  and  $V_{GS4} = V_{GS6}$ , where  $V_{GS5} = V_{GS6} = V_T + \sqrt{2I_O/K}$  it results  $V_{GS3} = V_{GS4}$ , so:

$$\frac{I_{X1}}{I_{Y1}} = \exp \left[ \frac{n-1}{nV_{th}} (V_{BS3} - V_{BS4}) \right] \quad (2.362)$$

Similarly, because  $V_{GS7} = V_{GS8}$ , it results:

$$\frac{I_{X2}}{I_{Y2}} = \exp \left[ \frac{n-1}{nV_{th}} (V_{BS7} - V_{BS8}) \right] \quad (2.363)$$

Knowing that  $V_{X1} - V_{Y1} = V_{BS4} - V_{BS3}$ ,  $V_{X2} - V_{Y2} = V_{BS8} - V_{BS7}$  and using (2.361) and (2.362), it can write that:

$$\frac{I_{OUT1}}{I_{OUT2}} = \frac{I_{Y1}}{I_{X1}} \left( \frac{I_{Y2}}{I_{X2}} \right)^{\frac{1}{n-1}} \quad (2.364)$$

A generalization of (2.364) relation for different values of  $I_O$  current sources ( $I_{Z1}$ ,  $I_{W1}$  and  $I_{Z2}$ ,  $I_{W2}$ , respectively) allows to obtain a more complex relation between the circuit currents:

$$\frac{I_{OUT1}}{I_{OUT2}} = \frac{I_{Y1}}{I_{X1}} \frac{I_{Z1}}{I_{W1}} \left( \frac{I_{Y2}}{I_{X2}} \frac{I_{Z2}}{I_{W2}} \right)^{\frac{1}{n-1}} \quad (2.365)$$

Another implementation of a current-mode multiplier/divider is referred to a bulk-driven active-load differential amplifier from Fig. 2.79 [42]. Considering a weak inversion operation of all transistors from Fig. 2.79, the ratio of  $I_1$  and  $I_2$  currents will be:

$$\frac{I_{OUT1}}{I_{OUT2}} = \exp \left( \frac{V_{GS1} - V_{GS2}}{nV_{th}} \right) \quad (2.366)$$

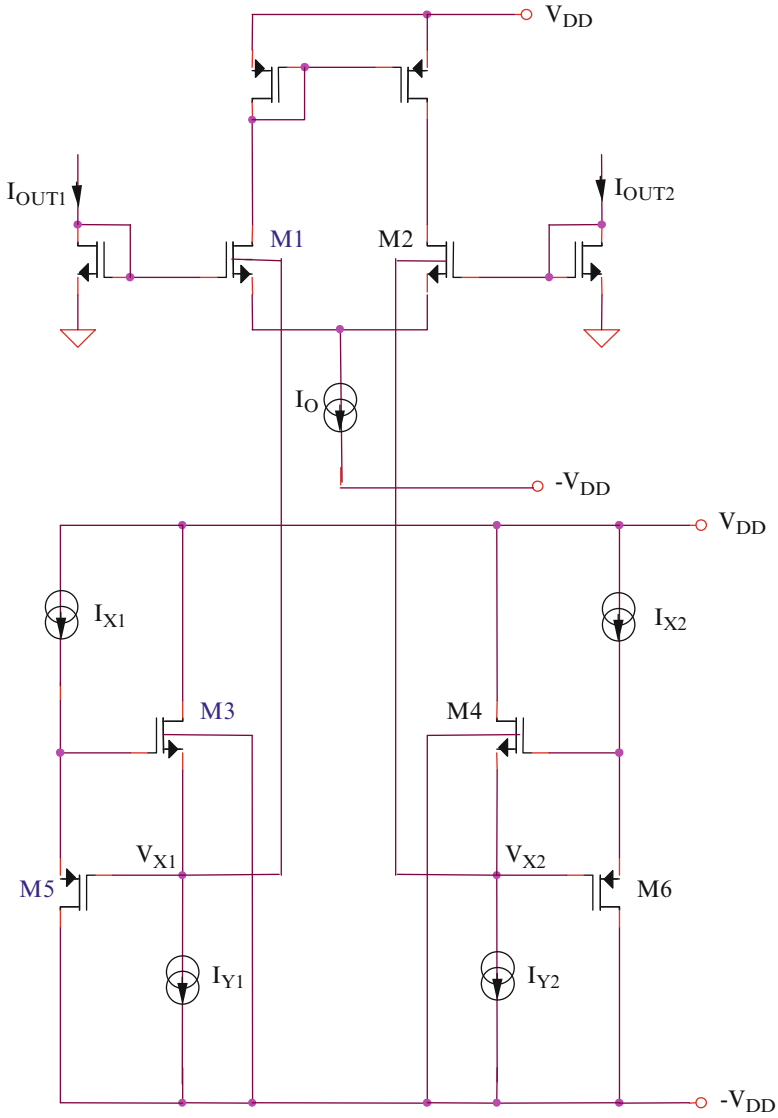


Fig. 2.79 Multiplier circuit (2) based on PR 2.11

For the active-load differential amplifier, it can write:

$$\frac{I_{D1}}{I_{D2}} = 1 = \exp\left(\frac{V_{GS1} - V_{GS2}}{nV_{th}}\right) \exp\left[\frac{n-1}{nV_{th}}(V_{BS1} - V_{BS2})\right] \quad (2.367)$$

From the two previous relations, it results:

$$\frac{I_{OUT1}}{I_{OUT2}} = \exp \left[ \frac{1-n}{nV_{th}} (V_{X1} - V_{X2}) \right] \quad (2.368)$$

Similarly, the ratios of  $I_{X1}$ ,  $I_{X2}$  and  $I_{Y1}$ ,  $I_{Y2}$  are, respectively:

$$\frac{I_{X1}}{I_{X2}} = \exp \left( \frac{V_{SG6} - V_{SG5}}{nV_{th}} \right) = \exp \left( \frac{V_{GS3} - V_{GS4}}{nV_{th}} \right) \quad (2.369)$$

and:

$$\frac{I_{Y1}}{I_{Y2}} = \exp \left( \frac{V_{GS3} - V_{GS4}}{nV_{th}} \right) \exp \left[ \frac{n-1}{nV_{th}} (V_{BS3} - V_{BS4}) \right] \quad (2.370)$$

So:

$$V_{BS3} - V_{BS4} = \frac{nV_{th}}{n-1} \ln \left( \frac{I_{Y1}}{I_{Y2}} \frac{I_{X2}}{I_{X1}} \right) \quad (2.371)$$

From (2.368) and (2.371), using that  $V_{X1} - V_{X2} = V_{BS4} - V_{BS3}$ , the relation between the currents from Fig. 2.79 will be:

$$\frac{I_{OUT1}}{I_{OUT2}} = \frac{I_{Y1}}{I_{Y2}} \frac{I_{X2}}{I_{X1}} \quad (2.372)$$

The current multiplier circuit presented in Fig. 2.80 [44–46] uses MOS transistors biased in weak inversion region. The translinear loop containing M1–M4 transistors has the following characteristic equation:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \quad (2.373)$$

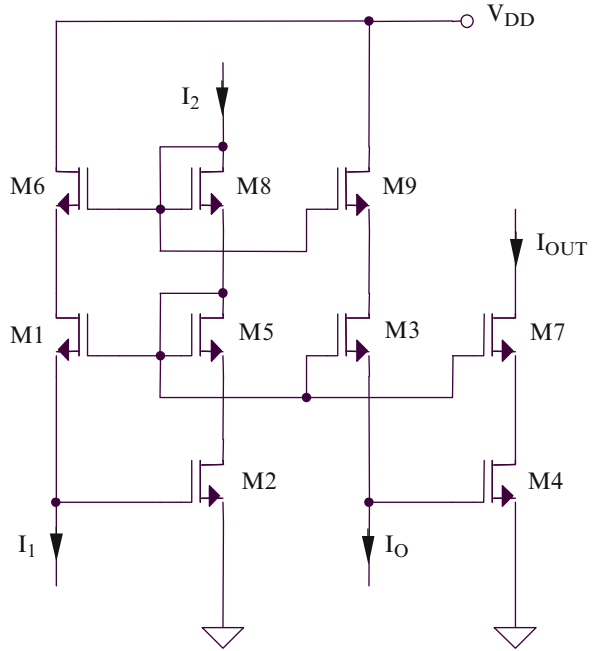
The biasing currents of these transistors are:  $I_1$  for M1,  $I_2$  for M2,  $I_O$  for M3 and  $I_{OUT}$  for M4. The previous relation can be written as:

$$\begin{aligned} & nV_{th} \ln \left[ \frac{I_1}{(W/L)I_{D0}} \right] + nV_{th} \ln \left[ \frac{I_2}{(W/L)I_{D0}} \right] \\ &= nV_{th} \ln \left[ \frac{I_O}{(W/L)I_{D0}} \right] + nV_{th} \ln \left[ \frac{I_{OUT}}{(W/L)I_{D0}} \right] \end{aligned} \quad (2.374)$$

resulting:

$$I_{OUT} = \frac{I_1 I_2}{I_O} \quad (2.375)$$

**Fig. 2.80** Multiplier circuit  
(3) based on PR 2.11



A four-quadrant multiplier derived from the circuit presented in Fig. 2.80 is shown in Fig. 2.81 [44].

Similarly with the previous circuit:

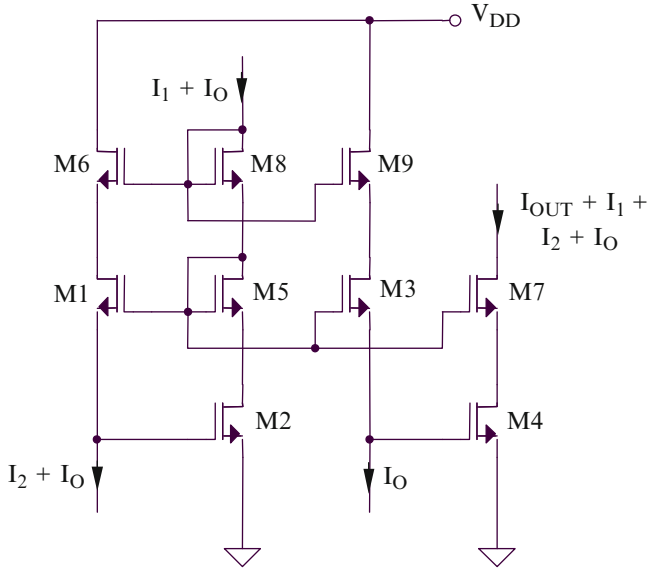
$$I_{D7} = \frac{(I_O + I_1)(I_O + I_2)}{I_O} = I_O + I_1 + I_2 + \frac{I_1 I_2}{I_O} \quad (2.376)$$

resulting the following expression of the output current:

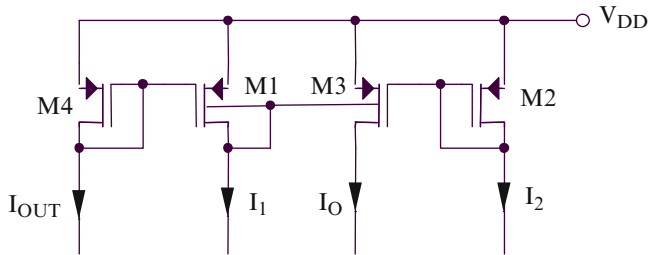
$$I_{OUT} = I_{D7} - I_O - I_1 - I_2 = \frac{I_1 I_2}{I_O} \quad (2.377)$$

The circuit presented in Fig. 2.82 [47, 48] represents a current multiplier implemented using MOS transistors biased in weak inversion region. Using the exponential dependence of the drain current on the gate-source and bulk-source voltages for a subthreshold-operated MOS device, the ratio between  $I_2$  and  $I_{OUT}$  currents can be expressed as follows:

$$\frac{I_2}{I_{OUT}} = \frac{I_{DO} \exp \left[ \frac{V_{SG2} + (n-1)V_{SB2}}{nV_{th}} \right]}{I_{DO} \exp \left[ \frac{V_{SG4} + (n-1)V_{SB4}}{nV_{th}} \right]} = \exp \left( \frac{V_{SG2} - V_{SG4}}{nV_{th}} \right) \quad (2.378)$$



**Fig. 2.81** Multiplier circuit (4) based on PR 2.11



**Fig. 2.82** Multiplier circuit (5) based on PR 2.11

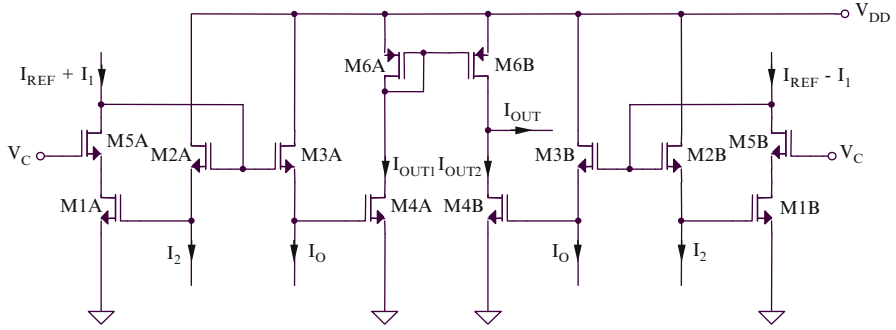
Using the exponential dependence of the drain current on the gate-source voltage for a MOS transistor biased in weak inversion region, it can be obtained:

$$V_{SG2} = V_{SG3} = nV_{th} \ln\left(\frac{I_O}{I_{DO}}\right) - (n-1)V_{SB3} \quad (2.379)$$

and:

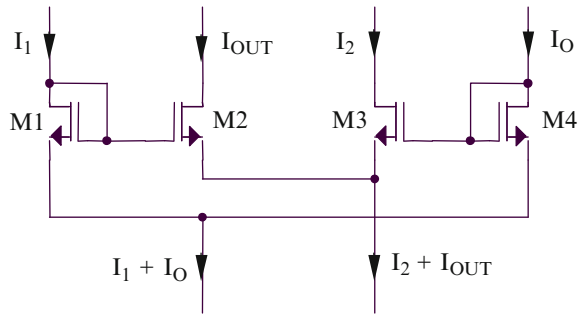
$$V_{SG1} = V_{SG4} = nV_{th} \ln\left(\frac{I_1}{I_{DO}}\right) - (n-1)V_{SB1} \quad (2.380)$$





**Fig. 2.84** Multiplier circuit (7) based on PR 2.11

**Fig. 2.85** Multiplier circuit (8) based on PR 2.11



and, similarly, for the translinear loop implemented using the gate-source voltages of M1B–M5B transistors:

$$I_{OUT2} = \frac{I_2}{I_O} (I_{REF} - I_1) \quad (2.387)$$

The expression of the differential output current of the entire structure will be:

$$I_{OUT} = I_{OUT1} - I_{OUT2} = 2 \frac{I_1 I_2}{I_O} \quad (2.388)$$

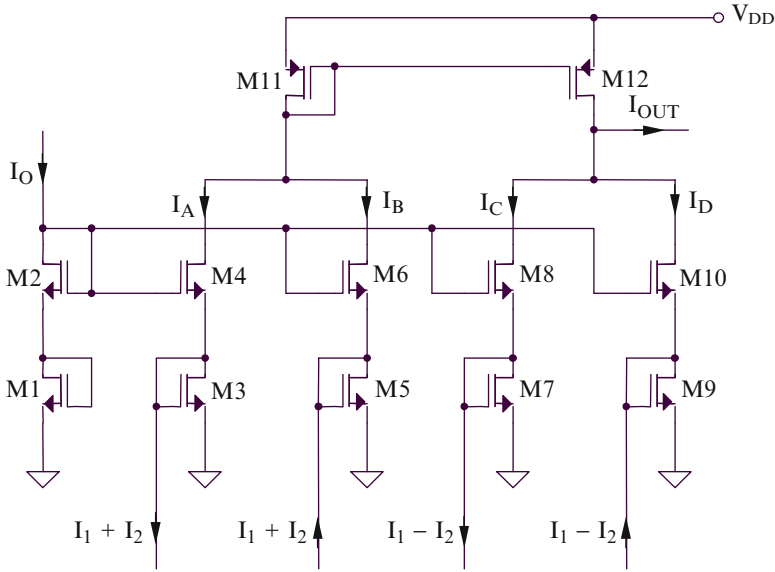
A possible realization of a current multiplier is presented in Fig. 2.85 [50].

The translinear loop implemented using M1–M4 transistors has the following characteristic equation:

$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \quad (2.389)$$

For a biasing in weak inversion of the circuit transistors, the previous relation becomes:

$$I_{OUT} = \frac{I_1 I_2}{I_O} \quad (2.390)$$



**Fig. 2.86** Multiplier circuit (1) based on PR 2.Db

#### 2.2.2.4 Multiplier circuits based on different mathematical principle (PR 2.Db)

The circuit presented in Fig. 2.86 [51] represents a current multiplier, having a principle of operation based on four translinear loops. The first loop contains M1–M4 transistors, M1–M2 pair being biased at the reference current,  $I_O$ , M3 transistor – at  $I_A - I_1 - I_2$  drain current, while M3 transistor is working at  $I_A$  current.

The characteristic equation of the translinear loop can be written as follows:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \quad (2.391)$$

resulting, for a biasing in saturation of all MOS transistors:

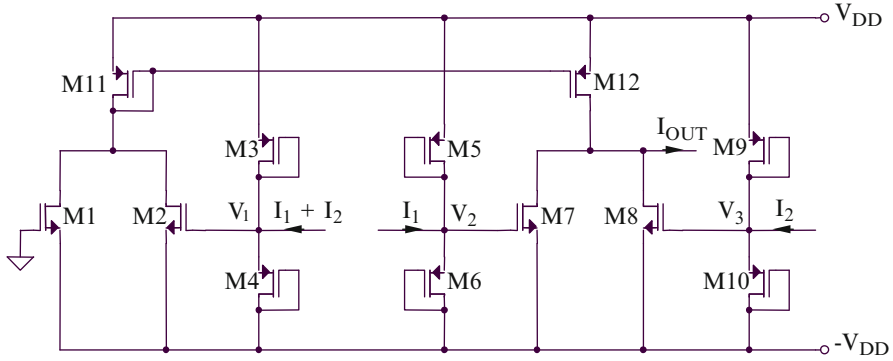
$$2\sqrt{I_O} = \sqrt{I_A} + \sqrt{I_A - I_1 - I_2} \quad (2.392)$$

Squaring the previous relation, it can be obtained:

$$4I_O = 2I_A - I_1 - I_2 - 2\sqrt{I_A(I_A - I_1 - I_2)} \quad (2.393)$$

So, the  $I_A$  current will have the following expression:

$$I_A = I_O + \frac{I_1}{2} + \frac{I_2}{2} + \frac{I_1 I_2}{8I_O} + \frac{I_1^2}{16I_O} + \frac{I_2^2}{16I_O} \quad (2.394)$$



**Fig. 2.87** Multiplier circuit (2) based on PR 2.Db

Similarly, considering the translinear loops implemented using the gate-source voltages of M1, M2, M5, M6 and M1, M2, M7, M8 and, respectively, M1, M2, M9, M10 transistors, it results the following expressions of the other three output currents:

$$I_B = I_O - \frac{I_1}{2} - \frac{I_2}{2} + \frac{I_1 I_2}{8I_O} + \frac{I_1^2}{16I_O} + \frac{I_2^2}{16I_O} \quad (2.395)$$

$$I_C = I_O + \frac{I_1}{2} - \frac{I_2}{2} - \frac{I_1 I_2}{8I_O} + \frac{I_1^2}{16I_O} + \frac{I_2^2}{16I_O} \quad (2.396)$$

$$I_D = I_O - \frac{I_1}{2} + \frac{I_2}{2} - \frac{I_1 I_2}{8I_O} + \frac{I_1^2}{16I_O} + \frac{I_2^2}{16I_O} \quad (2.397)$$

The output current can be expressed as follows:

$$I_{OUT} = (I_A + I_B) - (I_C + I_D) = \frac{I_1 I_2}{2I_O} \quad (2.398)$$

The independence of the circuit performances on technological parameters and, as a result, their immunity with respect to technological errors, represents an important characteristic of the previously presented multiplier circuit.

The circuit presented in Fig. 2.87 [52] implements the current multiplying function. Transistors M5 and M6 form a voltage divider with an input current,  $I_1$ , that will modify the divided potential  $V_2$ . The current balance in this point can be quantitatively evaluated by the following relation:

$$\frac{K}{2} (V_{DD} - V_2 - V_T)^2 + I_1 = \frac{K}{2} (V_2 + V_{DD} - V_T)^2 \quad (2.399)$$

resulting:

$$V_2 = \frac{I_1}{2K(V_{DD} - V_T)} \quad (2.400)$$

The output current of the circuit will linearly depend on the following drain currents:

$$I_{OUT} = I_{D1} + I_{D2} - I_{D7} - I_{D8} \quad (2.401)$$

the previous currents having the following expressions:

$$I_{D1} = \frac{K}{2}(V_{DD} - V_T)^2 \quad (2.402)$$

$$I_{D2} = \frac{K}{2}(V_1 + V_{DD} - V_T)^2 = \frac{K}{2} \left[ \frac{I_1 + I_2}{2K(V_{DD} - V_T)} + V_{DD} - V_T \right]^2 \quad (2.403)$$

$$I_{D7} = \frac{K}{2}(V_2 + V_{DD} - V_T)^2 = \frac{K}{2} \left[ \frac{I_1}{2K(V_{DD} - V_T)} + V_{DD} - V_T \right]^2 \quad (2.404)$$

and:

$$I_{D8} = \frac{K}{2}(V_3 + V_{DD} - V_T)^2 = \frac{K}{2} \left[ \frac{I_2}{2K(V_{DD} - V_T)} + V_{DD} - V_T \right]^2 \quad (2.405)$$

So, the output current will be proportional with the product between the input currents:

$$I_{OUT} = \frac{I_1 I_2}{4K(V_{DD} - V_T)^2} \quad (2.406)$$

The disadvantage of this circuit is represented by the dependence of the output current on the supply voltage and on the threshold voltage.

## 2.3 Conclusion

Chapter describes the principle of operation of CMOS multiplier circuits and, starting from their functional principle of operation, it presents many implementations in CMOS technology of these computational structures. There were analyzed multiplier

circuits having both current-input and voltage-input variables. Depending on the power consumption imposed to the designs, two important classes of multiplier structures have been presented. For improving the frequency response, circuits using exclusively MOS transistors biased in saturation region have been used, while low-power multipliers have been designed based on subthreshold-operated MOS active devices. The linearity of multiplier circuits has been improved by applying specific design techniques.

## References

1. Kim YH, Park SB (1992) Four-quadrant CMOS analogue multiplier. *Electron Lett* 28:649–650
2. Wallinga H, Bult K (1989) Design and analysis of CMOS analog signal processing circuits by means of a graphical MOST model. *IEEE J Solid-State Circuits* 24:672–680
3. Shen-Iuan L, Chen-Chieh C (1997) Low-voltage CMOS four-quadrant multiplier. *Electron Lett* 33:207–208
4. Gunhee H, Sanchez-Sinencio E (1998) CMOS transconductance multipliers: a tutorial. *IEEE Trans Circuits Syst II: Analog Digit Signal Process* 12:1550–1563
5. Chen JJ, Liu SI, Hwang YS (1998) Low-voltage single power supply four-quadrant multiplier using floating-gate MOSFETs. *IEE proceedings on circuits, devices and systems*, pp 40–43
6. Sawigun C, Mahattanakul J (2008) A 1.5 V, wide-input range, high-bandwidth, CMOS four-quadrant analog multiplier. *IEEE international symposium on circuits and systems*, pp 2318–2321, Washington, USA
7. Sawigun C, Demosthenous A, Pal D (2007) A low-voltage, low-power, high-linearity CMOS four-quadrant analog multiplier. *European conference on circuit theory and design*, pp 751–754, Seville, Spain
8. Liu SI, Hwang YS (1993) CMOS four-quadrant multiplier using bias offset crosscoupled pairs. *Electron Lett* 29:1737–1738
9. Ramirez-Angulo J, Carvajal RG, Martinez-Heredia J (2000) 1.4 V supply, wide swing, high frequency CMOS analogue multiplier with high current efficiency. *IEEE international symposium on circuits and systems*, pp 533–536, Geneva, Switzerland
10. Popa C (2006) Improved linearity active resistor with controllable negative resistance. *IEEE international conference on integrated circuit design and technology*, pp 1–4, Padova, Italy
11. Langlois PJ (1990) Comments on “A CMOS four-quadrant multiplier”: effects of threshold voltage. *IEEE J Solid-State Circuits* 25:1595–1597
12. Zarabadi SR, Ismail M, Chung-Chih H (1998) High performance analog VLSI computational circuits. *IEEE J Solid-State Circuits* 33:644–649
13. Popa C (2009) High accuracy CMOS multifunctional structure for analog signal processing. *International semiconductor conference*, pp 427–430, Sinaia, Romania
14. De La Cruz Blas CA, Feely O (2008) Limit cycle behavior in a class-AB second-order square root domain filter. *IEEE International conference on electronics, circuits and systems*, pp 117–120, St. Julians, Malta
15. Popa C (2001) Low-power rail-to-rail CMOS linear transconductor. *International semiconductor conference*, pp 557–560, Sinaia, Romania
16. Sakurai S, Ismail M (1992) A CMOS square-law programmable floating resistor independent of the threshold voltage. *IEEE Trans Circuits Syst II: Analog Digit Signal Process* 39:565–574
17. Jong-Kug S, Charlot J (2000) A CMOS inverse trigonometric function circuit. *IEEE midwest symposium on circuits and systems*, pp 474–477, Michigan, USA
18. Popa C (2010) CMOS multifunctional computational structure with improved performances. *International semiconductors conference*, pp 471–474, Sinaia, Romania

19. Popa C (2002) CMOS transconductor with extended linearity range. IEEE international conference on automation, quality and testing, robotics, pp 349–354, Cluj, Romania
20. Manolescu AM, Popa C (2009) Low-voltage low-power improved linearity CMOS active resistor circuits. Springer J Analog Integr Circuits Signal Process 62:373–387
21. Babanezhad JN, Temes GC (1985) A 20-V four-quadrant CMOS analog multiplier. IEEE J Solid-State Circuits 20:1158–1168
22. Popa C, Manolescu AM (2007) CMOS differential structure with improved linearity and increased frequency response. International semiconductor conference, pp 517–520, Sinaia, Romania
23. Popa C (2008) Programmable CMOS active resistor using computational circuits. International semiconductor conference, pp 389–392, Sinaia, Romania
24. Popa C (2009) Multiplier circuit with improved linearity using FGMOS transistors. International symposium ELMAR, pp 159–162, Zadar, Croatia
25. Seng YK, Rofail SS (1998) Design and analysis of a  $\pm 1$  V CMOS four-quadrant analogue multiplier. IEE proceedings on circuits, devices and systems, pp 148–154, Florida, USA
26. Kathiresan G, Toumazou C (1999) A low voltage bulk driven downconversion mixer core. IEEE international symposium on circuits and systems, pp 598–601, Florida, USA
27. Szczepanski S, Koziel S (2004) 1.2 V low-power four-quadrant CMOS transconductance multiplier operating in saturation region. International symposium on circuits and systems, pp 1016–1019, Vancouver, Canada
28. Coban AL, Allen PE (1994) A 1.5 V four-quadrant analog multiplier. Midwest symposium on Sch of Electr and Comput Eng, pp 117–120, La Fayette, USA
29. Manolescu AM, Popa C (2011) A 2.5 GHz CMOS mixer with improved linearity. J Circuits Syst Comp 20:233–242
30. Popa C, Coada D (2003) A new linearization technique for a CMOS differential amplifier using bulk-driven weak-inversion MOS transistors. International symposium on circuits and systems, pp 589–592, Iasi, Romania
31. Akshatha BC, Akshintala VK (2009) Low voltage, low power, high linearity, high speed CMOS voltage mode analog multiplier. International conference on emerging trends in engineering and technology, pp 149–154, Nagpur, India
32. Shen-Iuan L, Yuh-Shyan H (1995) CMOS squarer and four-quadrant multiplier. IEEE Trans Circuits Syst I: Fundam Theory Appl 42:119–122
33. Xiang-Luan Jia WH, Shi-Cai Q (1995) A new CMOS analog multiplier with improved input linearity. IEEE region 10 international conference on microelectronics and VLSI, pp 135–136, Hong Kong
34. Szczepanski S, Koziel S (2002) A 3.3 V linear fully balanced CMOS operational transconductance amplifier for high-frequency applications. IEEE international conference on circuits and systems for communications, pp 38–41, St. Petersburg, Russia
35. Mahmoud SA (2009) Low voltage low power wide range fully differential CMOS four-quadrant analog multiplier. IEEE international midwest symposium on circuits and systems, pp 130–133, Cancun, Mexico
36. Popa C (2010) Improved linearity CMOS active resistor based on complementary computational circuits. IEEE international conference on electronics, circuits, and systems, pp 455–458, Athens, Greece
37. Psychalinos C, Vlassis S (2002) A systematic design procedure for square-root-domain circuits based on the signal flow graph approach. IEEE Trans Circuits Syst I: Fundam Theory Appl 49:1702–1712
38. Naderi A et al (2009) Four-quadrant CMOS analog multiplier based on new current squarer circuit with high-speed. IEEE international conference on “Computer as a tool”, pp 282–287, St. Petersburg, Russia
39. Naderi A, Khoei A, Hadidi K (2007) High speed, low power four-quadrant CMOS current-mode multiplier. IEEE international conference on electronics, circuits and systems, pp 1308–1311, Marrakech, Morocco

40. Arthansiri T, Kasemsuwan V (2006) Current-mode pseudo-exponential-control variable-gain amplifier using fourth-order Taylor's series approximation. *Electron Lett* 42:379–380
41. Bult K, Wallinga H (1987) A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation. *IEEE J Solid-State Circuits* 22:357–365
42. Popa C (2003) Low-power CMOS bulk-driven weak-inversion accurate current-mode multiplier/divider circuits. *International conference on electrical and electronics engineering*, pp 66–73, Bursa, Turkey
43. Popa C (2009) Computational circuits using bulk-driven MOS devices. *IEEE international conference on "Computer as a tool"*, pp 246–251, St. Petersburg, Russia
44. Wilamowski BM (1998) VLSI analog multiplier/divider circuit. *IEEE international symposium on industrial electronics*, pp 493–496, Pretoria, South Africa
45. De La Cruz-Blas CA, Lopez-Martin A, Carlosena A (2003) 1.5-V MOS translinear loops with improved dynamic range and their applications to current-mode signal processing. *IEEE Trans Circuits Syst II: Analog Digit Signal Process* 50:918–927
46. Popa C (2003) A new curvature-corrected voltage reference based on the weight difference of gate-source voltages for subthreshold-operated MOS transistors. *International symposium on circuits and systems*, pp 585–588, Iasi, Romania
47. Cheng-Chieh C, Li S-I (1998) Weak inversion four-quadrant multiplier and two-quadrant divider. *Electron Lett* 34:2079–2080
48. Khateb F, Biolek D, Khatib N, Vavra J (2010) Utilizing the bulk-driven technique in analog circuit design. *IEEE international symposium on design and diagnostics of electronic circuits and systems*, pp 16–19, Vienna, Austria
49. Shu-Xiang S, Guo-Ping Y, Hua C (2007) A new CMOS electronically tunable current conveyor based on translinear circuits. *International conference on ASIC*, pp 569–572, Guilin, China
50. Gravati M, Valle M, Ferri G, Guerrini N, Reyes N (2005) A novel current-mode very low power analog CMOS four quadrant multiplier. *Solid-state circuits conference*, pp 495–498, Grenoble, France
51. Oliveira VJS, Oki N (2005) Low voltage analog synthesizer of orthogonal signals: a current-mode approach. *IEEE international symposium on circuits and systems*, pp 3708–3712, Kobe, Japan
52. Gravati M, Valle M, et al (2005) A novel current-mode very low power analog CMOS four quadrant multiplier. *Solid-state circuits conference*, pp 495–498, Grenoble, France
53. Cheng-Chieh C, Shen-Iuan L (1998) Weak inversion four-quadrant multiplier and two-quadrant divider. *Electron Lett* 34:2079–2080
54. Sawigun C, Serdijn WA (2009) Ultra-low-power, class-AB, CMOS four-quadrant current multiplier. *Electron Lett* 45:483–484
55. Hidayat R, Dejhan K, Moungnoul P, Miyanaga Y (2008) OTA-based high frequency CMOS multiplier and squaring circuit. *International symposium on intelligent signal processing and communications systems*, pp 1–4, Bangkok, Thailand
56. Machowski W, Kuta S, Jasielski J, Kolodziejewski W (2010) Quarter-square analog four-quadrant multiplier based on CMOS inverters and using low voltage high speed control circuits. *International conference on mixed design of integrated circuits and systems*, pp 333–336, Wroclaw, Poland
57. Ehsanpour M, Moallem P, Vafaei A (2010) Design of a novel reversible multiplier circuit using modified full adder. *International conference on computer design and applications*, pp V3-230–V3-234, Hebei, China
58. Parveen T, Ahmed MT (2009) OFC based versatile circuit for realization of impedance converter, grounded inductance, FDNR and component multipliers. *International multimedia, signal processing and communication technologies*, pp 81–84, Aligarh, India
59. Feldengut T, Kokozinski R, Kolnsberg S (2009) A UHF voltage multiplier circuit using a threshold-voltage cancellation technique. *Research in microelectronics and electronics*, pp 288–291, Cork, Ireland
60. Naderi A, Mojarrad H, Ghasemzadeh H, Khoei A, Hadidi K (2009) Four-quadrant CMOS analog multiplier based on new current squarer circuit with high-speed. *IEEE international conference on "Computer as a tool"*, pp 282–287, St. Petersburg, Russia

Synthesis of Computational Structures for Analog  
Signal Processing

Popa, C.R.

2012, XV, 449 p., Hardcover

ISBN: 978-1-4614-0402-6