Preface

State-of-the-art electronic systems are based on hundreds of functional blocks (called IP, intellectual property cores) such as processors, memories, analog blocks, etc. which are integrated and manufactured together in a single silicon die. Those blocks need to communicate with each other and exchange another several thousands of bits in order to operate as a cell phone, an MP3 player, an HDTV decoder, etc. The design of a communication infrastructure within such complex systems (called SoCs – systems-on-chip) is a problem per se, because it requires high performance and high quality levels while connecting an ever increasing number of cores. Such requirements can be typically met by a dedicated communication channel between two functional blocks, but this approach is not feasible when hundreds of blocks are involved. Thus, Networks-on-chip (NoCs) have been proposed as a solution to face the communication challenge within complex core-based electronic systems. However, to become an industrial reality, this new design paradigm still depends on the definition of feasible, efficient, and plug-and-play test mechanisms that can be used not only during manufacturing, to ensure a fault-free system, but also during operation, to ensure the correct behavior of the entire system. Such test mechanisms must apply to both the network itself and the IPs connected through the NoC since the whole system is integrated in a single die. Assuming the NoC is used to test the embedded IP cores, then the test of the NoC itself becomes an even more important issue to ensure the system test quality. On the other hand, the huge number of interconnects allied to the shrinking of the chip dimensions make the NoC prone to a growing number of permanent and transient faults. The capability of detecting and, if possible, tolerating such faults in NoC-based systems-on-chips is mandatory to increase the number of dies that can be delivered and to ensure the correct operation of the system afterwards.

It is within the context reported above that this book presents an overview of the issues related to the test, diagnosis, and fault-tolerance of NoC-based systems. First, the characteristics of the NoC design (topologies, structures, routers, wrappers, and protocols) are presented, as well as a summary of the terms used in the field and an overview of the existing industrial and academic NoCs. Secondly, the main aspects

of the test of a NoC-based system are discussed, starting with the test of the embedded cores where the NoC plays an important role. Current test strategies are presented, such as the reuse of the network for core testing, test scheduling for the NoC reuse, test access methods and interface, efficient reuse of the network, and power-aware and thermal-aware NoC-based SoC testing. Then, the challenges and solutions for the NoC infrastructure (interconnects, routers, and network interface) test and diagnosis are presented. Finally, fault tolerance techniques for the NoC are discussed, including techniques based on error control coding, retransmission, fault location, and system reconfiguration.

The main motivation to publish this book these days is the increasing interest on NoC-based designs in academia and industry. This new design paradigm is becoming an important trend because of its advantages on tackling the challenges of a complex SoC design. However, to become a real standard and an industrial reality, it is important that the issues related to its testing and to the testing of the systems built upon it are also well understood and dominated. Furthermore, as yield figures become an important issue for current technologies and electronic systems support an increasing number of safety-critical applications, fault-tolerance is mandatory for a large number of NoC-based devices. For the last 5 years or so, a number of testing and fault tolerance approaches have been proposed for NoCs and NoC-based systems. Although this is a relatively new topic, current research covers already a considerable spectrum and its analysis at this point can help summarizing the scientific and technological advances made so far and to identify the open issues that still need to be addressed. On the other hand, a book that organizes such a large material can be of great help to those willing to start looking at reliability, availability and serviceability aspects of NoCs.

The authors of this book have been working on these topics for many years now, have published important results in major test conferences (ITC, VTS, ETS, DATE, etc.) and journals (IEEE TCOMP, ACM TODAES, IEEE TCAD, IEEE D&T of Computers, IET Computers and Digital Techniques), and have presented tutorials in different meetings (ETS 2008, SBCCI 2008, DATE 2009, ISCAS 2009, NOCS 2009, VTS 2010). The feedback received in all occasions was so positive, that we felt encouraged to summarize all these past experiences and produce this book.

Testing and fault tolerance architectures for NoC-based SoCs are rather recent research topics and, to the best of our knowledge, no other published book is exclusively devoted to investigate both of them simultaneously. Professionals, graduate students, design and test engineers, and researchers interested in having introductory and intermediate knowledge on recent advances in test, diagnosis, and fault-tolerance of integrated systems based on Networks-on-Chip, will find in this book a reference guide. We want the reader to understand the problems, challenges, most important solutions, and trade-offs related to the quality of NoC-based systems. We also want it to be a didactical book in the sense that the reader can reproduce the presented techniques either as a solution for a possible real problem or as the means to extract its own observations and conclusions and advance the state-of-the-art in this topic.

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