

Preface

Motivation and Scope

Silicon-based electronics has been one of the key factor contributing for the creation and refinement of modern and sophisticated end-user applications. Examples of these achievements are reflected by the most recent mobile platforms able to carry out very complex tasks. In fact, they aggregate, in a single product, complex multi-standard and multi-mode radio transceivers (e.g., GSM, 3G, WiFi, Bluetooth) as well as digital processors able to reach high processing capabilities reinforced by significant amount of memory. However, these driving forces are still strongly accelerating, and therefore pushing the technology to continue to grow at a high rate. The known Moore's law [1] for digital technology, Edholm's law [2] for access bandwidth and Metcalfe's law [3] for network value, try to quantify this technology escalation.

At the end of 2008, more than 4 billion mobile phones were estimated to exist worldwide, representing more than 60% of penetration. Another emerging market of wireless sensor networks will tend to grow significantly in the next years, which can already reach approximately 120 million of remote units by 2010. Those huge numbers of devices results from the continuous and successful increase of the digital processing capacity and also, indirectly, from the selected supporting technology: the Complementary Metal-Oxide-Semiconductor (CMOS). Alternative technologies, like Bipolar or GaAs, are less attractive for transistor density increase due to downscaling lithography issues.

In the last decades, the technology has evolved from minimum device length ranging from 10 μm in 1971 to 45 nm in 2008 [4] and 32 nm in 2010. Interestingly, Fig. 1 shows the evolution of the installed wafer production capacity, in Wafers *per* Week (WSpW), both for MOS and Bipolar technologies, according to SICAS data [5]. It is clear from it that the production capacity has been completely dominated by

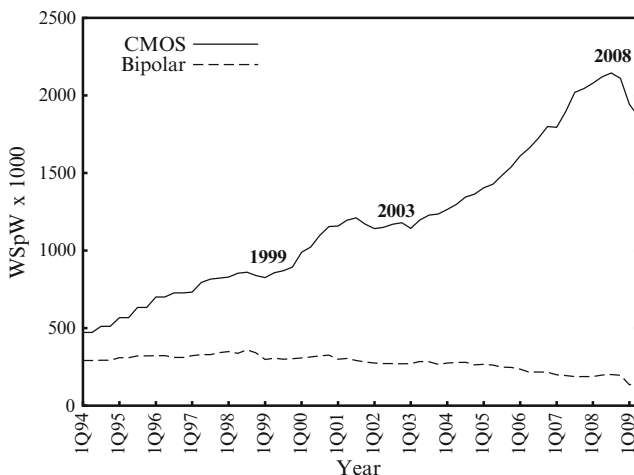


Fig. 1 Comparative evolution of the Bipolar and MOS installed wafer production capacity, based on data available from SICAS [5]

MOS technology in last years¹. Relative process simplicity and high manufacturing capacity contributed to lower the wafer die cost of CMOS when compared to Bipolar-CMOS (BiCMOS) or other alternative compound of distinct semiconductor technologies.

It is likely that competitive pressure will dictate that wireless applications (namely those related to a software defined radio architecture in a single chip), which can be implemented with acceptable performance in CMOS, will be effectively implemented in CMOS.

The CMOS scaling path has been evolving towards to higher integration level. In addition to this corresponding increase in device density, the process has significantly improved the switching speed, which is the result of higher transistor transition frequency (f_T) (this is a positive improvement for the integration of analog radio-frequency stages). On the other hand, the total chip power dissipation tends to be more demanding due to higher number of transistors *per* area unit. One of the selected countermeasure consists in reducing the applied power supply voltage, which will be as low as 0.5 V by 2020 [6]. Relatively to the transistor intrinsic gain (defined as the ratio between the device transconductance and the output conductance, g_m/g_{ds}), this value has decreased due to higher g_{ds} , degrading the gain achieved by operational amplifiers (opamps) and worsen the performance of closed loop configurations.

As a partial conclusion, while Moores Law has been predictive of continuous gains in digital circuit scaling, the relative performance of analog circuits has

¹As an out of scope remark, it can be detected in Fig. 1 the impact of economic crisis in 1999, 2003 and 2008.

not scaled along with digital ones, and some inherent challenges intensify with reduced supply voltage. In order to overcome some of these issues, new design methodologies both at the circuit and system levels have to be addressed together for the design of optimum wireless transceivers in submicron and nanoscale CMOS.

As digital circuitry has scaled down, it has become practical to use digital processing in conjunction with analog functions to offload some of the already known bottlenecks, making the track of digitally assisted analog an important one. At the analog circuit level, amplifier configurations stages with gain directly dependent on the g_m/g_{ds} ratio will experience a performance degradation due to lower size MOS transistors. Alternatively, new amplification approaches have to be found or recovered from earlier electronics, one of them being the Parametric Amplification.

In a Parametric Amplifier (PAMP), the amplification is governed by varying, with time, the reactance value of a capacitor or an inductor. In a traditional amplifier, the gain is mostly dependent on the transconductance and output conductance, and therefore, relies in a “resistive” type of configuration. Since the intrinsic gain process of a PAMP does depend on a time-varying reactance rather than on a “resistance”, it is intrinsically noiseless. Moreover, due to its simple nature, it adapts well to a low power supply, and since this reactance can be implemented using standard digital MOS devices, it is a promising technique to be used in digital nanoscale technologies. In other words, this contributes for the task of designing a full transceiver integration in a pure digital technology towards a low-cost MOSFET-only implementation. One of the main objectives of this book is to demonstrate the use of the parametric amplification technique as an alternative approach to overcome some of the difficulties in designing traditional analog circuits, as CMOS technology scale evolves into nanoscale range. This is achieved by a set of innovative contributions [7–12] that are described ahead in more detail:

- A modified MOS parametric cell amplifier is proposed, [9]. Instead of a single MOS device, this modified cell uses two half-sized MOS devices which are connected in parallel and with one of the tied terminals left floating. As a consequence it is shown that it becomes possible to decrease the effect of extrinsic gate parasitic capacitance during amplification phase, and therefore reducing the loading effect on the effective gain. Main expressions are derived for this class of MOS parametric amplifier cells.
- Application of this amplifier cell in some of the most important modern transceiver building blocks. It is shown how this cell can be used in an original passive sampling mixer [12], in a comparator [7,8] (for low resolution flash ADC) and in a multiplying digital-to-analog (D/A) converter (MDAC²) for multi-step, algorithmic or pipeline ADCs, [10].

²The main function of an MDAC block is to reconstruct a residue and amplifying it by a power of 2 for subsequent analog processing.

- Both for the comparator and MDAC/residue-amplifier, analytical expressions are derived and are related with offset, gain accuracy, noise. This supports a design methodology for this type of cells. They demonstrate that it is possible to design medium resolution (5–8 bit) ADCs [11] using this parametric technique and without the need of post-processing digital calibration.
- An 8-bit 120 MHz time-interleaved pipeline ADC is designed and fabricated in 0.13 μm digital CMOS technology, using only MOS devices as consequence of the extensive use of parametric amplification techniques within the comparators and MDACs. It is then proved, by experimental results obtained from three different samples, that this parametric amplification technique is well suited for purely digital CMOS technology, [11].

Book Organization

This book is structured in six chapters, which are complemented by a couple of appendixes. After this Preface, the following one is dedicated to give an insight into the design space of modern wireless systems supported on modern nanoscale digital CMOS technology. As a result of the previous analysis, it becomes clear that the CMOS analog design process faces the need to use alternative circuit and transceiver system design techniques to achieve the low power, area and cost requirements. Within this context, Chap. 2 goes into the foundations of the parametric amplification principle, known since the middle of the twentieth century. This technique is presented as a promising one to be recovered and adapted to CMOS digital technology, by means of a discrete time configuration, which is fully analyzed in Chap. 3. Latest sections of Chap. 3 focus on the use of parametric amplifiers in major digital transceiver buildings blocks, specially inside an ADC. For this last circuit, the design, implementation and testing details of an integrated prototype that is fully based on parametric amplification are described in Chaps. 4 and 5.

In more detail, Chap. 1 aims to demonstrate that the wireless system design space is shaped by the increasing diversity of modern multi-standard wireless system requirements on the one hand and, on the other hand, by the evolution of CMOS technology into deep submicron range. Not only the former pushes the transceiver architecture towards a software defined one but also, the technology scaling increases the available digital processing power *per* unit of wafer area. Therefore, this chapter presents an overview of the technology scaling and its impact on the devices performance, and also gives an overview concerning the most suited transceiver architecture for the modern CMOS based wireless environment.

The analysis in Chap. 1 concerning CMOS scaling shows the impact on device conductance, intrinsic gain, speed, noise and leakage. It reveals that the design of traditional analog blocks, e.g., operational amplifiers, is getting more difficult to achieve due to several reasons, one of them being the reduction of the available voltage headroom. This chapter ends with an overview about present emerging circuit design techniques to overcome some of the above limitations. This chapter is

complemented by Appendix A in which, the signal amplifier from RF to baseband, mixer and oscillator are discussed, with the emphasis on inductorless topologies as well as open-loop configurations. This first appendix also presents a simple co-design strategy involving these three circuits and also refers to an alternative merged topology.

Interestingly, many of these blocks only need limited gain amplifiers and, therefore, the use of a reactance based amplifier is an alternative that the following chapters demonstrate to be compatible with CMOS digital technology.

Chapter 2 recovers the concept of parametric amplifiers, that rely on reactance elements to achieve signal amplification, rather than on resistive ones. The classical Manley-Rowe power relations are presented as a fundamental result to understand the transfer of power between the different signal frequencies involved on the circuit operation. It is also shown that the MOS variable capacitor (varactor) is a good candidate for the implementation of the continuous time parametric converter. The gain achieved by this type of structure is of limited value but since the amplification is reached by the parametric change to the capacitance value, it has the advantage of being intrinsically noiseless.

The extension of the parametric amplification to the discrete-time domain is described in Chap. 3. This chapter describes the principle of operation of the basic parametric amplifier cell complemented by analytical models for the gain and noise. A modified MOS parametric cell is then presented in order to reduce some parasitic capacitance effects from the original cell, [13]. The chapter ends with the use of parametric amplification in common analog MOS circuits. The main focus goes to a discrete-time mixer and filter, a comparator and a multiplying-by-two amplifier. It is shown that the MOS parametric cell can be used from high to low frequency applications.

Chapter 4 is completely dedicated to give a detailed description about the design of a time-interleaved pipeline ADC for intermediate frequencies (IF). The design is validated through pre and post layout simulations using the BSIM3v3 MOS model.

The experimental results of the pipeline ADC prototype described in Chap. 4 are presented in Chap. 5. The achieved results, based on measurements of three chip samples, show the effectiveness and reliability of using parametric amplification techniques in the design of moderate speed and medium resolution ADCs.

The last chapter (Chap. 6) draws the most relevant conclusions of this work.

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