

# Preface

Continued improvements of transceiver systems-on-a-chip play a key role in the advancement of mobile telecommunication products as well as wireless systems in medical and remote sensing applications. This book addresses the problems of escalating CMOS process variability and system complexity that diminish the reliability and testability of integrated systems, especially relating to the analog and mixed-signal blocks. [Chapter 1](#) introduces the technical demands and incentives to adopt variation-aware design approaches. The described design techniques and circuit-level attributes are aligned with current built-in testing and self-calibration trends for integrated transceivers, which are explained in [Chap. 2](#). The main attention in this book is on various recent works in which the performances of analog and mixed-signal blocks were enhanced with digitally adjustable elements as well as with automatic analog tuning circuits. To convey the concepts, several case studies are presented that span theoretical aspects and experimental results for variation-aware design approaches related to receiver front-end circuits, baseband filter linearization, and data conversion.

The use of digitally controllable elements to compensate for variations is exemplified with two circuits. First, a distortion cancellation method for operational transconductance amplifiers that enables a third-order intermodulation (IM3) improvement of up to 22 dB is presented in [Chap. 3](#). A transconductance-capacitor lowpass filter with linearized amplifiers is discussed, which was fabricated in a 0.13  $\mu\text{m}$  CMOS process with 1.2 V supply. This filter has a measured IM3 below  $-70$  dB (with 0.2 V peak-to-peak input signal swing) and 54.5 dB dynamic range over its 195 MHz bandwidth. The second example circuit is a 3-bit two-step quantizer with adjustable reference levels, which is the focal point of [Chap. 4](#). This quantizer was designed and fabricated in 0.18  $\mu\text{m}$  CMOS technology as part of a continuous-time  $\Sigma\Delta$  analog-to-digital converter system. With 5 mV resolution at a 400 MHz sampling frequency, the quantizer's power dissipation is 24 mW and its die area is 0.4  $\text{mm}^2$ .

An alternative to electrical power detectors is explained in [Chap. 5](#) by outlining a strategy for built-in testing of analog circuits with on-chip temperature sensors. Comparisons of an amplifier's measurement results at 1 GHz with the measured

DC voltage output of an on-chip temperature sensor show that the amplifier's power dissipation can be monitored and its 1 dB compression point can be estimated with less than 1 dB error. The sensor has a tunable sensitivity up to 200 mV/mW, a power detection range measured up to 16 mW, and it occupies a die area of 0.012 mm<sup>2</sup> in standard 0.18  $\mu$ m CMOS technology.

In [Chap. 6](#), an analog calibration technique is discussed to lessen the mismatch between transistors in the differential high-frequency signal path of analog CMOS circuits. The described methodology involves auxiliary transistors that sense the existing mismatch as part of a feedback loop for error minimization. It was assessed by performing statistical Monte Carlo simulations of a differential amplifier and a double-balanced mixer designed in CMOS technologies. Finally, [Chap. 7](#) summarizes the results and conclusions for this calibration case study as well as the other specific design examples in the book.

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