

Chapter 2

Process Variation Challenges and Solutions Approaches

Abstract The technical and economic impacts of worsening process variations and intra-die device mismatches are elaborated in this chapter, especially with regards to product yield, reliability, and manufacturing cost. This introduction is followed by a survey of diverse built-in testing and calibration approaches aimed at enhancing performance, yield, and reliability in the presence of variations.

2.1 Current Trends

2.1.1 The Impact of Rising Process Variations

Most semiconductor product improvements over the past decades are direct or indirect consequences of the perpetual shrinking of devices and circuits, allowing performance enhancements at lower fabrication cost. A paralleling trend is that process variations and intra-die variability increase with each technology node. Since most high-performance analog circuits depend on matched devices and differential signal paths, this trend has begun to diminish yields and reliabilities of chip designs. Fundamentally, the problem is that parameters of devices on the same die show increasing intra-die variations, thereby exhibiting different characteristics. For example, Table 2.1 displays the evolution of the typical transistor threshold voltage standard deviation $\sigma\{V_{Th}\}$ normalized by the threshold voltage (V_{Th}) for several technologies, as reported in [1]. Also notice that V_{Th} exhibits further dependence on gate length variations through the drain-induced-barrier-lowering (DIBL) effect under large drain-source voltage bias conditions, as demonstrated by the characterization in [2] using 65 nm technology. Since DIBL worsens as the channel is scaled down, this additional impact on threshold voltage variations can be assumed to be even stronger beyond the 65 nm technology node.

Table 2.1 Intra-die variability vs. CMOS technology node

Technology node	250 nm (%)	180 nm (%)	130 nm (%)	90 nm (%)	65 nm (%)	45 nm (%)
$\sigma\{V_{Th}\}/V_{Th}$	4.7	5.8	8.2	9.3	10.7	16

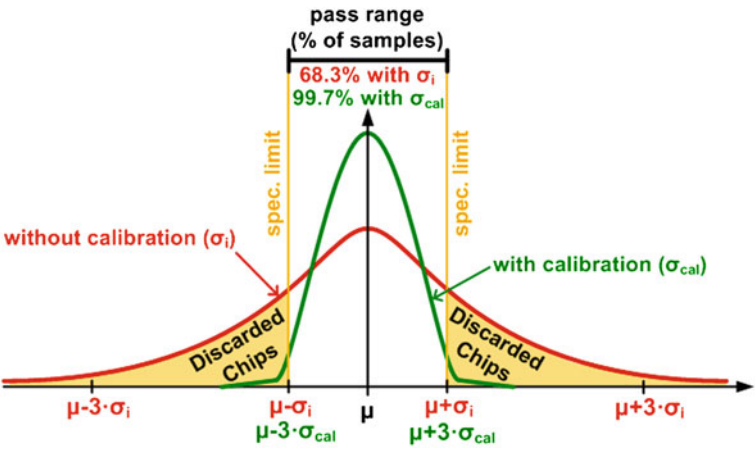
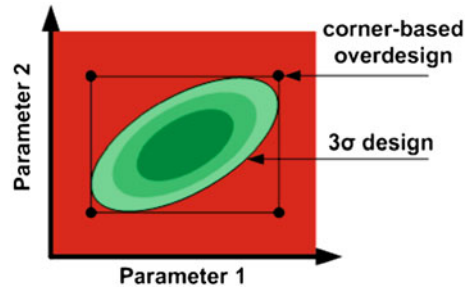


Fig. 2.1 Specification variation impact on the fraction of discarded chips

A direct consequence of device parameter variations is a decrease in production yields because block-level and system-level parameters will show a corresponding increase in variations. This relationship between variations and yield can be inferred from the visualization in Fig. 2.1, where the Gaussian distribution of a specification with a standard deviation σ around the mean value μ is shown together with the specification limits ($\pm 3\sigma$ in this example). For standalone analog circuits, parameters such as gain may have an upper and/or lower specification limit, and the samples that exceed the limit(s) during production testing must be discarded. Guardbands are often defined to account for measurement uncertainties by following procedures such as repeating the same test or performing other more comprehensive tests to determine whether the part can be sold to customers, which incurs additional test cost in a manufacturing environment.

An important observation from Fig. 2.1 is that an increase of variation (σ) widens the Gaussian distribution, which leads to a higher percentage of parts that fall within the highlighted ranges that require them to be scrapped or retested. Clearly, there is a direct relationship between the amount of process variations and production cost due to low yields. In the case of wireless mixed-signal integrated systems, the trend towards increasing integration and complexity has also been paralleled by technical challenges and rising cost of testing, which can amount up to 40–50% of the total manufacturing cost [3, 4]. As a consequence, built-in self-test, design-for-test, and design-for-manufacturability methods for analog and mixed-signal circuits have received growing attention over the past years.

Fig. 2.2 Process corner-based vs. 3σ design approaches



2.1.2 Circuit and System Design Tendencies

System complexities and process variations raise the importance of considering testability early in the design phase to avoid technical complications and time-to-market delays in the pre-production phase as well as test cost reduction during the production phase. Worst-case process corner models have been used extensively to account for variations during the design of analog circuits. But more recently, a paradigm shift towards the use of statistical models and Monte Carlo simulations has occurred. One of the main reasons for this development is that corner-based design easily results in too pessimistic designs [5], which is evident in Fig. 2.2. In this figure, the x-axis and y-axis represent the ranges over which two parameters can vary, and the area inside the ellipse indicates the combined range in which the 3σ limits are met. This region can be predicted with statistical Monte Carlo simulations for yield estimation. On the other hand, the area outside of the elliptical design space corresponds to design implementations that meet the specifications, but are over designed. This means that “investments” of area, power, or trade-offs with other parameters are made in order to allow acceptable performance despite of increased deviations of the two parameters from their nominal values. The rectangular region between the combination of the four worst corner cases of the two parameters includes over design space, implying that it involves costly performance or parameter trade-offs. This economic reason and the availability of more efficient computational tools have created a trend towards statistical yield optimizations rather than corner-based design [5].

Defect densities on wafers become worse in newer technologies and production yields decrease with increased chip size [6]. Self-test and self-repair schemes for digital circuits have been routinely incorporated into products for a long time, especially since on-chip verification of logic blocks and repair with redundant circuitry do not require analog instrumentation resources. The inclusion of scan chains gives easy access to internal digital circuitry through a minimal number of pins during production testing. Similarly, the standardized mixed-signal test bus (IEEE Std. 1149.4) has been developed to improve the testability of analog blocks by allowing better observation of internal nodes. Nowadays, the use of analog test buses within single-chip systems is feasible in the industry, but significant design

considerations are required to avoid that the interface circuitry does not affect the integrity of the analog signals or measurements [7].

In addition to the underlying variation and defect issues on the device level, several system-level and technology trends impair the testability and manufacturability of integrated circuits for mobile applications:

Support of multiple communication standards and more features on low-power chips

The wireless communication industry has experienced phenomenal growth in the past decade that resulted in low-power handheld devices with multi-purpose functionality such as video, voice, pictures, and internet access. The wireless local-area networks for laptops, desktops, and personal digital assistants (PDAs) include standards like Bluetooth, WiFi, IEEE 802.16, WiMAX, Ultra-Wideband (UWB), and GPS. Most relevant services for handheld devices range from 470 MHz to almost 11 GHz. The main technical challenge is the co-existence of wireless devices, which results in signal interference. This can be solved if more linear high-performance analog receiver front-ends are available to tolerate and filter out high-power interfering signals without saturation of the analog blocks due to high signal power levels. Further filtering and channel selection can be performed in the digital domain when the signal integrity is maintained by the processing through unsaturated highly-linear analog blocks. Support of multiple communication standards requires chips with more circuitry and complexity, which makes them less testable in the production stage because of limited access to internal nodes, interactions between blocks, and a higher number of test cases to verify functionality. Systems with more subcomponents are more likely to fail, which is another reason why yields of integrated receivers, transmitters, and transceivers are on the decline. Simultaneously, the processing of broadband signals in their front-ends mandates high-performance analog circuits, which in many cases requires continued circuit-level innovations for on-chip self-calibration to tune for optimum performance.

Process technology optimizations for digital circuits create analog design challenges

The main advantages of device scaling with CMOS technology are improved performance at higher frequencies, reduced power consumption, and increased levels of integration. Those benefits are particularly aiding the development of digital circuits and systems. With regards to analog circuits, deep-submicron technology scaling progress comes together with adverse effects such as reduced gains from lower transistor output impedances, design with limited voltage headroom, higher flicker noise levels, and reduced transistor linearity. Larger variability of parameters is caused by physical and fabrication limitations such as under-etching uncertainties, variations of effective transistor dimensions, severe channel length modulation due to higher electric fields, and channel dopant fluctuations. Interestingly, the random dopant fluctuations have reached a severity that can lead to significant threshold voltage mismatch in neighboring devices at the 65 nm node [8]. Additional reliability concerns arise from the restricted power that transistors can supply to the load without exceeding the low breakdown voltage of the deep submicron devices. Furthermore, digital CMOS processes often do not

provide high-quality passive devices required for conventional high-performance analog designs. For example, metal-insulator-metal (MIM) capacitors, high-resistivity polysilicon resistors, or well-characterized inductor models might not be available in a digital process, forcing analog designers to get by with metal-oxide-semiconductor (MOS) capacitors and standard polysilicon resistors. Both of these have higher parasitic capacitances to the substrate than the equal-valued MIM capacitors or high-resistivity polysilicon resistors. Scaling down transistors permits more digital functionality and memory on a single chip, but with less reliability especially for analog signal processing.

2.2 System Perspective on Transceiver Built-In Testing and Self-Calibration

The concepts and examples presented in this book are all involving circuit blocks which are found in conventional transceivers within mobile wireless devices. While equipping the circuit blocks with built-in test (BIT) and self-calibration features to compensate for variations, it is important to keep their role as part of the system in mind because of the interaction between blocks and the overall goal to optimize system-level performance specifications such as bit error rate (BER) or error vector magnitude (EVM). In general, the self-calibration challenge can be divided into two parts: one is to add tunability and controllability capabilities in the individual blocks, and the other one is to devise comprehensive system-level calibration algorithms in a digital signal processing unit. The former task is the focus of this book, but the existing approaches for the latter task will be briefly discussed next and when applicable throughout the book.

BIT strategies for transceivers vary tremendously depending on the transceiver architecture, communication standard, available on-chip measurement and computation resources, the production volume, and whether the BIT is designed for production testing (quality control) or on-line self-calibration (reliability) during the life time of the chip. Consequently, most BITs involve a mix of analog and digital blocks, on-chip and off-chip measurement devices, long calibration routines at start-up, and shorter periodic or on-line calibration. Generally, a trend has emerged to combine techniques for verification of complex mixed-signal transceivers implemented as single chips. Nevertheless, the BIT approaches can be grouped into a few rough high-level categories that represent the different design philosophies in academia and the industry. In the following overview, a few example cases will be discussed to highlight the distinctive characteristics of methods that can be broadly classified into the categories below.

- Digital correction and calibration (digitally assisted)
- Analog measurements and tuning
- Loopback testing
- Combined digital performance monitoring and analog compensation
- Combined digital monitoring, analog measurements, and analog compensation

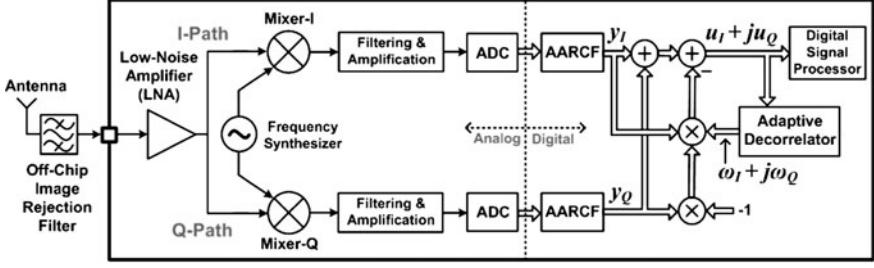


Fig. 2.3 Receiver with digital I/Q mismatch compensation

2.2.1 Digital Correction and Calibration

Digital BIT approaches involve measurements and compensation techniques that are realized in the digital baseband processor of the transceiver. They are suitable for parameters that are observable and traceable in the digital domain, such as slowly drifting DC offsets or mismatch between the in-phase (I) and quadrature-phase (Q) paths in the front-end. Generally, digital methods have the advantage of high precision when sufficient computational resources are available. They are also very attractive for on-line calibration schemes that run in the background.

Digital I/Q mismatch compensation is a widely used method that involves digital measurement and compensation of the I/Q gain and phase mismatches in the analog front-end circuitry. For example, the work in [9] presents a scheme that runs during start-up or in a dedicated calibration mode to ensure acceptable performance of a low-IF receiver even with up to 10% gain and 10° phase imbalance in the analog front-end. On-line digital I/Q compensation techniques have also been reported, such as [10], in which the training symbols that are standard in orthogonal frequency-division multiplexing (OFDM) transmissions are exploited for background I/Q calibration. It was also demonstrated in [10] how digital I/Q compensation relaxes the overall signal-to-noise ratio (SNR) requirements in the receiver chain because I/Q imbalance directly affects the SNR and thereby degrades the bit error rate (BER). In the OFDM receiver example presented in [10], the digital calibration allowed to improve the tolerance to I/Q imbalances from 1%-gain/1°-phase to 10%-gain/10°-phase.

Digital I/Q calibration is widely used in the industry. An example is the work from Texas Instruments describing a low-IF GSM receiver in 90 nm CMOS technology [11]. This receiver utilizes an adaptive filter that obtains the mismatch information from on-line I/Q correlations, for which the modified block diagram from [11] is displayed in Fig. 2.3. The interesting part of the block diagram is the adaptive decorrelator after the analog-to-digital converter (ADC) and anti-aliasing rate change filter (AARCF). In the digital domain, gain mismatch appears as difference in the auto-correlation between I and Q paths, while phase mismatch appears as nonzero cross-correlation between I and Q. The authors use an algorithm that takes advantage of the aforementioned relationships by implementing an

adaptive decorrelator which attempts to minimize the auto-correlation and the cross-correlation between I and Q outputs (y_I , y_Q). This is done by adjusting the correction coefficients:

$$\begin{aligned}\omega_{I(n+1)} &= \omega_{I(n)} + \mu \cdot [u_{I(n)} \cdot u_{I(n)} - u_{Q(n)} \cdot u_{Q(n)}], \omega_{Q(n+1)} \\ &= \omega_{Q(n)} + 2\mu \cdot u_{I(n)} \cdot u_{Q(n)}\end{aligned}\quad (2.1)$$

where μ is the adaptation step size which is inversely proportional to the signal energy. Thus, periodic training sequences are required with this scheme. Depending on process-voltage-temperature (PVT) variations, 15–30 dB image rejection ratio (IRR) improvement has been demonstrated in practice with phase mismatch $<1^\circ$ and amplitude mismatch $<10\%$ in [11] with a settling time in the range of 3–4 ms. This settling time is lengthy compared to analog tuning approaches that can be as short as a few microseconds [12], which becomes important in production testing situations because any adjustments for different test conditions in the front-end (different gain settings, channel, etc.) would require 3–4 ms idle time for digital I/Q calibration before the BER test can begin. On the other hand, settling times of analog tuning schemes depend on the loop bandwidth, which can be designed in the megahertz range to achieve settling times in the microseconds regime. Hence, analog I/Q tuning approaches would fill the niche of situations that require fast convergence.

The incentive for using a digital BIT technique is high when the circuit under test itself has digital features. An example is the BIT of a transmitter in [13] that includes an all-digital phase-locked loop (ADPLL). In that case, the error signal of the ADPLL is already in the digital domain, allowing to monitor failures and the center frequency drift of the digitally controlled oscillator. Furthermore, the authors of [13] state that digital filtering and spectral estimation can be used to monitor and adjust the phase noise transfer function.

2.2.2 Analog Measurements and Tuning

The analog equivalent to the digital I/Q imbalance calibration scheme has been proposed and demonstrated for image-reject receiver (IRRX) architectures. A simplified block diagram of such a BIT is displayed in Fig. 2.4, which is representing the work from [14]. In an IRRX, the down-conversion scheme with two mixing stages suppresses the image signal at the second intermediate frequency output $\text{Out}(f_{\text{IF2}})$, which avoids the need for an external image-rejection filter. The quality of the image-rejection is typically expressed with the image-rejection ratio (IRR) that depends on the I/Q amplitude mismatch (ΔA) and phase mismatch ($\Delta\theta$):

$$\text{IRR}_{(\text{dB})} \approx 10 \cdot \log \left((1/4) \cdot [(\Delta\theta)^2 + (\Delta A/A)^2] \right) \quad (2.2)$$

In practice, the IRR is normally limited to 25–40 dB due to mismatches, even though almost 60 dB are required for acceptable BER performance. In [14], a

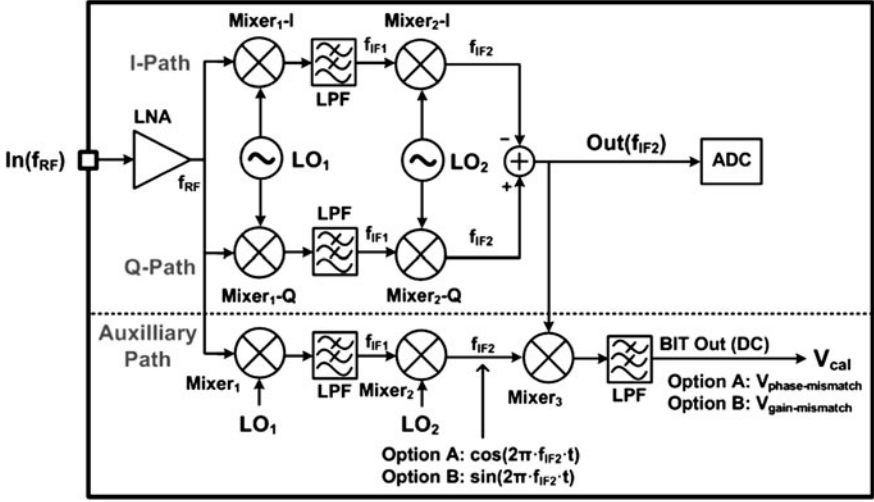
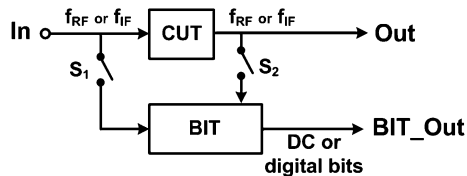


Fig. 2.4 Analog I/Q calibration for image-rejection receivers

purely analog calibration scheme was implemented with the auxiliary path shown in Fig. 2.4. This path contains the duplicate mixing operations as in the main path with the exception that the output signal at the second intermediate frequency (f_{IF2}) can be of the form $\cos(2\pi \cdot f_{IF2} \cdot t)$ or $\sin(2\pi \cdot f_{IF2} \cdot t)$, depending on which phases of the two local oscillators (LO_1 , LO_2) are routed to the auxiliary mixers. Finally, mixer₃ correlates the signals from the two paths to extract the I/Q mismatch information contained in the DC component after the lowpass filter (LPF). This analog DC voltage (V_{cal}) can be directly used to tune the bias voltages of analog circuits for mismatch compensation, resulting in high IRR (e.g. 57 dB in [14]). A similar automatic IRR calibration with analog mixers, variable phase shifter, and gain tuning has been realized in [15] with an IRR of 59 dB.

A benefit with analog tuning is that the bias conditions of the analog blocks under calibration are controlled and less affected by PVT variations due to the correcting action of the loops, thereby allowing higher yields as a result of automatic correction in the analog front-end. However, the power and area consumption of the BIT circuitry is the main trade-off. In addition, the BIT circuits themselves have to be designed robustly to avoid failures, making the implementation more challenging and invasive than digital calibration schemes. Efforts for the analog approach are generally more justified in transceivers that have few on-chip digital resources and in scenarios that require fast automatic correction. For example, the IRR calibration in [15] can be used on-line with a settling time that depends on the bandwidth of the analog control loops rather than convergence of digital algorithms which take several milliseconds as in [11]. Another fast analog calibration method with a convergence time in the microseconds regime is described in [12].

Fig. 2.5 BIT with analog instrumentation along the signal path



Instead of using a system-level test strategy, it has been more popular to extract information from each block in the analog front-end for characterization or tuning of the individual block, which is visualized in Fig. 2.5. The circuit under test (CUT) represents a block in the RF front-end or analog baseband that can be connected to a BIT circuit in test mode by closing the two switches S_1 and S_2 . In [16] for instance, a low-noise amplifier (LNA) was tested with a BIT block containing a test amplifier and two power detectors to measure input impedance, gain, noise figure, input return loss, and output SNR of the LNA. This approach has the advantage that the fault location/cause can be identified clearly and that the DC or digital outputs of the BIT circuits can be used to recover from certain failure modes. High-frequency RF front-ends have been targeted in particular with dedicated design of BIT circuits because gain, impedance matching, and linearity performances are very sensitive to variations. Furthermore, direct signal digitization is not feasible at high frequencies, eliminating many digital compensation schemes. Hence, several RF block-level measurement approaches involve power or amplitude detectors along the signal path [17–20].

Self-calibration of impedance matching for an LNA at the input of the receiver chain as done in [21] also requires on-chip analog sensing circuitry, especially to achieve a short calibration time such as the 30 μ s reported in [21]. An alternative proposition to monitor individual blocks in the signal path was made in [22], in which the transient supply currents of the CUTs are monitored with the BIT circuitry by placing small series resistors in the power supply lines. However, a clear disadvantage with any block-level measurement is that the BIT circuitry is connected to the CUT and therefore must be designed carefully to avoid impact on performance. But, some degradation due to loading effects from BIT circuitry must usually be tolerated. Furthermore, switches in or along the signal path are undesired due to their added noise, power losses and signal feed through from finite isolation, particularly at RF frequencies.

Though with less accuracy than off-chip measurement equipment, efforts have also been made to mimic conventional instrumentation such as spectrum analyzers [23, 24] on the chip with sufficient accuracy for BIT applications. In [23] for example, the analyzer with a frequency range of 33 MHz–3 GHz could cover the entire signal paths of many wireless transceivers in handheld consumer products. A multiplexer could be used to selectively route a test input at a time to one spectrum analyzer, but the on-chip measurement circuitry still takes up large area and significant power that might not be permissible in certain applications. For example the analyzer in [23] consumes 0.384 mm² and more than 20 mW.

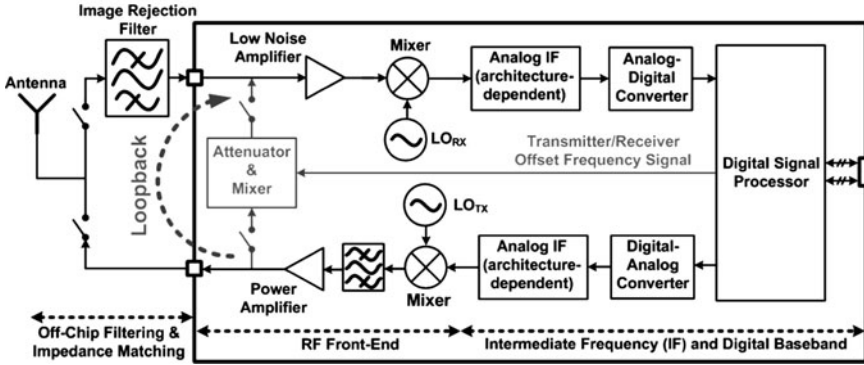


Fig. 2.6 Generalized transceiver block diagram with loopback

2.2.3 Loopback Testing

Loopback testing is a system-level BIT technique in which the BER is monitored in the digital baseband [25]. It allows simultaneous verification of the analog and digital transceiver blocks (Fig. 2.6) with a low-frequency digital input signal applied to the baseband subsection of the transmitter. This up-converted signal is routed from the transmitter (TX) output to the receiver (RX) input via a loopback connection [26]. After down-conversion and digitization in the RX, the received bitstream is analyzed in the digital baseband processor to determine the BER. Attenuation and frequency translation with a mixer are required in the loopback block to maintain signal integrity and to ensure that the power levels during testing are comparable to normal operation. If the communication standard does not require frequency translation between TX and RX, then only the attenuator is required. In any case, the overhead of the BIT circuitry is below 10% of the complete transceiver, which is efficient. However, the loopback BIT cannot be executed on-line; it requires a dedicated test mode during production testing or self-checks during times when the transceiver is idle.

The main benefit of the loopback technique is that a BER test is the most important metric, which is only low when all components function properly. This property makes loopback very attractive for fast pass/fail production testing and quick self-checks during in-field use, especially when few or no off-chip test resources are available. For example, a loopback test for the on-wafer production test stage was presented in [27].

A drawback of early loopback implementations is the lack of information regarding failure causes and fault locations. In response, one proposed variant [28] involves more computations in the digital baseband processor to determine the spectral content of the received bits and to use the data for estimation of receiver/transmitter nonlinearity specifications. Alternatively, power detectors could be placed at critical nodes to extract block-level gain and 1 dB compression point measurements. Or, similarly, statistical sampling blocks were placed along the

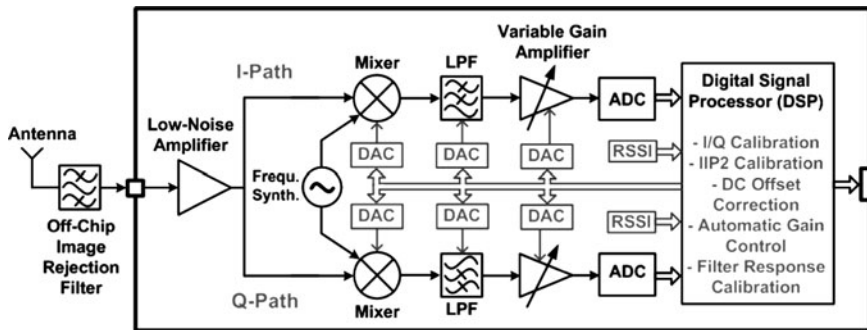


Fig. 2.7 Transceiver with digital monitoring and tuning of analog blocks

signal path in [29]. These blocks produce digital bitstreams for analysis of fault locations. In general, inclusion of auxiliary circuitry during a loopback test increases the observability of faults, but with the associated trade-offs that have been discussed for on-chip measurement circuitry in Sect. 2.2.2.

2.2.4 Digital Performance Monitoring with Analog Compensation

A BIT approach for complex transceiver chips that has become increasingly popular in recent years is depicted in Fig. 2.7. It incorporates accurate digital monitoring and I/Q mismatch correction in the baseband processors as well as a few analog observables such as outputs from received signal strength indicators (RSSIs) or DC control voltages of blocks that give some insights into their operating conditions. A significant aspect is that many analog bias voltages for RF front-end and baseband circuits are generated with digital-to-analog converters (DACs). These DACs are utilized for coarse adjustments at start-up in order to compensate for PVT variations. They also reduce DC offsets in the analog circuits to prevent saturation of internal nodes due to large gains in the receiver. Thus, more mismatches can be tolerated because of the capability to counteract them.

Combined digital monitoring/calibration with analog compensation DACs has been reported in publications describing industrial transceivers. Some examples are:

- Single-chip GSM/WCDMA transceiver in 90 nm CMOS [30], Freescale, 2009
 - DC offset, I/Q gain & phase, IIP2 calibration in the digital signal processor
 - 6-bit DACs for analog compensation
- 2.4 GHz Bluetooth Radio in 0.35 μm CMOS [31], Broadcom, 2005
 - Bias networks with digital settings for LNA, mixer, filter

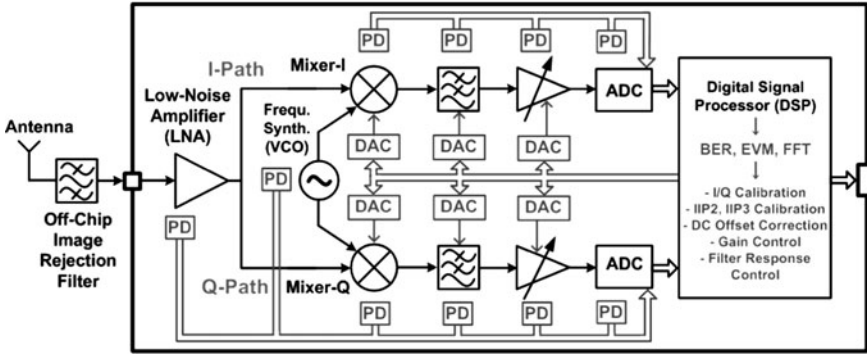


Fig. 2.8 Transceiver with digital monitoring, analog measurements, and tuning

- Tuning patent (US 7,149,488 B2); RSSIs & digital block-level bias trimming
- 2.4 GHz WLAN transceiver in 0.25 μm CMOS [32], MuChip, 2005
 - Baseband I/Q gain and phase calibration
 - Extra analog mixer & peak detector
- 5.15–5.825 GHz WLAN transceiver in 0.18 μm CMOS [33], Athena, 2003
 - Digital I/Q mismatch correction
 - Multiple internal loopback switches for self-calibration in test mode
 - 8-bit DACs for DC offset minimization after mixers and filters

2.2.5 Combined Digital Monitoring, Analog Measurements, and Tuning

The circuit-level research projects discussed in the following sections are based on the hybrid analog/digital approach in the previous subsection. One goal is to improve fault observability and calibration effectiveness by adding more measurement circuitry in the analog segments to provide data that can become part of the system-level calibration routine. Information from measurements can be used for block-level tuning prioritizations and optimizations, leading to shorter start-up routines and convergence times of algorithms. Figure 2.8 portrays the envisioned transceiver with enhanced analog measurements, where power detectors (PD) measure gains along the analog chain [17–20]. Power gain and linearity measurements through temperature sensing are explored in Chap. 5. In contrast to conventional power detectors, temperature sensors do not physically come in contact with the CUT and thus avoid loading effects.

Another aspect of comprehensive system-level self-calibration is that the analog circuits must have tunable or programmable elements, meaning that “knobs” to adjust performance parameters must be identified. Progress towards more analog features for detection of process parameter shifts and performance degradations is also beneficial because detection and tuning in the analog domain is often faster than the digital counterpart. Hence, start-up routines could be improved with added analog tuning features. One tool to do so is the analog mismatch reduction scheme in Chap. 6. Current trends show that the conglomerate of analog and digital techniques is crucial for effective built-in tests of complex single-chip systems, motivating the continued development of BITs and digitally controllable analog circuit blocks. Pros and cons of the aforementioned self-test and calibration concepts are recapped in Table 2.2.

2.2.6 High-Volume Manufacturing Testing

A production test strategy for transceiver systems-on-a-chip has recently been proposed in [34] to address cost savings through the use of soft specification limits based on statistical parameter distributions in combination with a defect-oriented test approach that enables low-cost testing using less accurate equipment or built-in circuitry. Such a test strategy would open doors for positive impact of the circuit-level adjustment features from this research on product yields. Since the suggested approach in [34] involves crude and fast tests around the acceptable minimum and maximum specification limits for a given parameter, digital programmability in the analog blocks makes retesting with fast on-chip performance tuning possible. Therefore, in reference to Fig. 2.1, self-calibration leads to narrower parameter distributions and thus higher production yields [34].

The on-chip temperature sensor in Chap. 5 extracts the gain and linearity information that conventional power detectors [17–20] for built-in testing provide. Since such on-chip sensors generate DC output voltages, they simplify production testing by avoiding RF outputs requiring well-designed impedance-matched interfaces with the automatic test equipment (ATE). Furthermore, RF measurements drive up the production test cost and are undesirable in multi-site (parallel) testing setups due to the limited number of RF channels on the ATE [35]. Since reading out DC voltages with on-chip multiplexers is more practical than routing high-frequency signals, built-in test and calibration typically reduces the number of I/O pads, thereby decreasing die sizes.

2.2.7 Analog Tuning “Knobs”

Individual blocks are tuned as part of the system-level calibrations summarized in this chapter, for which diverse mechanisms can be used depending on the specific

Table 2.2 Comparison of transceiver built-in testing and calibration techniques

Approach	Typical applications	Advantages	Disadvantages
Digital correction and calibration (Sect. 2.2.1)	I/Q mismatch calibration	High accuracy	Large variations in the analog front-end gain or linearity cannot be corrected (e.g. saturation of analog stages from DC offset amplification)
	Digital dynamic offset compensation	No measurement circuitry in the analog front-end that could load the signal path	
	System-level performance measurements (BER, FFT, EVM) with external test input or training symbols during normal operation	Well-suited for background calibration	Convergence times are longer (millisecond range). Converge times increases with PVT variation severity
		Digital BIT circuit performance is robust to PVT variations	Adaptive optimization of analog circuits is not possible because failure cause information is not available
Analog measurements and tuning (Sect. 2.2.2)		Low area and power overhead (when the DSP is on the chip)	Increased power and die area due to analog BIT circuitry
		Direct correction of analog blocks with control voltages	
	I/Q mismatch calibration in image-reject receivers	Fast settling times	BIT circuitry is connected to CUTs and failures can impact the main signal path
	Block-level characterization and tuning	Typically suitable for background calibration	
Loopback Testing (Sect. 2.2.3)	Dedicated transceiver front-end chips without on-chip digital resources	The only option when the digital baseband processor is on a different chip	Intensive design efforts (BIT circuitry implementation is significantly different, depending on transceiver types, applications, and accuracy requirements.)
	Production testing	Can be applied to high-frequency blocks	No or limited data about fault locations unless combined with analog measurement circuits
	Quick self-tests when the transceiver is idle	The most important system-level parameter is verified: bit error rate performance	Not suitable for on-line calibration (transceiver must be idle and in test mode)
		Fast verification of all on-chip blocks	
		Low area and power overhead for BIT circuits	

(continued)

Table 2.2 (continued)

Approach	Typical applications	Advantages	Disadvantages
Combined Digital Performance Monitoring and Analog Compensation		Analog compensation overcomes large PVT variations and reduces design margin requirements	Limited insights into block-level performance Complex calibration algorithms
		Front-end circuitry adjustments for deficiencies that cannot be corrected in the digital domain (transistors in unacceptable operating region due to process variations, low SNR from diminished front-end gain, amplified DC offsets in analog circuits that saturate internal nodes or the ADC input)	
	(Sect. 2.2.4)	I/Q mismatch calibration Analog dynamic offset compensation to prevent saturation Coarse start-up calibrations Production testing and on-line calibration	Solutions are developed specific to the transceiver under test Analog circuits must be programmable
Combined Digital Monitoring, Analog Measurements, and Analog Compensation		Highest detection capability of faults and performance shifts on the block-level and system-level	Area and power overhead for measurement circuitry
		Block-level optimization as part of system calibration algorithms	Complex calibration algorithms
	(Sect. 2.2.5)	Well-suited for background calibration	Intensive design efforts (BIT circuitry implementation is significantly different depending on transceiver types, applications, and accuracy requirements.)

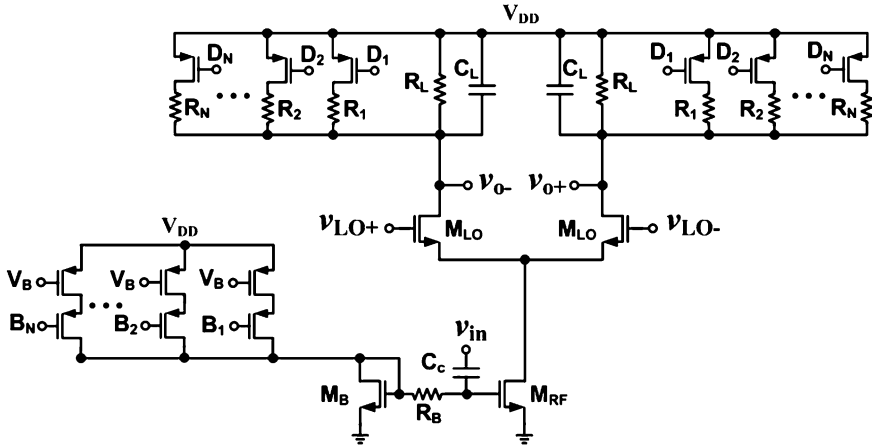


Fig. 2.9 Tuning of mixer gain ($B_1 \dots B_N$) and 2nd-order nonlinearity ($D_1 \dots D_N$)

circuit and its application. For instance, the gain of the RF transconductor in [30] has 5-bit digital gain programmability by selectively activating a number of transconductance elements that are connected in parallel. Alternatively, the transconductance values of the baseband filter in [33] are tuned by adjusting bias voltages with 8-bit DACs. Additionally, the receiver path in [33] contains 8-bit current-steering DACs to cancel DC offsets at the output of the mixing stage. Digital correction of I/Q gain mismatches can also be carried out immediately after the down-conversion by generating the bias currents for the mixers in the I and Q paths with separate current sources consisting of multiple elements [36]. This is visualized for a single-balanced mixer in Fig. 2.9, where control bits $B_1 \dots B_N$ set the conversion gain. Second-order nonlinearities due to mismatches in the mixer can be reduced as well with load resistors that are comprised of multiple parts and switches [36], which enables mismatch compensation by setting the optimum resistor value for each branch at the mixer output with digital control bits $D_1 \dots D_N$. Digitally programmable resistors have also been employed for enhancement of third-order nonlinearities in transconductance-capacitor baseband filters, provided that a linearization scheme with dependence on resistors is applied such as the one proposed in [37].

Circuit-level tuning methods have also been reported to recover from process variations of passive components that influence the frequency response in the RF front-end. For instance, Fig. 2.10 shows how, as proposed in [21], the input impedance matching network of a conventional inductively degenerated common-source LNA can be digitally tuned by designing it with a gate inductor L_g that is tapped at several points by closing one of the switches $S_1 \dots S_N$ to optimize the input impedance matching. However, the on-resistance of the switch in the signal path must be carefully considered during the design in order to minimize its effect on the quality factor of the input matching network as well as on the noise and linearity performance. An additional tuning feature is the varactor C_{var} in the

Fig. 2.10 Tuning knob examples for LNAs: input impedance matching ($S_1 \dots S_N$), center frequency (C_{var}), gain (V_T)

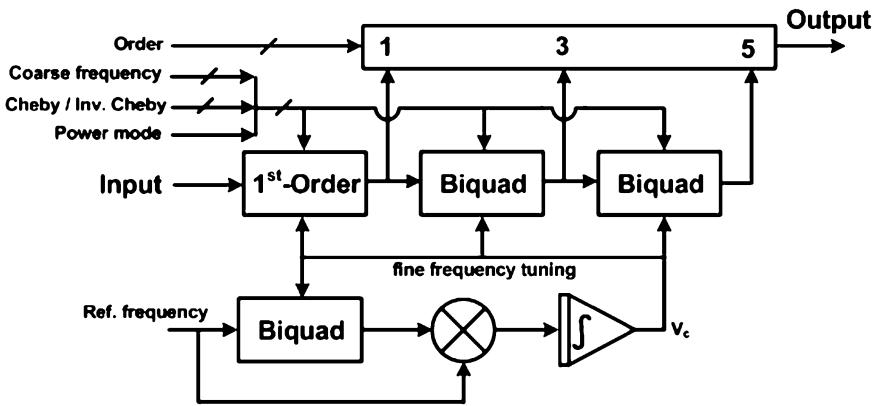
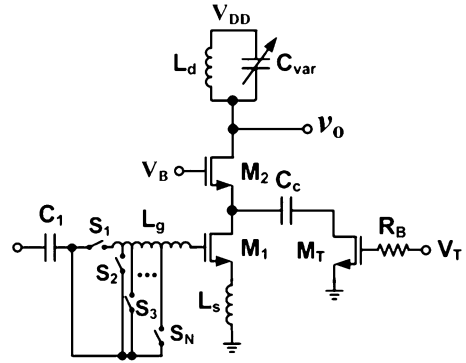


Fig. 2.11 Reconfigurable and tunable active-RC filter example

inductor–capacitor tank, which can be used to adjust the self-resonant frequency according to [38]. Finally, Fig. 2.10 also displays the gain adjustment method from [39]: the auxiliary transistor M_T is employed as variable resistor that diverts signal current to the AC ground instead of the output, modifying the LNA gain while the LNA DC bias remains unaffected thanks to the capacitor C_c .

Generally, baseband circuits allow for more tuning and reconfiguration compared to RF circuits because of the loading effects from parasitic capacitances have less impact at lower frequencies and more switches can be included in the signal path. For example, Fig. 2.11 shows the block diagram of the reconfigurable active-RC filter presented in [40], which can realize Chebyshev and Inverse Chebyshev filter functions with orders ranging from 1 to 5. Such reconfigurability enables design reuse as well as adjustable power consumption (3–7.5 mW in the discussed example) according to the filter requirements. Moreover, the design in [40] permits filter cutoff frequency tuning by two means that are displayed in Fig. 2.12: coarse tuning with digitally-controlled capacitors (switches S_0 – S_2), and continuous fine tuning with an analog control voltage (V_C).

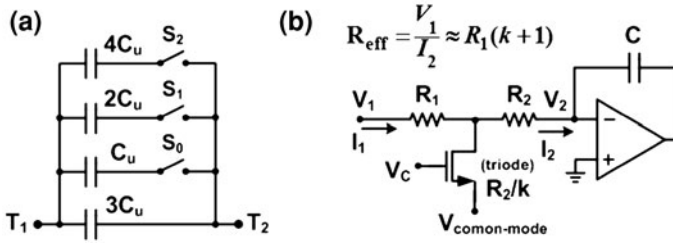


Fig. 2.12 Filter cutoff frequency tuning with adjustable elements: **a** coarse tuning with programmable capacitors, **b** fine tuning with continuous impedance multipliers

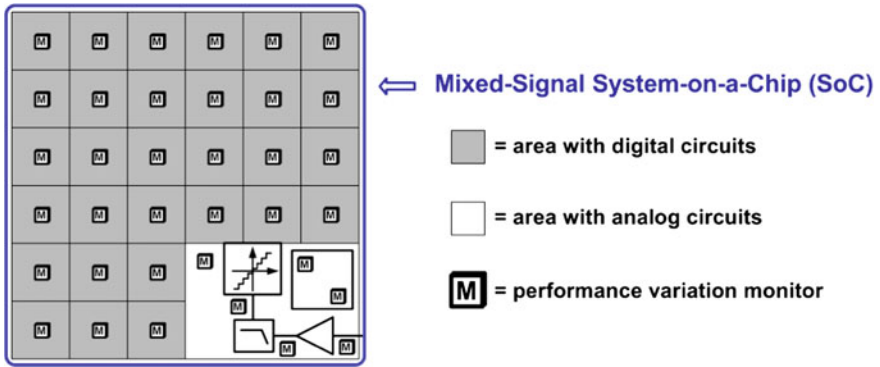


Fig. 2.13 Partitioned die with on-chip variation and performance monitoring

2.2.8 Variation-Aware Design of Digital Circuits

The purpose of this subsection is to distinguish the variation-aware design approaches for entirely digital SoCs from those for mixed-signal SoCs. Both analog and digital variation-aware design approaches require on-chip PVT monitors or measurement circuits. As visualized in Fig. 2.13, a die can be divided into many partitions to detect within-die variation, where each section contains at least one local monitoring circuit. For digital systems, variation monitors have been reported with features such as ring oscillators or delay lines for speed assessments [41–44] and temperature sensors for power density management [45–48]. As the levels of integration and number of processor cores increase (e.g. 80 cores in [49]), the adaptive methods will become more effective when the number of partitions with local PVT monitors is also increased. Nevertheless, the die area of the monitors and routing must be minimized to avoid excessive fabrication cost.

In microprocessors and other digitally-intensive systems it becomes increasingly popular to manage on-chip power dissipations and temperatures using numerous variable supply voltages or clock frequencies for different sections

(cores) on the die, such as in [50–52]. These techniques directly benefit from the information provided by the distributed placement of the sensors with sensitivity to static and dynamic power.

A major advantage of variation-sensing approaches for on-chip calibration of circuits is the enhanced resilience to the process and environmental variations that are presently creating yield and reliability challenges for chips fabricated with widely used CMOS technology. Since the threshold voltage is a significant process variation indicator for analog [53, 54] and digital circuits [41, 55], there are existing methods to monitor its statistical variation [8, 56]. In digital sections, the local operating frequency/speed measurements supplied by the variation monitors is also valuable information in adaptive body bias methods and other approaches to cope with worsening within-die variations in CMOS technologies [57–60]. In digitally-intensive systems, the extracted information that represents local on-die variations is sufficient to enable on-chip power and thermal management techniques by applying variable supply voltages or clock frequencies in the different sections (cores) [50–52, 61]. In general, the continued enhancement of on-chip local variation-sensing capabilities to assess the digital performance indicators will allow more reductions of variation and aging effects [45]. To achieve variation-resilient analog circuits in mixed-signal SoCs, the variation monitors are typically placed directly next to analog blocks as indicated in Fig. 2.13 because the information about local parameter variations is not sufficient to predict performance. As elaborated throughout this book, the need to directly extract critical performance indicators for individual analog blocks can be addressed with dedicated sensors. This difference generally leads to more specialized and complex measurement and calibration procedures compared to the digital counterparts.

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