Preface

I started working on 3D IC and through-silicon-via (TSV) in 2001 when I first joined Georgia Tech. As a young faculty and a researcher, my mission was to find a topic that I can devote myself onto for many years to come and promises high risk and high return. Die stacking was not a new idea in 2001. But, the simple idea of stacking individual dies and connecting them using vias that vertically penetrate the whole die – the term TSV did not exist or widely accepted back then – made a lot of sense to me. The benefits were very obvious: shorter interconnects, shorter interconnects, and shorter interconnects (and then smaller footprint).

As many of the readers of this book are very well aware, interconnects are a huge headache in modern (and future, too) VLSI circuits and systems. Many researchers worldwide have been struggling everyday with interconnect-related issues. So, the moment you hear that interconnect lengths will reduce naturally and significantly, you begin to smile at its related benefits: higher performance, lower power consumption, fewer metal layers used, etc. And yes, extreme memory bandwidth for the architects. No, I did not forget about the cost saving for System-On-Chip (SOC) developers because they do not have to integrate all those mixed signal components into the same die!

Well, things have not exactly been the way everyone expected. Despite the huge volume of work and success stories on materials and manufacturing research and development, efforts in architecture, design, and CAD tools have been lagging behind. People have encountered electro-thermo-mechanical reliability issues associated with TSVs, and testing became highly challenging and expensive. Most of all, the killer application that will justify the huge initial investment on the manufacturing lines has not been identified until recently.[1] In the meantime, some have turned their attention to "2.5D integration," where TSVs are not used in the dies but in an interposer (silicon or glass) to integrate components mounted on it.

[1]Many agree that wide-I/O 3D DRAM for mobile applications will be the first mainstream product that commercializes TSVs.

This book came out of the effort during the last decade (2001–2012) of 3D IC design research and development at the Georgia Tech Computer-Aided Design (GTCAD) Laboratory, with more focus on the last 4 years (2009–2012). The scope of our research has expanded from physical design automation to architecture, modeling, pathfinding, and validation. We also have developed a real 3D IC that stacks one tier of 64 general-purpose cores and another tier of SRAM memory. Through this effort, we worked on the entire spectrum of design and testing for this test chip: architecture, layouts, CAD tools, package, board, and testing infrastructure. We also began to look beyond the conventional TSV-based 3D ICs and started investigating monolithic 3D IC design. The 20 chapters included in this book are organized to reflect this evolution. The first part of this book contains six chapters on design issues and solutions for high performance and low power 3D ICs.

- In Chap. 1, we study the pros and cons of two distinct ways to place through-silicon-vias (TSVs) in gate-level 3D layouts, namely, regular and irregular styles. We also study the area, wirelength, timing, and power overhead of TSVs in 3D IC layouts.
- In Chap. 2, we study how to build a Steiner tree for a given set of points in multiple dies. We also study how to relocate TSVs in a given set of Steiner trees to alleviate thermal hotspot issues.
- In Chap. 3, we study how to add buffers to a 3D net that connects gates in multiple dies in 3D IC to optimize signal delay and slew.
- In Chap. 4, we study how TSVs can be used to build a clock tree for 3D IC to reduce the total power consumption while minimizing clock skew.
- In Chap. 5, we study the issues in power delivery network design for 3D ICs and the impact of power/ground TSV usage on power supply noise.
- In Chap. 6, we study how to build a clock tree for 3D IC so that it can be used to deliver clock signal during pre-bond and post-bond testing.

The second part of this book contains 3 chapters on design-for-electrical-reliability for 3D ICs.

- In Chap. 7, we study the TSV-to-TSV coupling issues and investigate various ways to alleviate the associated problems.
- In Chap. 8, we investigate the current crowding problem at the wire-to-TSV junction in the power delivery network and its impact on IR-drop.
- In Chap. 9, we study the electro-migration failure mechanisms in TSVs caused by the current density, mechanical stress, and thermal gradient issues in 3D ICs.

The third part of this book contains 3 chapters on design-for-thermal-reliability for 3D ICs.

- In Chap. 10, we study thermal-aware architectural floorplanning for 3D IC and its impact on other metrics such as area, wirelength, and performance.
- In Chap. 11, we study gate-level placement techniques to alleviate thermal problems in 3D IC designs.

- In Chap. 12, we investigate the issues in codesign and co-analysis of thermal, power delivery, and performance targeting a 3D IC that employees micro-fluidic channels for cooling.

The fourth part of this book contains 5 chapters on design-for-mechanical-reliability for 3D ICs.

- In Chap. 13, we study the full-chip analysis of mechanical stress in 3D IC designs caused by the coefficient of thermal expansion (CTE) mismatch between TSV and silicon substrate.
- In Chap. 14, we study the impact of mechanical stress on device mobility and full-chip timing variations in 3D IC.
- In Chap. 15, we extend the full-chip study in Chap. 13 to investigate the impact of package elements on the mechanical reliability of the entire 3D chip/package system.
- In Chap. 16, we study the impact of chip/package mechanical stress on device mobility and full-chip path delay variations.
- In Chap. 17, we study the impact of TSV-induced mechanical stress on crack growth between TSV and its liner (= interfacial crack).

The last part of this book covers other topics on 3D IC design.

- In Chap. 18, we study the density, performance, and power benefit of monolithic 3D integration, where NMOS and PMOS are placed in two different tiers and connected with extremely small monolithic inter-tier vias (MIVs).
- In Chap. 19, we study the impact of TSV scaling on the area, wirelength, timing, and power quality of 3D designs done at the current and future technology nodes.
- In Chap. 20, we study the design, manufacturing, and testing of the 3D-MAPS (massively parallel processor with stacked memory), where one tier of 64 general-purpose cores and another tier of SRAM memory are bonded face to face for core-to-memory communication and utilize TSVs to communicate with the package.

These topics are mostly based on our work published at premier design and CAD conferences such as IEEE International Solid-State Circuits Conference (ISSCC), IEEE Custom Integrated Circuits Conference (CICC), ACM Design Automation Conference (DAC), IEEE International Conference on Computer-Aided Design (ICCAD), etc., during last 4 years (2009–2012).

This book is primarily intended for circuit designers and CAD tool developers from both industry and academia who are interested in learning about what the researchers at the Georgia Tech Computer-Aided Design (GTCAD) Laboratory and their colleagues have experienced from designing and validating high performance, low power, and reliable 3D ICs. However, a significant portion of this book is also based on our collaboration with people from other areas such as manufacturing, materials, testing, software applications, and computer architecture. This book discusses the needs and outcomes of such collaborations. The materials presented

in this book are also based on our close collaboration with industry partners through funded research projects from Intel, IBM T. J. Watson, Samsung, Qualcomm, Mentor Graphics, and Cadence.

Despite our effort, this book may still contain errors. We will be truly grateful if you could help us correct those mistakes. Please send any report of bugs, misprints, and other errata to me at limsk@ece.gatech.edu. In the meantime, please visit our website for other resources and errata: http://users.ece.gatech.edu/limsk/3d-book.

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