

Chapter 2

Digital-to-Analog Converters

In this chapter, the concept and performance specifications of digital-to-analog converters (DACs) are reviewed. Different DAC architectures and physical implementations are introduced. Recently published state-of-the-art DACs are summarized to show the performance limitations.

2.1 Introduction to DACs

In this section, the general function and applications of digital-to-analog converters (DACs) are briefly discussed.

2.1.1 Time Domain Response

In electronics, a Digital-to-Analog Converter (DAC) is a device that converts a finite-precision digital-format number (the input, typically a finite-length binary-format number) to an analog electrical quantity (such as voltage, current or electric charge). Nowadays, with the development of digital technologies, for easy storage and processing, most analog signals are digitized by Analog-to-Digital converters (ADCs) and are processed by digital signal processors (DSPs) [1]. However, our perceptual world is still analog so that the digital signal has to be converted back into analog domain such that, for example, the data can be transmitted with high signal quality in communication systems or a human being can hear a music or watch a video. Therefore, a DAC is an essential device in scientific research, industry control and people's daily life.

Figure 2.1 shows a simplified signal chain with a DAC in a wireless transceiver. The input information to a DAC can come from two sources: the digital signal processor (DSP) or the Analog-to-Digital converter (ADC). The difference between

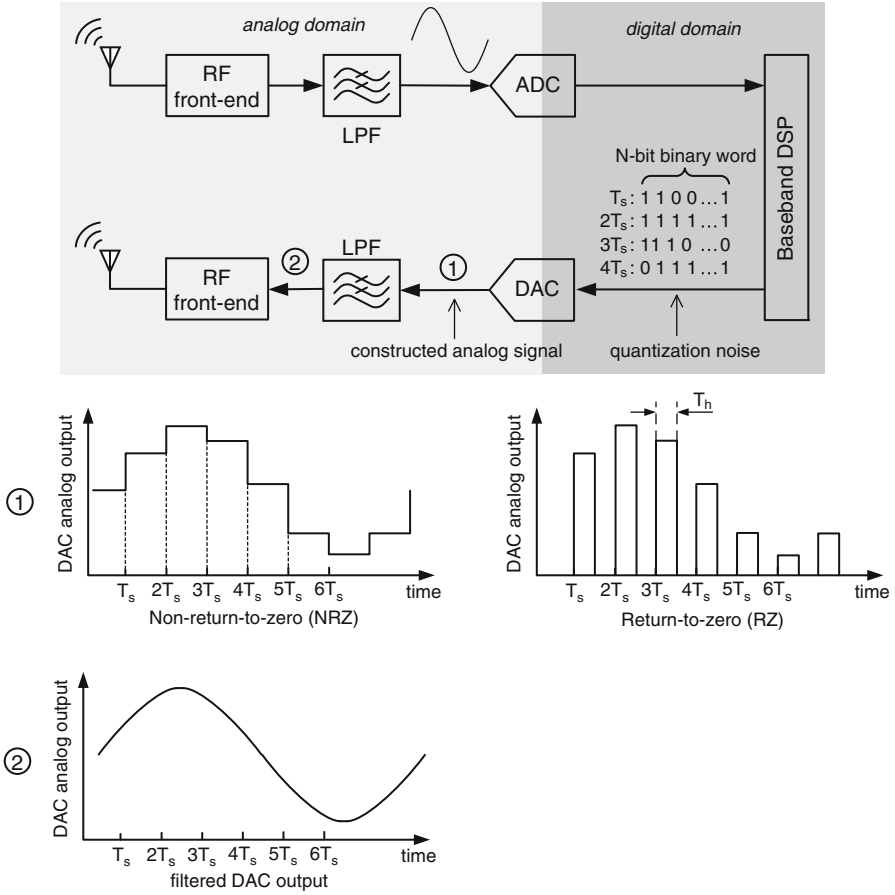


Fig. 2.1 DAC in a wireless transceiver

these two sources is that the information from the ADC is generated by digitizing an analog signal, while the DSP may directly generate this information. In order to construct an analog signal, there are two basic types of DAC output format: non-return-to-zero (NRZ) and return-to-zero (RZ). As shown in Fig. 2.1, for NRZ, the DAC updates its analog output according to its digital input at a fixed time interval of T_s and holds the output, where T_s is called updating or sampling period. For RZ, after updating the output at each time interval T_s , the DAC holds the output only for a certain time (T_h), then goes back to zero. In both cases, the DAC's output is held for a certain time T_h , where $0 < T_h \leq T_s$, known as zero-order-hold (ZOH). Compared to NRZ DACs, RZ DACs have a lower output power due to return-to-zero, e.g. half power when $T_h = 0.5T_s$. The output of a DAC is typically a stepwise or pulsed analog signal and can be low-pass filtered to construct the required analog signal.

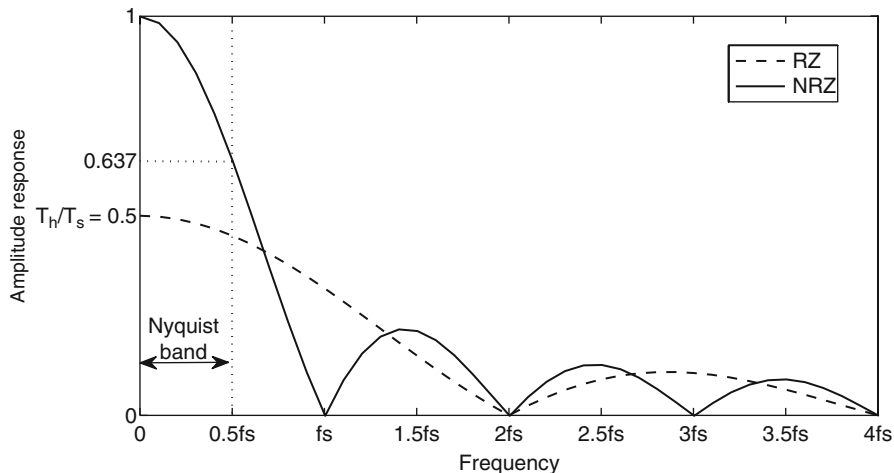


Fig. 2.2 Magnitude of frequency responses of ideal NRZ and RZ DACs

From a simple point of view, the DAC performs the reverse operation of the ADC. However, it should be noticed that unlike the ADC, the DAC itself does not add any quantization noise because the quantization noise is already generated before the DAC. This is due to the finite quantization levels of the ADC or the finite word length of the DSP, i.e. finite precision. The word length of the binary digital input of the DAC, i.e. N-bit, is called the number of bits. Though the DAC does not generate quantization noise, it will most likely generate conversion errors due to the non-ideality of the DAC. The conversion errors are often input-signal related and generate harmonic distortion. The relation between the conversion errors and the performance of DACs will be discussed in Chap. 3.

2.1.2 Frequency Domain Response

The magnitude of the frequency responses of ideal NRZ and RZ DACs are shown in Fig. 2.2, where the RZ DAC example has a holding time (T_h) of a half of the sampling period (T_s). $f_s (= \frac{1}{T_s})$ is called updating rate or sampling frequency. The frequency responses are sinc-shaped because of the zero-order hold (ZOH) function in the DAC's output, and the shape is dependent on $\frac{T_h}{T_s}$. As seen, in the Nyquist band, the RZ DAC has a larger signal attenuation than the NRZ DAC. Compared to the NRZ DAC, the maximum signal loss for the RZ DAC is $|20 \log_{10} \frac{T_h}{T_s}|$ dB at DC, e.g. 6 dB power loss at DC for $\frac{T_h}{T_s} = 0.5$. However, in the Nyquist band, a RZ DAC has a more flat magnitude response than a NRZ DAC. In this example, the magnitude drop is 3.9 dB for NRZ and 0.9 dB for RZ at $0.5 f_s$, respectively. For some applications where a flat magnitude response is required in the Nyquist band, an anti-sinc digital filter can be placed before the DAC to compensate the sinc attenuation.

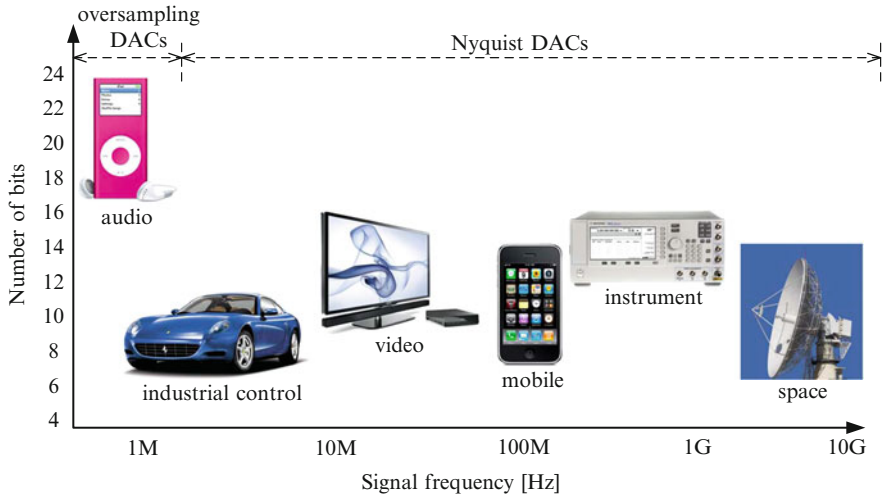


Fig. 2.3 Application examples of digital-to-analog converters

2.1.3 Applications

Figure 2.3 shows a few typical applications of DACs. Oversampling DACs are dominant in audio applications, where 16- to 24-bit is required in a kHz signal frequency range. This work focuses on Nyquist DACs for high signal frequencies (MHz- to GHz-range). This kind of DAC is widely used in high-speed instruments and telecommunications.

2.2 Performance Specifications

In this section, static and dynamic performance specifications of DACs are briefly introduced.

2.2.1 Static Performance (DC) Specifications

Static performance specifications introduced below are used to evaluate the DC performance of DACs.

2.2.1.1 Offset and Gain Errors

The offset error of a DAC is defined as the deviation of the linearized transfer curve of the DAC output from the ideal zero. The linearized transfer curve is based on the

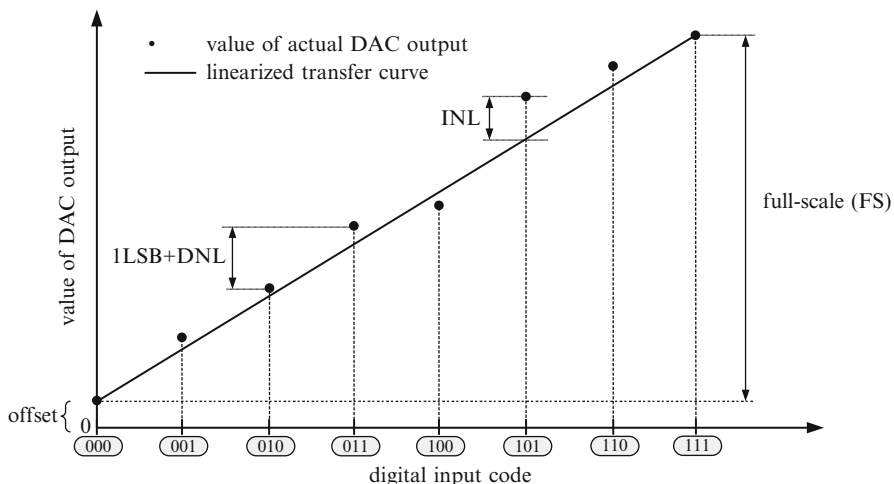


Fig. 2.4 DC specs of a DAC

actual DAC output, either a simple min-max line connecting the minimal and the maximal DAC output value or a best-fit line of all the output values of the DAC. A 3-bit DAC example is shown in Fig. 2.4 with a simple line as the linearized transfer curve. The difference between the minimal value and the maximum value of the linearized transfer curve is called full-scale (FS) output range. The error between 1 and the ratio of the actual full-scale range over the ideal full-scale range is called the gain error (in percentage). The offset can be easily compensated by a DC auxiliary DAC and the gain error can be corrected by adjusting the full-scale range settings. Since the offset and gain errors do not introduce non-linearity, they have no effect on the spectral performance of DACs.

2.2.1.2 Integral Non-linearity (INL)

As shown in Fig. 2.4, integral non-linearity (INL) is defined as the deviation of the actual DAC output from the linearized transfer curve at every code input. The INL_{max} is the worst value of the INL, as shown in (2.1), where N is the number of bits of the DAC. As seen, the INL directly reflects the static linearity of the DAC.

$$\begin{aligned}
 INL(code) &= out_{dac}(code) - (offset + 1LSB_stepsize \times code), \\
 \text{where } 1LSB_stepsize &= \frac{\text{full-scale DAC output}}{2^N - 1} \\
 INL_{max} &= \max(INL(code)), \text{ code}=0 \sim \text{full-scale digital input code} \quad (2.1)
 \end{aligned}$$

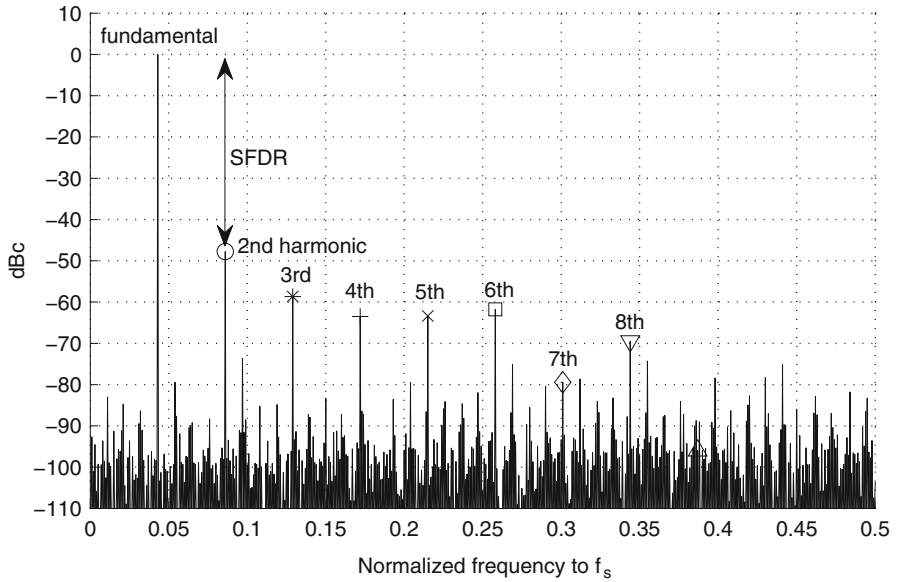


Fig. 2.5 An example of DAC output spectrum

2.2.1.3 Differential Non-linearity (DNL)

As shown in Fig. 2.4, the differential non-linearity (DNL) is the deviation of the actual step size from the ideal step size (1LSB) between any two adjacent digital input codes. The DNL_{max} is the worst case of the DNL.

$$DNL(code) = out_{dac}(code) - out_{dac}(code - 1) - 1LSB_{stepsize}$$

$$DNL_{max} = \max(DNL(code)), \text{code}=1 \sim \text{full-scale digital input code} \quad (2.2)$$

2.2.2 Dynamic Performance (AC) Specifications

Dynamic performance specifications are used to evaluate the AC performance of DACs. These parameters are very important in many applications, such as in high-speed communication systems which is one of the targeted applications of this work.

2.2.2.1 Single-Tone SFDR/THD/NSD/SNR/SNDR

Figure 2.5 shows an example of the output spectrum of a Nyquist DAC with a single-tone sine-wave input. The frequency axis is normalized to the sampling frequency (f_s). Several parameters are defined in the frequency domain to evaluate the dynamic performance of the DAC.

Spurious-free Dynamic Range (SFDR):

The ratio, in decibels, between the power of the fundamental component of the constructed output sine wave and the power of the largest spurious tone observed (excluding the DC component) in the frequency domain. Typically a high SFDR is required to suppress spurious emissions, especially in communication systems.

Total Harmonic Distortion (THD):

The total power of all harmonics of the reconstructed output sine wave. The THD can be expressed in decibels if it is relative to the power of the fundamental component of the constructed output sine wave.

Noise Power Spectral Density (NSD):

The power density of the noise at the DAC's output in the frequency domain. It can be specified in dBm/Hz.

Signal-to-Noise Ratio (SNR):

The ratio of the power of the measured output signal to the integrated power of the noise floor in the Nyquist band ($[0, \frac{\text{sampling frequency}}{2}]$, except DC and harmonics). The value for SNR is expressed in decibels.

Signal-to-(Noise+Distortion) Ratio (SNDR):

The ratio of the power of the measured output signal to the integrated power of the noise floor in the Nyquist band plus the total power of the harmonics. The SNDR directly relates to the SNR and THD.

2.2.2.2 Two-Tone Intermodulation Distortion (IMD)

When a two-tone signal is applied to a nonlinear system, intermodulation distortion products are generated. Assuming the frequencies of the two tones are f_1 and f_2 ($f_1 < f_2$), the spectral components which are most close to the fundamental output tones are two third-order intermodulation distortion components $2f_1 - f_2$ (IM3_{left}) and $2f_2 - f_1$ (IM3_{right}), as shown in Fig. 2.6. Then, the IM3 is defined as the worse one between IM3_{right} and IM3_{left}. As seen, if the frequencies of the two input tones are adjacent with close spacing, the IM3 falls very close to the desired signals. This is strongly not desired since the IM3 is then very difficult to be filtered out.

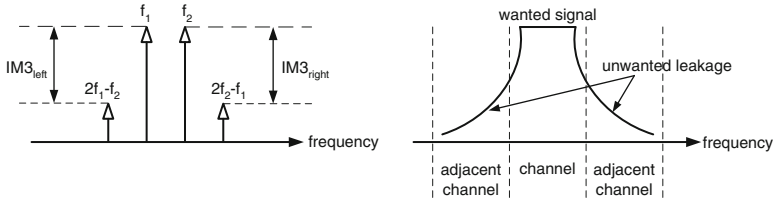


Fig. 2.6 Graphic representation of IM3 and ACLR

The adjacent channel leakage ratio (ACLR) is also used to indicate the intermodulation performance, especially in multi-channel broadband systems such as WCDMA, CDMA2000, WiMAX, LTE, etc.. It is defined as a ratio, in dBc, of the transmitted power within a desired channel to the power in its adjacent channel. It has the same generation mechanism as the intermodulation and can be related to the IMDs.

2.3 Architectures

According to different decoding schemes, DACs have three basic architectures: binary, thermometer and segmented architectures. There are also other types of architectures which are optimized for specific input signals, such as sine-weighted DACs. In this section, only basic DAC architectures for general input signals are discussed.

2.3.1 Binary Architecture

Since the input to a DAC is typically a binary digital word, the most straightforward way to implement the function of the DAC is to let every input bit corresponds to a binary-weighted element (voltage, current or charge). An example of 4-bit binary-coded DAC is shown in Fig. 2.7.

The advantage of a binary-coded DAC is that its decoding circuit and the number of switches are minimal, i.e. its chip area and power consumption are small. The disadvantage is that the ratio between the least significant element and the most significant element is so large that the matching between them is difficult to be guaranteed, resulting in large DNL and INL errors. Another drawback is that if the switching of the elements are not perfectly synchronized, large glitch errors occur during input code transitions, especially when the most significant element is being switched.

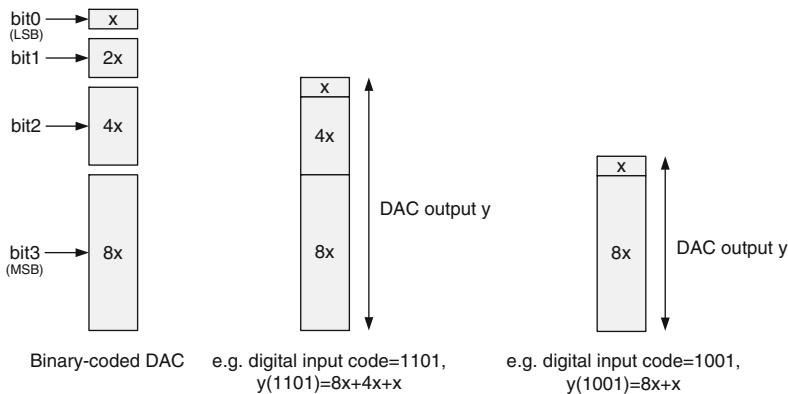


Fig. 2.7 A 4-bit binary-coded DAC example

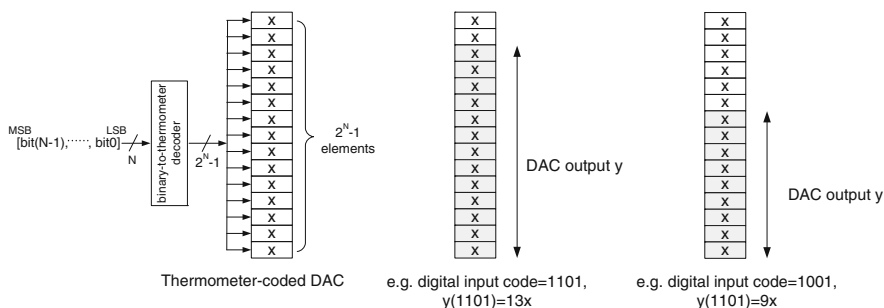


Fig. 2.8 A 4-bit thermometer-coded DAC example

2.3.2 Thermometer (Unary) Architecture

In order to overcome the drawbacks of the binary-coded DAC architecture, a thermometer-coded DAC architecture has been developed. As shown in Fig. 2.8, an N -bit thermometer-coded DAC has $2^N - 1$ unary elements. Those unary elements are switched on or off in a certain sequence according to the input digital code. Compared to the binary-coded architecture, the thermometer-coded architecture reduces the INL/DNL and glitch errors. The costs are: a binary-to-thermometer decoder is needed and lots of switches have to be synchronized. Since the area and power consumption of the decoder and switches are exponentially increasing with the number of bits, a full thermometer-coded DAC architecture is seldom used with N above 10-bit.

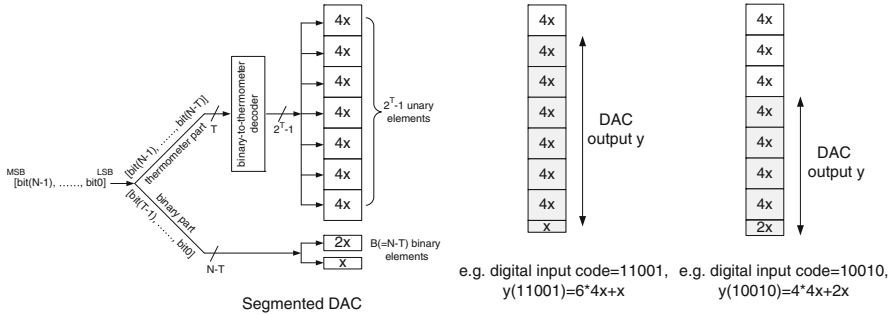


Fig. 2.9 A 5-bit 3T-2B segmented DAC example

2.3.3 Segmented Architecture

The segmented architecture is the most widely used DAC architecture since it balances the pros and cons of binary and thermometer architectures. For a segmented DAC, part of the input digital code, typically several most significant bits, are implemented as unary elements and the other part is implemented as binary elements. In the 5-bit DAC example shown in Fig. 2.9, the first three bits are implemented as a thermometer-coded sub-DAC and the last two bits are implemented as a binary-coded sub-DAC. As a result, the DAC has a 3thermometer-2binary (3T-2B) segmented architecture. How to segment the total bits into thermometer and binary parts is a trade-off between performance, area and power consumption. In a segmented DAC, the thermometer part is typically dominant in the whole performance of the DAC.

2.4 Physical Implementations

Depending on how an element is implemented, there are three basic DAC physical implementations: resistor DACs, capacitor DACs and current-steering DACs. In the following sections, examples of basic implementations of these three types of DACs and their applications are discussed.

2.4.1 Resistor DAC

Figure 2.10 shows a frequently used R-2R ladder DAC. By connecting or disconnecting the resistors, the output voltage (V_{out}) is controlled by the input binary bits. The DAC accuracy depends on the matching of the resistors. Speed and linearity are main limits of resistor type DACs due to the nonlinear resistors and the bandwidth and linearity of the output buffer.

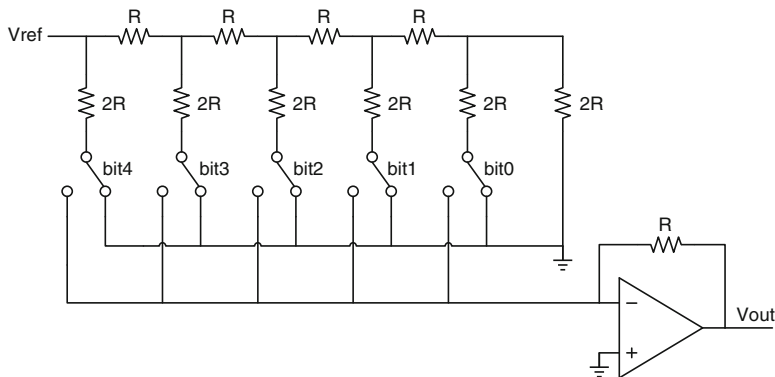


Fig. 2.10 A 5-bit R-2R ladder DAC example

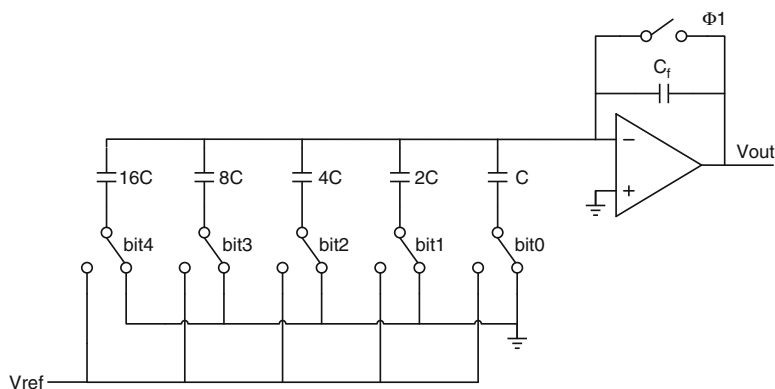


Fig. 2.11 A 5-bit switched-cap DAC example

2.4.2 Capacitor DAC

Figure 2.11 shows an example of a switched-capacitor DAC. The operation needs two phases. During phase ϕ_1 , the input capacitors are connected either to a reference voltage (V_{ref}) or to ground according to the input digital code, and the feedback capacitor is shorted. During phase ϕ_2 , all input capacitors are switched to ground and the feedback capacitor is connected around the amplifier. Based on charge conservation, the output voltage (V_{out}) is a fraction of V_{ref} which is set by the input digital code. Similar to the resistor DAC, the capacitor DAC's accuracy depends on the matching of the capacitors. Speed and linearity are also main limits of this type of DAC. The advantage of capacitor DACs is that the power consumption is quite low since only a certain charge needs to be transferred.

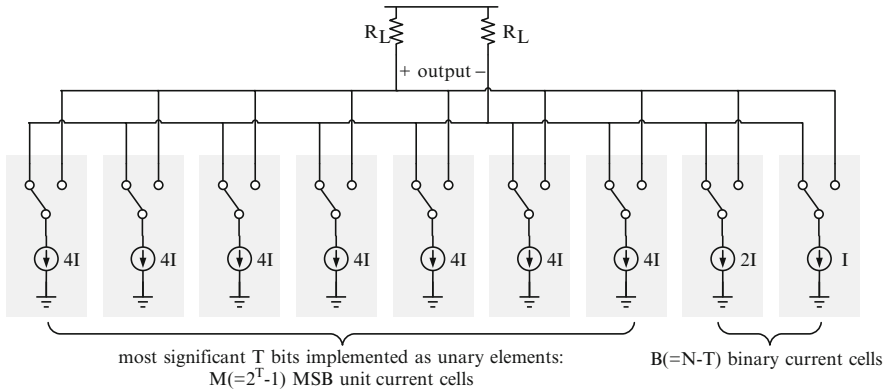


Fig. 2.12 A 5-bit 3T-2B segmented current-steering DAC example

2.4.3 Current-Steering DAC (CS-DAC)

With the rapid development of communication systems, such as Direct-Digital-Synthesis (DDS) and novel RF transceivers in new applications, high-speed and high-resolution DACs are required. In these applications, very high sampling-rate DACs, which often need to be operated at hundreds of MHz and drive a 50 ohm load, can directly generate RF/IF signals. Consequently, it is unnecessary to use traditional mixers for up-conversion. This is very suitable for multi-standard or long-term evolution applications because in this way, most of the signal processing can be done in the digital domain. The current-steering DAC is a suitable architecture for such applications, because of its intrinsic high speed and driving capability.

An example of a 5-bit 3T-2B segmented current-steering DAC architecture with a differential output is shown in Fig. 2.12. In this figure, N is the total number of bits of the DAC (for simplicity, the binary-to-thermometer decoder shown in Fig. 2.9 is not shown here). As seen, most significant T bits are implemented as unary elements, called MSB unit current cells which all provide the same current. The remaining $B (=N-T)$ bits are implemented as binary elements, called binary current cells whose currents are binary-weighted. The current cell consists of a current source and differential switches: the current is switched to the positive output node or to the negative output node according to the input digital bits. Therefore, all current cells are acting as switched-current (SI) cells. The DAC's accuracy relies on the matching between current sources.

Since the output of a current-steering DAC is a current and has a high output impedance, it has very fast conversion speed and good intrinsic driving ability for low impedance loading. For high speed applications, a loading resistor (R_L , typically $25\Omega \sim 300\Omega$) converts the current output to a voltage. The differential output voltage swing is $2I_{FS}R_L$, where I_{FS} is the full-scale output current of the DAC. As seen, a larger loading resistor leads to a larger output voltage swing,

i.e. larger delivered power. Because the DAC output is a current and the resistor performs a linear I–V conversion, in theory, the linearity of the DAC is only determined by the linearity of the output current. Therefore, the linearity of the DAC, such as the SFDR or IM3, is independent of the output swing, as long as the linearity of the output current is not compromised by the large voltage swing, e.g. if there is not enough voltage headroom for correct current source biasing. However, in practice, due to technology limitations, the linearity of the output current can be compromised by a larger output voltage swing, so does the linearity of the DAC.

2.5 State of The Art

Table 2.1 lists the main state-of-the-art Nyquist DACs published in the last twelve years. As seen, high speed, high performance and low power are major research trends. Especially, driven by new communication applications, the DAC is moving to the RF frequency where high speed and high dynamic performance are both required. How to meet those requirements is a challenge for the DAC design and will be addressed in this work.

Figure 2.13 shows the sampling frequency of the published DACs in Table 2.1 versus the process technology. As expected, due to higher f_T , a BiCMOS or bipolar technology can achieve a much higher sampling frequency than a CMOS technology. In the same category of CMOS technology, in general, more advanced technology nodes can achieve a higher sampling frequency. However, as seen, the sampling frequencies of most of the Nyquist CMOS DACs are still in the range of 100 MHz to 1 GHz. One reason for this is that in most traditional applications, due to a low signal frequency, a high-linearity performance is typically required rather than a very high sampling frequency. With increasing signal frequency in emerging applications, a DAC with >1 GHz sampling frequency and high-linearity performance becomes very attractive [2, 12].

The SFDR of these published DACs at very low signal frequencies (near DC) versus static effective number of bits (static ENOB, based on the INL) is summarized in Fig. 2.14. As seen, most of these DACs have an 11–15 bit ENOB for their static performance, which is limited by the static matching accuracy. The SFDRs at very low signal frequencies are mostly located between 70–85 dBc, which are mainly limited by the static linearity of DACs, i.e. the INLs.

The SFDR of these DACs at high input signal frequencies (near Nyquist frequency, i.e. near half of sampling frequency, unless specified in Table 2.1) are plotted in Fig. 2.15. At tens or hundreds of MHz signal frequencies, not only static non-linearity but also dynamic non-idealities limit the DAC's dynamic performance. As seen, the SFDR at signal frequencies below 100 MHz is hardly higher than 80 dBc, and it drops pretty fast with further increasing signal frequencies. For CMOS technology, the state-of-the-art DACs achieve 60 dBc around 500 MHz

Table 2.1 State-of-the-art Nyquist DACs

Ref.	Year	Bits	INL/DNL [LSB]	fs [MS/s]	SFDR@low fi [dBc]	SFDR@high fi [dBc]	Technology	Power
[2]	ISSCC'09	12	0.5/0.3	2,900	74	60 ^a	65 nm CMOS, 2.5 V	188 mW
[3]	ISSCC'07	13	0.8/0.4	200	83.7	54.5	0.13 μ m CMOS, 1.5 V	25 mW
[4]	ISSCC'06	14	–	100	74.4	77.8	0.18 μ m CMOS, 1.8 V	150 mW
[5]	ISSCC'06	6	–	20,000	–	50 ^b	0.18 μ m SiGe, 1.8 V	360 mW
[6]	ISSCC'06	9	1/0.5	2	–	–	0.5 μ m CMOS, 5 V	0.3 mW
[7]	ISSCC'05	15	8	1,200	72	63	0.35 μ m BiCMOS, 3.3 V	6 W
[8]	ISSCC'05	12	–	1,600	62	55	GaAs, 5 V	1.2 W
[9]	ISSCC'05	12	–	1,700	64	50	0.35 μ m BiCMOS, 3 V	3 W
[10]	ISSCC'05	12	1/0.6	500	78	58	0.18 μ m CMOS, 1.8 V	216 mW
[11]	ISSCC'05	6	0.9/0.5	22,000	–	–	0.13 μ m BiCMOS, 3.3 V	1.2 W
[12]	ISSCC'04	14	1.8/0.8	1,400	–	60	0.18 μ m CMOS, 1.8 V	400 mW
[13]	ISSCC'04	10	0.1/0.1	250	74	60	0.18 μ m CMOS, 1.8 V	4 mW
[14]	ISSCC'04	14	0.65/0.55	200	85	44	0.18 μ m CMOS, 1.8 V	97 mW
[15]	ISSCC'03	16	1/0.25	400	95	73	0.25 μ m CMOS, 3.3 V	400 mW
[16]	ISSCC'03	14	0.43/0.34	100	82	62	0.13 μ m CMOS, 1.5 V	16.7 mW
[17]	ISSCC'01	12	0.3/0.25	500	75	35	0.35 μ m CMOS, 3 V	110 mW
[18]	ISSCC'00	14	0.5/0.5	100	82	72	0.35 μ m CMOS, 3.3 V	180 mW
[19]	ISSCC'99	14	0.3/0.2	150	84	50	0.5 μ m CMOS, 2.7 V	300 mW
[20]	ISSCC'99	14	0.5/0.5	60	85	75	0.8 μ m CMOS, 5 V	750 mW
[21]	ISSCC'98	10	0.2/0.1	250	71	57	0.5 μ m CMOS, 5 V	100 mW
[22]	ISSCC'98	12	0.6/0.3	300	70	40	0.5 μ m CMOS, 3.3 V	320 mW
[23]	VLSI'07	14	3.5/1	150	83	83	0.18 μ m CMOS, 1.8 V	127 mW
[24]	ESSCIRC'06	8	0.25/0.25	600	68	–	0.13 μ m CMOS, 1.2 V	2.4 mW

[25]	ESSCIRC'05	12	0.4/0.6	50	80	60	0.25 um CMOS, 3.3 V	270 mW
[26]	ESSCIRC'04	14	0.7/0.45	130	80	40	0.25 um CMOS, 3.3 V	103 mW
[27]	JSSC' 06	5	-	32,000	31	30	300 GHz ft Bipolar	4.4 W
[28]	JSSC'06	12	0.38/0.44	180	72	62	0.25 um CMOS, 3.3 V	155 mW
[29]	JSSC'03	12	0.4/0.3	320	95	45	0.18 um CMOS, 1.8 V	60 mW
[30]	JSSC'03	14	0.3/0.3	300	72	68	0.25 um CMOS, 3.3 V	53 mW
[31]	JSSC'01	10	0.2/0.15	1,000	72	61	0.35 um CMOS, 3 V	110 mW
[32]	JSSC'98	12	0.6/0.3	300	70	40	0.5 um CMOS, 3.3 V	320 mW

^a @550 MHz

^b @186 MHz

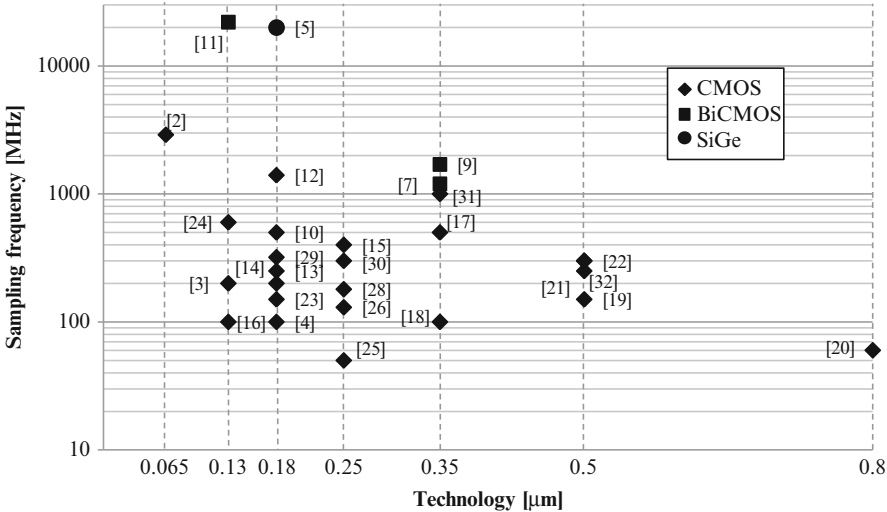


Fig. 2.13 State-of-the-art DACs: sampling frequency versus technology node

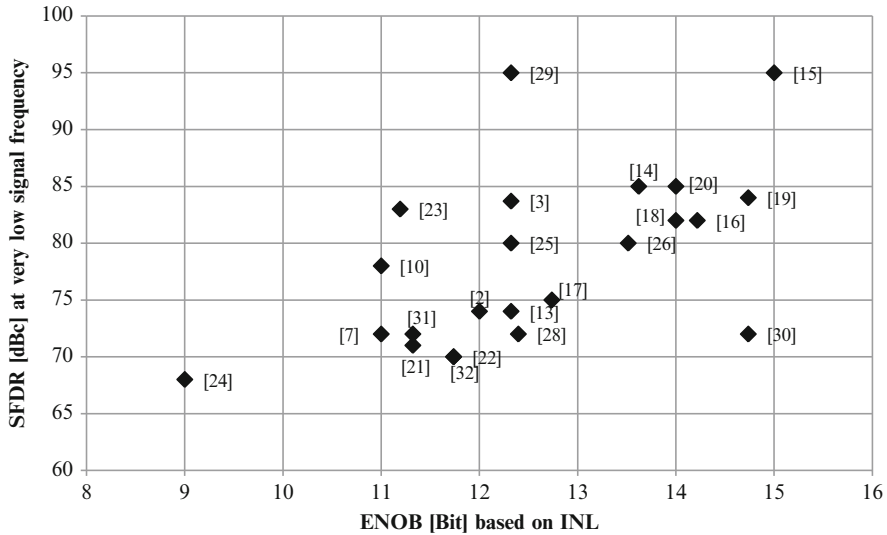


Fig. 2.14 State-of-the-art DACs: SFDR at very low signal frequencies (near DC) versus static ENOB

signal frequencies. For BiCMOS and III–V compounds technology, higher sampling and signal frequencies can be achieved, but the SFDR is still limited at 50 dBc around 1 GHz signal frequency.

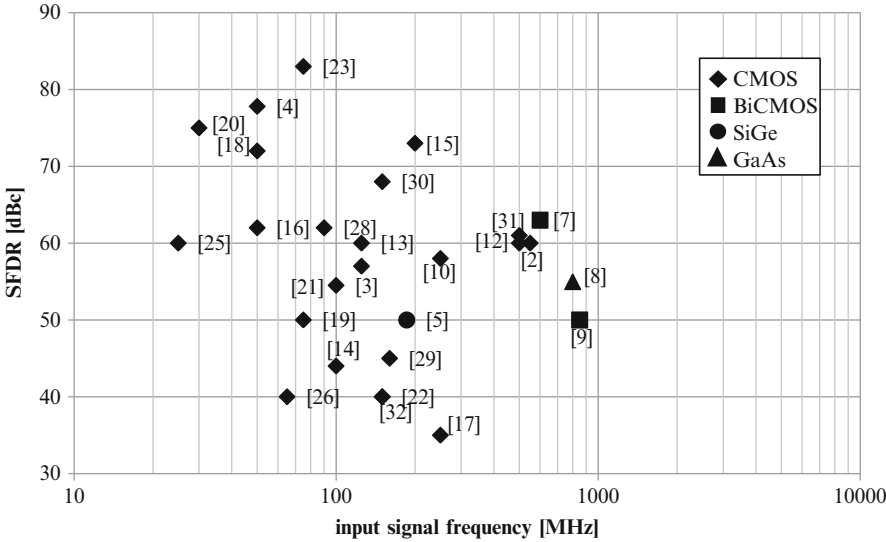


Fig. 2.15 State-of-the-art DACs: SFDR at high signal frequencies (near Nyquist) versus input signal frequency

Apparently, in order to achieve a good performance in a wide frequency range, it has to be analyzed how the DAC's static and dynamic performance are limited by various error sources. Accordingly, design techniques should be developed to overcome these design challenges. These issues are the main focus of this work.

2.6 Conclusions

In this chapter, the function and performance specifications of digital-to-analog converters (DACs) are briefly introduced. Different DAC architectures (binary, thermometer and segmented) and physical implementations (resistor, switched-cap and current-steering) are also discussed. The performance of state-of-the-art published DACs is summarized.

Due to its intrinsic high speed and driving ability, Nyquist current-steering DACs are most frequently used in high-speed, high-performance applications. Therefore, this work focuses on analysis and design techniques of current-steering DACs.

Dynamic-Mismatch Mapping for Digitally-Assisted DACs

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