

# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Growing SoC Validation Complexity	1
1.2	System-Level Validation: Opportunities and Challenges	3
1.2.1	Top-Down Design and Validation Flow	4
1.2.2	SoC Validation Approaches	6
1.2.3	Opportunities in System-Level Validation	10
1.2.4	System-Level Validation Challenges	12
1.3	A Comprehensive Approach for System-Level Validation	14
1.4	Book Organization	14
	References	15
<b>2</b>	<b>Modeling and Specification of SoC Designs</b>	<b>19</b>
2.1	Introduction	19
2.2	Modeling of Complex Systems	19
2.2.1	Graph-Based Modeling	20
2.2.2	FSM-Based Behavior Modeling	20
2.3	Specification Using SystemC TLMs	22
2.3.1	Modeling of SystemC TLM Designs	22
2.3.2	Transformation from SystemC TLM to SMV	24
2.3.3	Case Study: A Router Example	28
2.4	Specification Using UML Activity Diagrams	29
2.4.1	Graphic Notations	30
2.4.2	Formal Modeling of UML Activity Diagrams	32
2.4.3	Transformation from UML Activity Diagrams to SMV	36
2.4.4	Case Study: A Stock Exchange System	40
2.5	Chapter Summary	40
	References	40

<b>3</b>	<b>Automated Generation of Directed Tests</b>	43
3.1	Introduction	43
3.2	Related Work	44
3.3	The Workflow of Model Checking Based Test Generation	45
3.4	Coverage-Driven Property Generation	46
3.4.1	Safety Property and Its Negation	46
3.4.2	Testing Adequacy Using Model Checking	48
3.4.3	Fault Models	48
3.4.4	Functional Coverage Based on Fault Models	51
3.5	Test Generation Using Model Checking Techniques	51
3.5.1	Test Generation Using Unbounded Model Checking	51
3.5.2	Test Generation Using Bounded Model Checking	52
3.6	Case Studies	54
3.6.1	A Control System	55
3.6.2	A Stock Exchange System	56
3.7	Chapter Summary	57
	References	58
<b>4</b>	<b>Functional Test Compaction</b>	61
4.1	Introduction	61
4.2	Manufacturing Test Reduction Techniques	61
4.2.1	Test Compression	63
4.2.2	Test Compaction	63
4.2.3	Applicability and Limitations	65
4.3	Functional Test Compaction	67
4.3.1	Binary Format of FSM Models	68
4.3.2	Number of FSM States and Transitions	70
4.3.3	Property Compaction of FSM States and Transitions	71
4.3.4	FSM Coverage-Driven Test Selection and Generation	73
4.3.5	A Case Study	74
4.4	Chapter Summary	76
	References	76
<b>5</b>	<b>Property Clustering and Learning Techniques</b>	79
5.1	Introduction	79
5.2	Related Work	80
5.3	Background: SAT Solver Implementation	81
5.3.1	DPLL Algorithm	81
5.3.2	Conflict Clause	82
5.4	Property Clustering	84
5.4.1	Similarity Based on Structural Overlap	85
5.4.2	Similarity Based on Textual Overlap	86
5.4.3	Similarity Based on Influence	87
5.4.4	Similarity Based on CNF Intersection	88
5.4.5	Determination of Base Property	88

5.5	Conflict Clause Based Test Generation . . . . .	89
5.5.1	Conflict Clause Forwarding Techniques. . . . .	89
5.5.2	Name Substitution for Computation of Intersections . . . .	91
5.5.3	Identification and Reuse of Common Conflict Clauses . . .	92
5.6	Case Studies . . . . .	93
5.6.1	A MIPS Processor. . . . .	94
5.6.2	A Stock Exchange System . . . . .	102
5.7	Chapter Summary . . . . .	104
	References . . . . .	105
<b>6</b>	<b>Decision Ordering Based Learning Techniques . . . . .</b>	<b>107</b>
6.1	Introduction . . . . .	107
6.2	Related Work . . . . .	108
6.3	Decision Ordering Based Learnings . . . . .	108
6.3.1	Motivation . . . . .	109
6.3.2	Bit Value Ordering . . . . .	110
6.3.3	Variable Ordering . . . . .	111
6.3.4	Hybrid Learning from Conflict Clauses and Decision Ordering . . . . .	112
6.4	Test Generation Using Decision Ordering Techniques . . . . .	113
6.4.1	Test Generation for a Single Property . . . . .	114
6.4.2	Test Generation for Similar Properties. . . . .	116
6.5	Case Studies . . . . .	119
6.5.1	Intra-Property Learning . . . . .	119
6.5.2	Inter-Property Learning . . . . .	123
6.6	Chapter Summary . . . . .	127
	References . . . . .	127
<b>7</b>	<b>Synchronized Generation of Directed Tests . . . . .</b>	<b>129</b>
7.1	Introduction . . . . .	129
7.2	Related Work . . . . .	130
7.3	Synchronized Test Generation. . . . .	130
7.3.1	Correctness of STG. . . . .	135
7.3.2	Implementation Details . . . . .	136
7.4	Case Studies . . . . .	137
7.4.1	A Stock Exchange System . . . . .	137
7.4.2	A MIPS Processor. . . . .	140
7.5	Chapter Summary . . . . .	142
	References . . . . .	142

<b>8</b>	<b>Test Generation Using Design and Property Decompositions . . . . .</b>	<b>145</b>
8.1	Introduction . . . . .	145
8.2	Related Work . . . . .	147
8.3	Decomposition of Design and Property . . . . .	148
8.3.1	Design Decomposition. . . . .	149
8.3.2	Property Decomposition. . . . .	150
8.4	Decompositional Test Generation . . . . .	155
8.4.1	Test Generation Using Module-Level Partitioning. . . . .	158
8.4.2	Test Generation Using Path-Level Partitioning . . . . .	160
8.5	Merging Partial Counterexamples . . . . .	161
8.6	A Case Study . . . . .	162
8.6.1	Module-Level Decomposition. . . . .	163
8.6.2	Group-Level Decomposition Based on Time Step. . . . .	164
8.6.3	Discussion: Applicability and Limitations . . . . .	166
8.7	Chapter Summary . . . . .	166
	References . . . . .	166
<b>9</b>	<b>Learning-Oriented Property Decomposition Approaches . . . . .</b>	<b>169</b>
9.1	Introduction . . . . .	169
9.2	Related Work . . . . .	170
9.3	Learning-Oriented Property Decomposition . . . . .	171
9.3.1	Spatial Property Decomposition . . . . .	171
9.3.2	Temporal Property Decomposition . . . . .	174
9.4	Decision Ordering Based Learning Techniques . . . . .	176
9.5	Test Generation Using Decomposition and Learning Techniques . . . . .	178
9.6	An Illustrative Example . . . . .	179
9.6.1	Spatial Decomposition. . . . .	179
9.6.2	Temporal Decomposition. . . . .	180
9.7	Case Studies . . . . .	181
9.7.1	A MIPS Processor. . . . .	181
9.7.2	A Stock Exchange System . . . . .	182
9.8	Chapter Summary . . . . .	183
	References . . . . .	184
<b>10</b>	<b>Directed Test Generation for Multicore Architectures . . . . .</b>	<b>185</b>
10.1	Introduction . . . . .	185
10.2	Related Work . . . . .	186
10.3	Test Generation for Multicore Architectures . . . . .	187
10.3.1	Correctness of TGMA . . . . .	191
10.3.2	Implementation Details . . . . .	193
10.3.3	Heterogeneous Multicore Architectures . . . . .	194

10.4	Case Studies . . . . .	195
10.4.1	Experimental Setup . . . . .	195
10.4.2	Results. . . . .	196
10.5	Chapter Summary . . . . .	199
	References . . . . .	199
<b>11</b>	<b>Test Generation for Cache Coherence Validation . . . . .</b>	<b>201</b>
11.1	Introduction . . . . .	201
11.2	Related Work . . . . .	202
11.3	Background and Motivation . . . . .	203
11.4	Test Generation for Transition Coverage . . . . .	204
11.4.1	SI Protocol. . . . .	205
11.4.2	MSI Protocol . . . . .	206
11.4.3	MESI Protocol . . . . .	208
11.4.4	MOSI Protocol . . . . .	209
11.5	Case Studies . . . . .	210
11.6	Chapter Summary . . . . .	213
	References . . . . .	213
<b>12</b>	<b>Reuse of System-Level Validation Efforts . . . . .</b>	<b>215</b>
12.1	Introduction . . . . .	215
12.2	Related Work . . . . .	216
12.3	RTL Test Generation from TLM Specifications . . . . .	217
12.3.1	Automatic TLM Test Generation . . . . .	217
12.3.2	Translation from TLM Tests to RTL Tests. . . . .	219
12.3.3	A Prototype Tool for TLM-to-RTL Validation Refinement. . . . .	222
12.4	Case Studies . . . . .	224
12.4.1	A Router Example . . . . .	224
12.4.2	A Pipelined Processor Example . . . . .	228
12.5	Chapter Summary . . . . .	233
	References . . . . .	233
<b>13</b>	<b>Conclusions . . . . .</b>	<b>235</b>
13.1	Summary . . . . .	235
13.2	Future Directions. . . . .	237
	<b>Appendix A: Acknowledgments of Copyrighted Materials . . . . .</b>	<b>239</b>
	<b>Index . . . . .</b>	<b>243</b>

System-Level Validation

High-Level Modeling and Directed Test Generation

Techniques

Chen, M.; Qin, X.; Koo, H.-M.; Mishra, P.

2013, XXII, 250 p., Hardcover

ISBN: 978-1-4614-1358-5