

# Preface

This book presents methodologies for embedded systems design, using field programmable gate array (FPGA) devices, for the most modern applications. This manuscript covers state-of-the-art research from academia and industry on a wide range of topics, including applications, advanced electronic design automation (EDA), novel system architectures, embedded processors, arithmetic, and dynamic reconfiguration.

The book organization is based on 11 chapters, which cover different issues and deal with alternative scientific issues and industrial areas. The description of each chapter in a more analytical manner is as follows:

Chapter 1 presents a lightweight extension to statically scheduled microarchitectures for speculative execution: PreCoRe. Its judicious use of an efficient dynamic token model allows to predict, commit, and replay speculation events. Even if the speculation fails continuously, no additional execution cycles are required over the original static schedule. PreCoRe relies on MARC II, a high-performance multi-port memory system based on application-specific coherency mechanisms for distributed caches, and on RAP, a technique to efficiently resolve memory dependencies for speculatively reordered accesses.

The field which Chap. 2 deals with is decimal arithmetic. The importance of decimal for computer arithmetic has been further and definitely recognized by its inclusion in the recent revision of the IEEE-754 2008 standard for floating-point arithmetic. The authors propose a new iterative decimal divider. The divider uses the Newton–Raphson iterative method, with an initial piecewise approximation calculated with a minimax polynomial, and is able to take full advantage of the embedded binary multipliers available in today’s FPGA technologies. The comparisons of the implementation results indicate that the proposed divider is very competitive in terms of area and latency and better in terms of throughput when compared to decimal dividers based on digit-recurrence algorithms.

Chapter 3 presents the design and mapping of a low-cost logic-level aging sensor for FPGA-based designs. The mapping of this sensor is designed to provide controlled sensitivity, ranging from a warning sensor to a late transition detector. It provides also a selection scheme to determine the most aging-critical paths at which

the sensor should be placed. Area, delay, and power overhead of a set of sensors mapped for most aging-critical paths of representative designs are very modest.

Chapter 4 is devoted to complex event processing (CEP), which extracts meaningful information from a sequence of events in real-time application domains. This chapter presents an efficient CEP framework, designed to process a large number of sequential events on FPGAs. Key to the success of this work is logic automation generated with our C-based event language. With this language, both higher event-processing performance and higher flexibility for application designs than those with SQL-based CEP systems have been achieved.

Chapter 5 outlines an approach to model the DPR datapath early in the design cycle using queueing networks. The authors describe a method of modeling the reconfiguration process using well-established tools from queueing theory. By modeling the reconfiguration datapath using queueing theory, performance measures can be estimated early in the design cycle for a wide variety of architectures with nondeterministic elements. This modeling approach is essential for experimenting with system parameters and for providing statistical insight into the effectiveness of candidate architectures. A case study is provided to demonstrate the usefulness and flexibility of the modeling scheme.

Chapter 6 is dedicated to switch design for soft interconnection networks. The authors first present and compare the traditional implementations that are based on separate allocator and crossbar modules, and then they expand the design space by presenting new soft macros that can handle allocation and multiplexing concurrently. With the new macros, switch allocation and switch traversal can be performed simultaneously in the same cycle, while still offering energy-delay efficient implementations.

Chapter 7 presents advanced techniques, methods, and tool flows that enable embedded systems implemented on FPGAs to start up under tight timing constraints. Meeting the application deadline is achieved by exploiting the FPGA programmability in order to implement a two-stage system start-up approach, as well as a suitable memory hierarchy. This reduces the FPGA configuration time as well as the start-up time of the embedded software. An automotive case study is used to demonstrate the feasibility and quantify the benefits of the proposed approach.

Chapter 8 looks at the structure of a scalable architecture where the number of processing elements might be adapted at run-time, by means of exploiting a run-time variable parallelism throughout the dynamic and partial reconfiguration feature of modern FPGAs. Based on this proposal, a scalable deblocking filter core, compliant with the H.264/AVC and SVC standards, has been designed. This scalable core allows run-time addition or removal of computational units working in parallel.

Chapter 9 introduces a new domain-specific language (DSL) suited to the implementation of stream-processing applications on FPGAs. Applications are described as networks of purely dataflow actors exchanging tokens through unidirectional channels. The behavior of each actor is defined as a set of transition rules using pattern matching. The suite of tools currently comprises a reference interpreter and a compiler producing both SystemC and synthesizable VHDL code.

In Chap. 10, two compact hardware structures for the computation of the CLEFIA encryption algorithm are presented, one structure based on the existing state of the art and another a novel structure with a more compact organization. The implementation of the 128-bit input key scheduling in hardware is also herein presented. This chapter shows that, with the use of the existing embedded FPGA components and a careful scheduling, throughputs above 1 Gbit/s can be achieved with a resource usage as low as 238 LUTs and 3 BRAMs on a Virtex-4 FPGA.

Last but not least, Chap. 11 proposes a systematic method to evaluate and compare the performance of physical unclonable functions (PUFs). The need for such a method is justified by the fact that various types of PUFs have been proposed so far. However, there is no common method that can fairly compare them in terms of their performances. The authors propose three generic dimensions of PUF measurements and define several parameters to quantify the performance of a PUF along these dimensions. They also analyze existing parameters proposed by other researchers.

Throughout the above chapters of the book the reader has a deep point of view in detailed aspects of technology and science, with state-of-the-art references to the following topics like:

- A variety of methodologies for modern embedded systems design
- Implementation methodologies presented on FPGAs
- A wide variety of applications for reconfigurable embedded systems, including communications and networking, application acceleration, medical solutions, experiments for high energy, cryptographic hardware, inspired systems, and computational fluid dynamics

The editors of the *Embedded Systems Design with FPGAs* book would like to thank all the authors for their high-quality contributions. Special thanks must be given to the anonymous reviewers, for their valuable and useful comments on the included chapters.

Last but not least, special thanks to Charles Glaser and his team in Springer for the best work they all did regarding this publication.

We hope that this publication will be a reference of great value for the scientists and researchers to move forward with added value, in the areas of embedded systems, FPGAs technology, and hardware system designs.

Blacksburg, VA, USA  
Chania, Crete, Greece  
Pyrgos, Greece

Peter Athanas  
Dionisios Pnevmatikatos  
Nicolas Sklavos

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Athanas, P.; Pnevmatikatos, D.; Sklavos, N. (Eds.)

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