

Chapter 2

Nullors, Their Bipolar and CMOS Implementations and Applications in Analog Circuit Synthesis and Design

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2.1 Introduction

Analog circuits using the traditional voltage mode (VM) op-amps suffer from the well-known drawbacks resulting from the limited slew rate, gain-bandwidth conflict and requirements of passive component-matching in the realization of several functions (such as controlled current sources, non-inverting integrators/differentiators and variable gain differential/instrumentation amplifiers, to name a few). The requirement of component-matching quite often leads to increased sensitivities and may even cause instability in several cases.

During the past four decades, a number of research groups around the world have toiled with the idea of searching for a universal analog building block overcoming the aforementioned limitations. Of various building blocks proposed so far, nullors have been regarded to be universal building blocks since the four controlled sources and all existing analog circuit building blocks can be represented using only nullors

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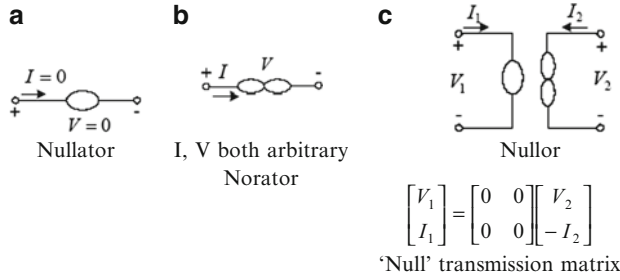


Fig. 2.1 Symbols and definitions of nullator, norator and nullor

and resistors. The floating nullor is a special form of nullor in which ground is external to the four terminals forming the two-port (with nullator comprising the input port and norator comprising the output port).

Although the origin of the concept of nullor itself was advanced as early as 1961–1964, by Carlin and Youla [1, 2] till about 1984 or so, these elements were largely regarded as theoretical concepts useful only in generating equivalent networks of BJT and Op-Amp based circuits such as gyrators and impedance converters/inverters. However, over the years, nullors have attracted a lot of attention in literature and there have been a large number of publications dealing with applications and implementations of nullors, for instance, see [3] and the references cited therein. It was shown by a number of researchers (such as Nordholt [4], Stevenson [5], Huijsing [6] and Senani [7] (who coined the term “four-terminal floating-nullor” (FTFN) to represent a fully floating nullor) that fully floating versions of Op-Amps [termed as operational floating amplifier (OFA)] and FTFNs are more versatile and flexible building blocks than the traditional op-amps in several applications. Thus, the “OFA” and “FTFN” got going and soon attracted the attention of circuit designers as attractive building blocks for a number of voltage-mode and current-mode signal processing applications. In most of the investigations, the FTFNs have been realized by a composite connection of two CCII_s as suggested by Senani in [7]. The current feedback op-amp AD844 from Analog Devices, which embodies a CCII₊ followed by an on-chip buffer, became a preferred choice for implementing FTFNs using the quoted formulation (shown explicitly in Fig. 2.7d in this chapter). However, it is the CMOS implementability of the concept of FTFN which has brought it to the forefront of analog design in more recent years. A number of CMOS implementations of the FTFNs are now known, for instance, see [8–11] and references cited therein.

In this chapter, we deal with the nullors, particularly the floating ones namely, the FTFNs or OFAs, their hardware implementations and applications in circuit synthesis and design.

The symbolic notation and characterizing equations for nullator, norator and nullor have been depicted in Fig. 2.1.

2.2 Nullor Representation of Various Analog Circuit Building Blocks

Since the evolution of nullors, the utility of nullor representation of ideal transistors (both BJT, FET) and the ideal Op-Amps was soon understood [12]. Subsequently, nullors have also been used to model other active building blocks which came into existence later on. Thus, it is well known that an ideal BJT as well as an ideal FET/MOSFET is a three-terminal nullor (see Fig. 2.2a); an ideal op-amp is also a three-terminal nullor with its input terminals representing a nullator and the output terminal with respect to the ground representing the norator; see Fig. 2.2b. A CCII— is equivalent to a three-terminal nullor (Fig. 2.3). This equivalence and the basic properties of nullators and norators and different ways of combining these have been used by Senani [13] and Higashimura and Fukui [14, 15] to synthesize a number of interesting CCII—based inductance simulation circuits.

In principle, since all the four controlled sources (namely, the voltage-controlled/current-controlled voltage/current sources) can be represented by nullators, norators and resistors, a CCII+ can also be represented by nullors but requires two resistors in addition (see Fig. 2.4).

A nullor representation of an operational transconductance amplifier (OTA), voltage follower (VF) and current follower (CF) are shown in Fig. 2.5.

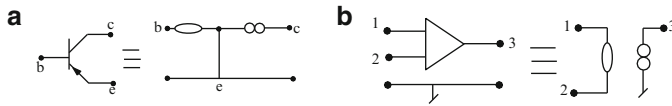


Fig. 2.2 Nullor models of active devices: (a) Ideal transistor (BJT). (b) Ideal op-amp

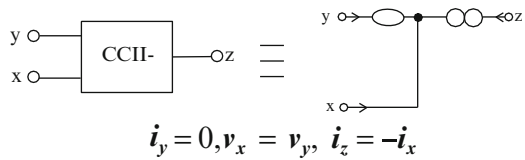


Fig. 2.3 Nullor model of CCII—

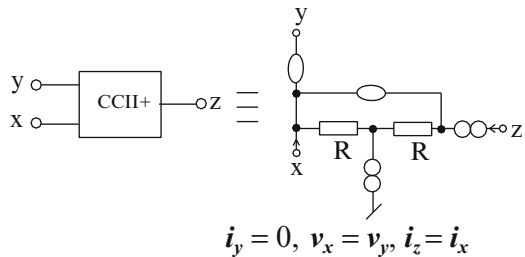


Fig. 2.4 Nullor model of CCII+

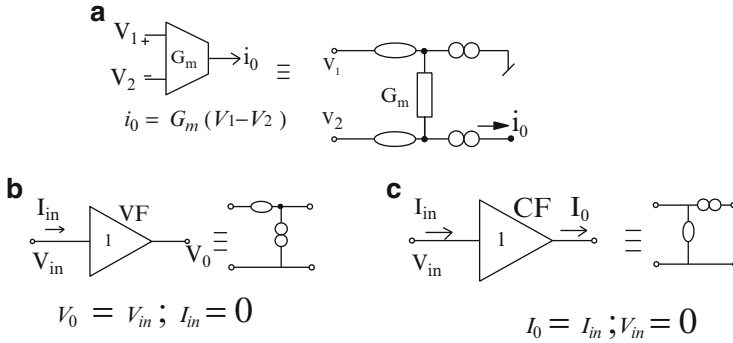


Fig. 2.5 Nullor model of other active building blocks. (a) Nullor model of an OTA. (b) Nullor model of a VF. (c) Nullor model of a CF

Since nullors can be used to represent a variety of active elements, they provide a unified framework not only for analysis, synthesis and design of active networks but also for inter-relating the realizations using different active elements. This fact will be unfolded in subsequent sections of this chapter. However, before proceeding further, we briefly look into the advent of OFAs and FTFNs.

2.3 The Advent of OFA and FTFN

Nordholt in 1982 [4], presented a method of extending op-amp capabilities using current source power supplies. This “extended op-amp” represented a four-port active element which was loosely equivalent to a floating nullor.

Another op-amp-based floating nullor was employed by Stevenson in 1984 in realizing two-way circuits with inverse transmission properties in [5]. This floating nullor circuit was derived from a three-terminal nullor realized with two op-amps, proposed earlier by Cox, Su and Woodland in 1971 [16].

Huijsing in [6, 17], introduced the concept of an OFA which is same as a floating nullor (Fig. 2.6). It was demonstrated that an OFA is particularly useful in realizing current amplifiers, gyrators and instrumentation amplifier with a minimum possible number of external passive components in contrast to conventional op-amp-based circuits for the same functions and hence, an OFA can be regarded to be a versatile building block.¹

¹For a differential difference version of an OFA, see [18].

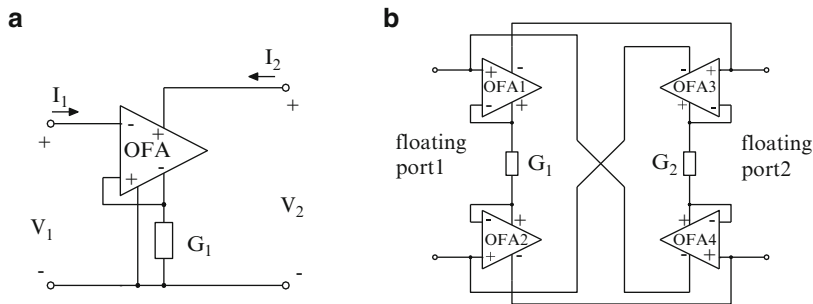


Fig. 2.6 OFA-based circuits (adapted from [17] © 1993 Springer). (a) V to I converter $I_1 = G_1 V_1$. (b) Floating gyrator ($I_1 = G_2 V_2$, $I_2 = -G_1 V_1$)

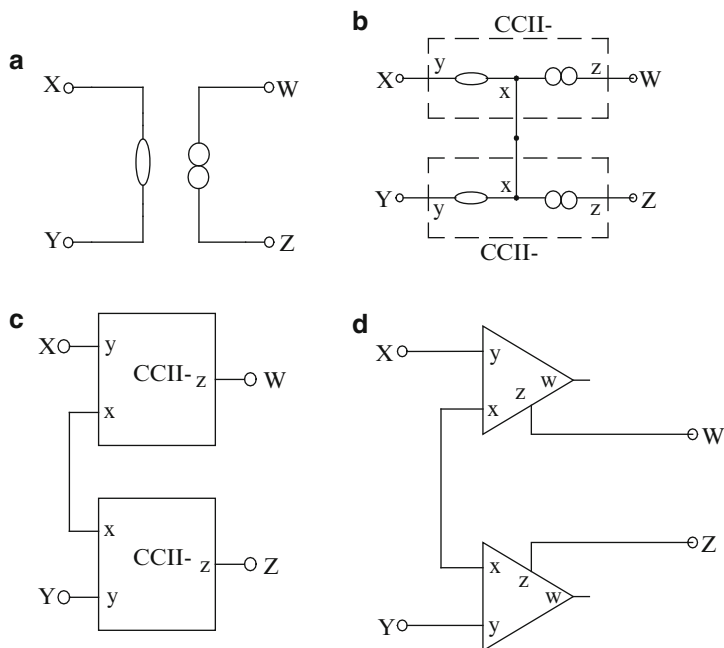


Fig. 2.7 A FTFN implementation using CCII Θ . (a) FTFN. (b) A FTFN using two three-terminal nullors. (c) FTFN using two CCII Θ . (d) FTFN using two CFOAs

It was shown by Senani in [7, 13] that FTFNs provide a novel solution to the problem of RC active synthesis of floating impedances. A discrete implementation of the FTFN using only an op-amp, OTA and a resistance was proposed in [7]. It was also suggested in [7] that a composite connection of two CCII Θ can be used to realize an FTFN (see Fig. 2.7a–c of this chapter). This follows from the fact that the representation of FTFN of Fig. 2.7a is equivalent to the combination of two 3-terminal nullors as shown in Fig. 2.7b where each 3-terminal nullor is equivalent to a

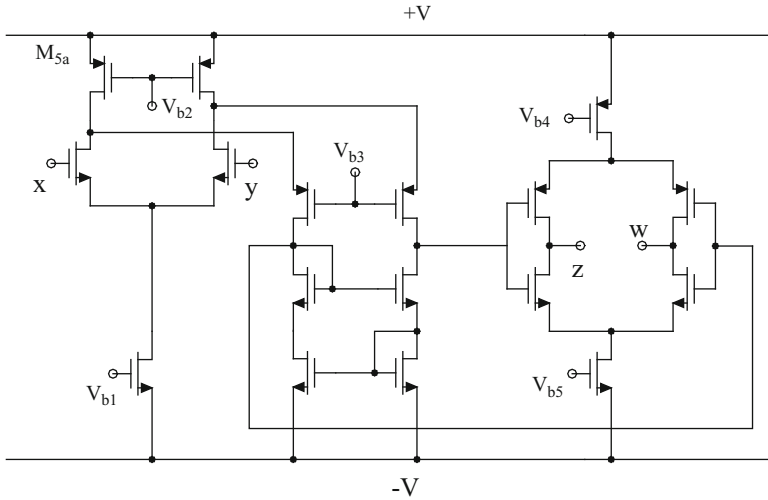


Fig. 2.9 CMOS FTFN proposed by Cam and Kuntman (adapted from [10] © 2000, Taylor and Francis)

worked out a number of CMOS implementations of the FTFN. Because of space limitations, it is difficult to describe all bipolar/CMOS OFAs/FTFNs reported so far, the discussion would be limited to a few representative implementations only.

In 1999, Cam and Kuntman presented a CMOS implementation of two circuits that realize FTFNs [8]. Both these implementations were based on CMOS CCII—architecture. In yet another proposition in 2000, Cam, Toker and Kuntman [9] presented a CMOS implementation of FTFN based on translinear cells. Though not mentioned there explicitly, this implementation is in fact, an interconnection of two translinear CCII+- conforming to the scheme of Fig. 2.7b.

Cam and Kuntman in [10] proposed another CMOS realization of the FTFN which combines the advantages of a cascade of common-source and common-gate amplifiers and a floating current source. This circuit was shown to exhibit wideband operation (unity gain bandwidth in excess of 250 MHz) with a wide dynamic range. Fig. 2.9 shows the circuit proposed in [10].

Tansritat, Unhavanich, Dumawipata and Surakompontrorn [24] presented a bipolar implementation of an FTFN with variable current gain which they termed as a tunable FTFN. This implementation is a modification of the basic supply current sensing method for the realization of FTFN. Jiraseri-amornkun, Chipipop and Surakompontrorn [25] presented another bipolar implementation of an FTFN with multiple complementary outputs. This implementation is based on a transconductor and an improved translinear cell wherein a number of CMs have been used to replicate the output currents (see Fig. 2.10).

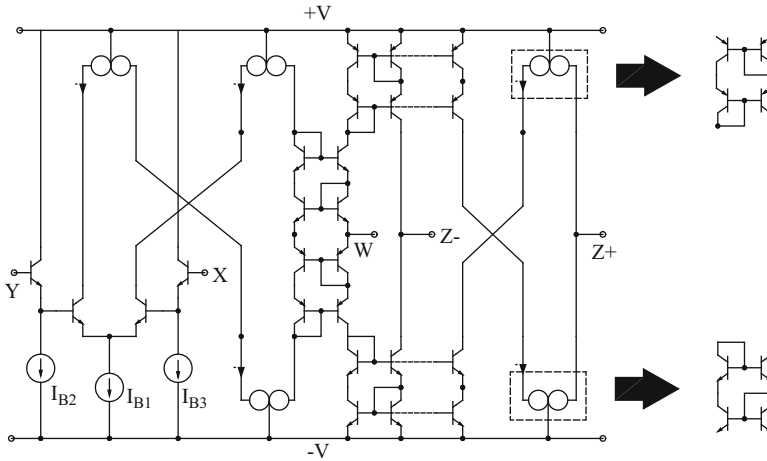


Fig. 2.10 Bipolar implementation of the multiple output floating nullor (adapted from [25] © 2001, IEEE)

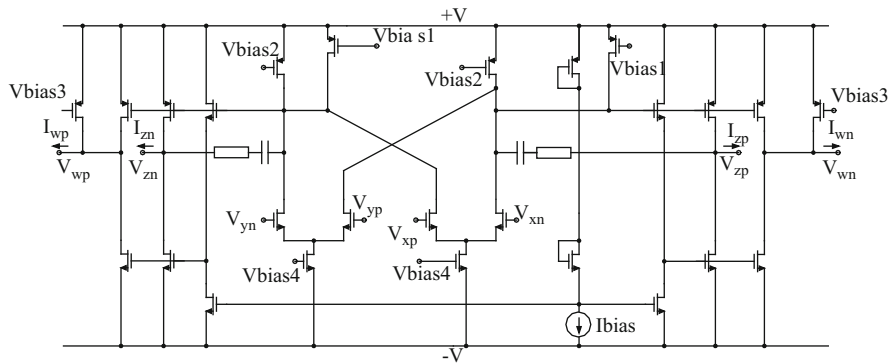


Fig. 2.11 CMOS fully-balanced FTFN (adapted from [11] © 2002, IEEE)

In 2002, Al-Zaher and Ismail in [11] presented the notion of a fully-balanced³ FTFN and its CMOS implementation. They modified the design of the Op-Amp used in supply current sensing mode, by providing two input differential stages. Provision of two balanced outputs was made instead of a single output from the op-amp. These outputs are finally mirrored to the output port of the FTFN. This circuit is shown in Fig. 2.11 and is characterized by the following equations: $I_{xp} = I_{xn} = I_{yp} = I_{yn} = 0$; $V_{dx} = V_{xp} - V_{xn} = V_{dy} = V_{yp} - V_{yn}$; $I_{dz} = I_{zp} - I_{zn} = -(I_{wp} - I_{wn})$.

³For another extension of FTFN or OFA termed as “Differential difference operational floating amplifier”, the reader is referred to [18].

From survey of literature and the exemplary implementations outlined here, the opinion of the authors is that any “perfect” bipolar/CMOS implementation of the FTFN has yet not been achieved.

In the subsequent sections, we will show important applications of nullors/FTFNs in the areas of floating impedance simulation, generation of equivalent oscillators and universal biquad filter realization which may serve as a motivation for developing a fully integrable bipolar/CMOS FTFN as an off-the-shelf IC.

2.5 Novel Applications of FTFN in Impedance Synthesis

Simulated inductors have important applications in the design of both filters and oscillators. The Antoniou’s generalized impedance converter (GIC) [26] based grounded lossless inductance simulation circuit has been the most well-recognized and widely-acceptable solution in many applications. Before the advent of FTFN, the problem of synthesizing floating inductors/impedances (FI) was regarded to be relatively more difficult than that of realizing grounded inductors/impedances. All available circuits/techniques called for either the use of two identical op-amp RC sub-circuits thereby leading to the requirement of double the number of op-amps and RC elements as in [7, 13, 27] or required a large number of resistors with matching constraints and/or cancellation conditions when only two op-amps were employed (as in the circuits of The-Yanagisawa [28]).

A potential application of FTFNs has been in the area of floating impedance simulation where the resulting circuits offer significant advantages as compared to the previously known op-amp RC based FI circuits.

In the following, we highlight a number of techniques of realizing floating impedances of various kinds using the concept of nullors/FTFNs known so far.

2.5.1 Realizing Floating Generalized Impedance Converters/Inverters

The method to be presented here is based upon the following theorem presented in [7] and similar ideas contained in [13]:

Theorem 2.1. *Suppose that a 1-port active network N , containing grounded and floating, two terminal passive elements, nullators and norators realizes a grounded driving point impedance (GDPI) $Y_{11}(s) = y(s)$. If a 2-port network N^* be formulated from N by disconnecting from ground all grounded passive elements and terminals (of grounded nullators and norators) and joining them together to form port 2, then N^* will have short circuit admittance matrix $[Y]_{N^*} = [Y]$ (with $i_1 = -i_2 = y(s)[v_1 - v_2]$).*

For a formal proof of the above theorem, the reader is referred to [7].

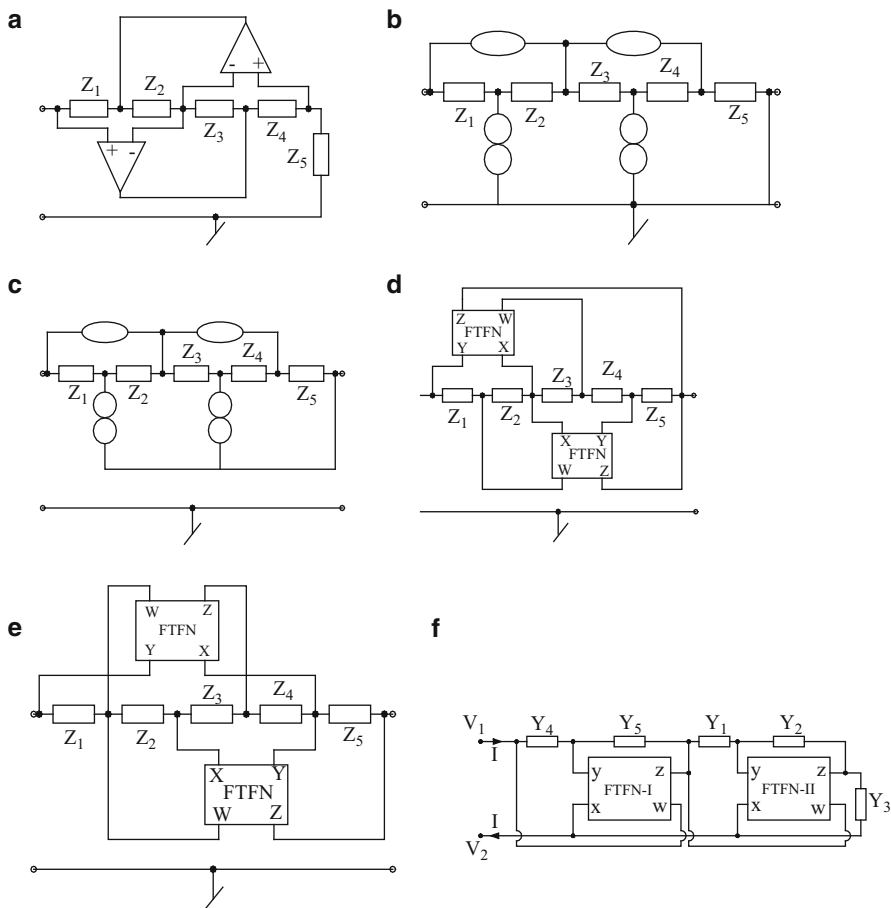


Fig. 2.12 Conversion of GIC-based grounded impedance into FTFN-based floating impedance (a) Antoniou's GIC-based grounded impedance (adapted from [26] © 1969 IEE). (b) The nullor model of the circuit of (a). (c) A floating version of the GIC resulting from the application of Theorem 2.1 [7]. (d) An FTFN-based floating generalized impedance as per the method first introduced in 1987 in [7, 13]. (e) An alternative generalized floating impedance using FTFNs (adapted from [30] © 1997 © 2000 Springer). (f) Another FTFN based generalized floating impedance simulation (adapted from [31] © 2001 Springer)

Consider now the Antoniou's GIC shown in Fig. 2.12a. Figure 2.12b shows the nullor model for the same. In Fig. 2.12c, the two-port obtained by ungrounding both the norators as well as the impedance Z_5 have been shown. Thus, from Theorem 2.1 it follows that the circuit of Fig. 2.12c would realize the same impedance in floating form as the grounded impedance realized by the GIC-based circuit of Fig. 2.12a, i.e.

$$Z(s) = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}$$

An FTFN implementation of the circuit of Fig. 2.12a is shown in Fig. 2.12d. It is, thus, seen that not only one does not require four op-amps and double the number of passive elements (including two capacitors) as required in the known methods of obtaining GIC-based floating impedance (for instance, see [29]) but one does not require any component matching conditions either which are required in the two-GIC-based (hence, four op-amp- based) approach. Note that for inductance simulation, Z_2 or Z_4 is chosen as a capacitor with all other impedances being resistors.

An alternative floating structure of GIC-based generalized floating impedance proposed by Cabeza and Carlosena 1997, [30] is shown here in Fig. 2.12e which also realizes a floating impedance of the same value. Yet another circuit having the same characterization was proposed by Cam, Ozoguz and Kuntman in 2001 [31] as shown here in Fig. 2.12f.

2.5.2 *Generation of CCII Θ -based Floating Generalized Impedance Converters/Inverters*

Consider now the nullor model for generalized impedance converter/inverter shown in Fig. 2.13a taken from one of the models of reference [32]. By a routine analysis, the admittance looking into terminals 1 and 2 is found to be

$$y_0 = \frac{y_1 y_3 y_5}{y_2 y_4}$$

It is immediately clear from this nullor circuit, by appropriately defining the second port, a number of two port immittance inverter/converter circuits can be generated. Since none of the terminals or impedances is connected to ground, Theorem 2.1 applies. Since each pair of nullator, norator has common terminal, both the nullors are realizable with a CCII Θ . It may appear that a total number of six different floating generalized impedance converter/inverter should be derivable from the model of Fig. 2.13a however, after discarding the redundant cases; it is found that only three distinctly different configurations [27] are possible which are shown here in Fig. 2.13b.

It may be pointed out that all the three configurations of Fig. 2.12d–f as well as those of Fig. 2.13b can be used to realize a number of useful floating impedances. In this context, it may be noted that the three most common elements, from the point of view of various active network applications, are the synthetic floating L, floating FDNR ($Z(s) = 1/Ds^2$) and floating FDNC ($Z(s) = Ms^2$) elements. With the proposed GPIC/GPII configurations, these are realizable more efficiently than the CC- based simulations previously known.

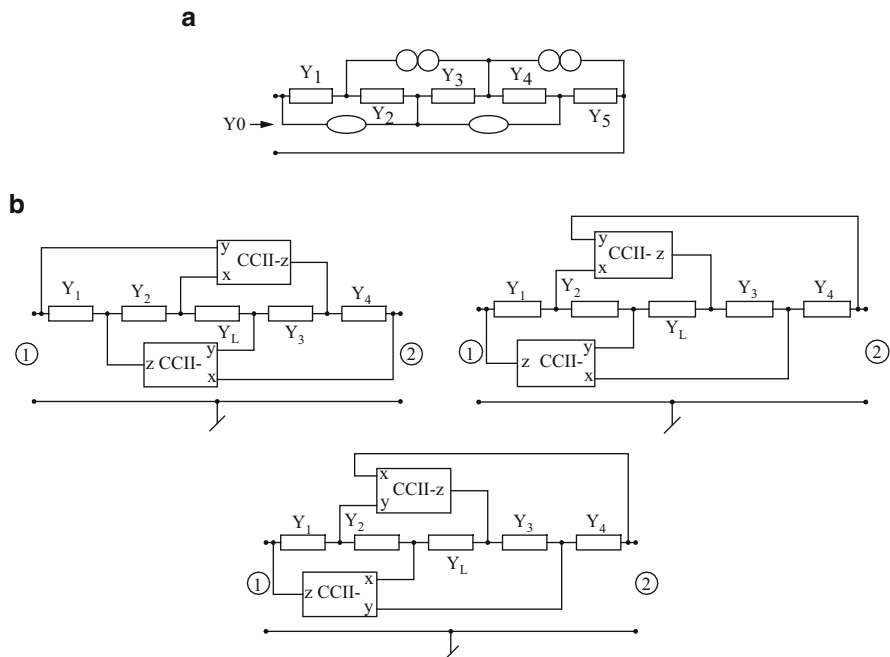


Fig. 2.13 (a) A nullor model of generalized impedance converter/inverter (adapted from [32] © 1970 IEEE). (b) Three CCI-based floating generalized impedance converter/inverter derived from nullor model of (a) (adapted from [27] © 1986 IEEE)

- (a) Synthetic floating inductance (FI)-choosing Z_3 as a capacitor and remaining impedances as resistors, the simulated L is given by

$$L_{1-2} = \frac{C_3 R_1 R_4 R_L}{R_2} \quad (2.1)$$

- (b) Floating FDNR- choosing Z_1 and Z_L as capacitors, the circuit simulates a floating FDNR having value

$$D_{1-2} = \frac{C_1 C_L R_2 R_3}{R_4} \quad (2.2)$$

- (c) Floating FDNC- choosing Z_2 and Z_3 as capacitors, the circuit simulates a floating FDNC having value

$$M_{1-2} = R_1 R_4 R_L C_2 C_3 \quad (2.3)$$

It is worthwhile to point out that the previously published CC-networks simulating floating ideal L or D elements [33–38] use three to four CCs. Also, the ideal floating L (and also the corresponding D element), outlined by Paul and Patranabis [39] as an application example of their proposed floating NIC too employs four CCs. In comparison, the use of the proposed networks of Fig. 2.13b makes it possible to realize these elements with only two FTFNs or two CCs, while providing the merits of lack of any component-matching requirement, low sensitivities to element value changes and single-resistance-tunability of the realized immittances. For the CC-based realization of lossy FIs using nullors see [40].

2.5.3 Generation of Lossless Floating Inductance Circuits Using a Single FTFN

To the best knowledge of the authors, only four single op-amp lossless grounded inductance circuits appear to have been known in the earlier literature till date which were proposed by Orchard-Willson 1974, [41], Schmitt-Lee 1975, [42], Ramsey 1978, [43] and Horn-Moschytz 1979, [44]. Here, we demonstrate how all these four circuits can be transformed as per the techniques of [7, 13] into as many as *sixteen*⁴ lossless FI circuits using Theorem 2.1 in conjunction with Theorem 2.2 (to be outlined subsequently). Consider the grounded inductance simulation circuit of Horn-Moschytz [44] which realizes an inductance value

$$L = CR_3R_6 \left(1 + \frac{R_2}{R_1}\right) \left(1 + \frac{R_5}{R_4}\right)^{-1} \text{ provided } \frac{R_2}{R_4} = \frac{R_1 + R_6}{R_5} + \frac{R_1}{R_3} \left(1 + \frac{R_6}{R_5}\right) \quad (2.4)$$

The process of deriving an FTFN/OFA based FI circuit corresponding to this circuit is shown in Fig. 2.14a to c is self-explanatory.

It is, however, interesting to note that from the FI circuit of Fig. 2.14c, three additional FI circuits can be derived as follows:

- (1) An equivalent of the circuit of Fig. 2.14c can be generated invoking the following theorem:

Theorem 2.2. *If a 2-port active-RC network N_1 containing floating two terminal passive elements, floating nullators and floating norators has short circuit admittance matrix*

$$[Y_1] = y(s) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (2.5)$$

⁴In [13] 32 equivalent FI realizations were stipulated using a two-op-amp FTFN available then.

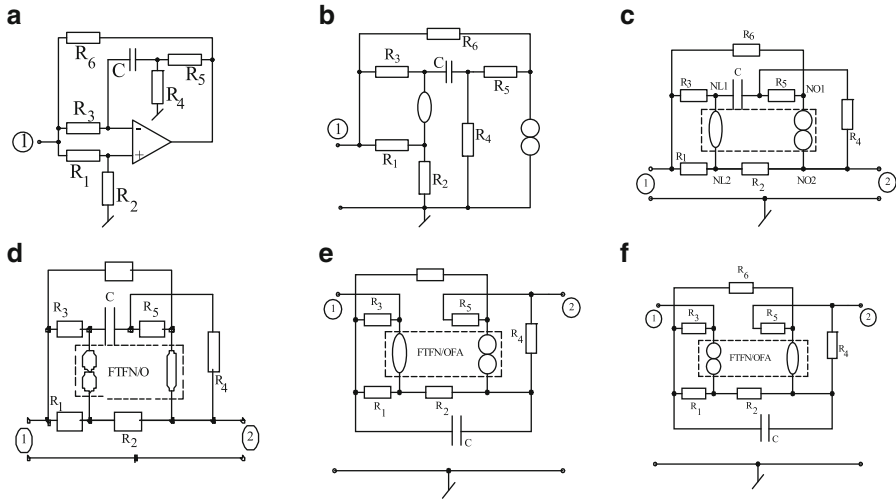


Fig. 2.14 (a–c) Method of transformation of a lossless grounded inductor into a FI using an FTFN or OFA [7, 13]. (d–f) Three other equivalent FIs having same value of realized inductance under the same condition of realization

then if it is transformed into another network N_2 by interchanging all nullators and norators, the transformed network has the same Y -matrix.

By applying Theorem 2.2 to the FI circuits of Fig. 2.14c, the resulting second equivalent FI turns out to be as shown in Fig. 2.14d.

- (2) Owing to simulating a lossless inductance employing a single floating capacitor, the two port network of Fig. 2.14c can be looked upon as a floating gyrator with terminals 1 and 2 constituting the input port and terminals 3 and 4 (between which the capacitor is connected) constituting the output port. Thus, gyrator action is available even if the input and the output ports are transposed i.e. the capacitor is connected between terminals 1 and 2 and the floating impedance is looked between 3 and 4. This results in the third equivalent FI shown in Fig. 2.14e.
- (3) Finally, the fourth and the last additional equivalent FI is obtained by swapping the nullator and norator in the circuit of Fig. 2.14f in accordance with Theorem 2.2.

Lastly, it must be pointed out that twelve additional lossless FI circuits, each employing only a single FTFN, are similarly realizable starting from the lossless grounded inductance circuits of Orchard-Wilson [41], Schmidt-Lee [42] and Ramsey [43] by following the above outlined procedure.

It may be mentioned that the basic ideas outlined above had been elaborated by Senani in [7] and [13].

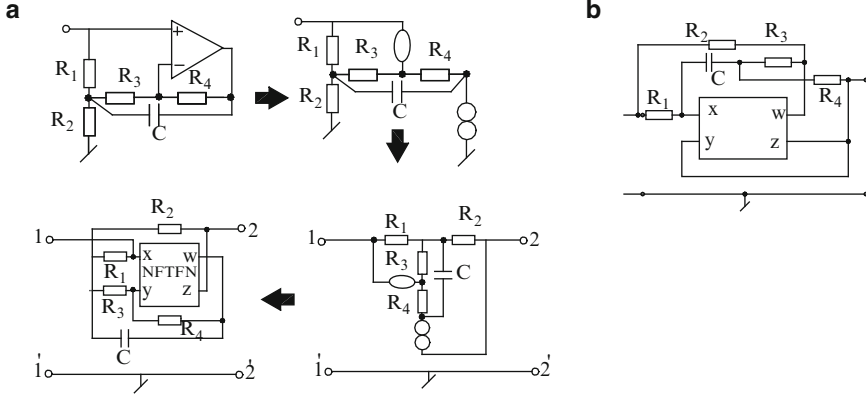


Fig. 2.15 Conversion of an op-amp based single resistance controllable GI into FTFN-based FI of the same form: (a) Floating series RL, (b) floating parallel RL

2.5.4 Single-Resistance-Tunable Lossy Floating Inductance Simulation Using Only a Single FTFN

The technique explained in Sect. 2.5.1 above opens the way for evolving a large number of floating impedance circuits starting from various known grounded GDPI circuits. Figure 2.15 shows the conversion of a simulated single resistance tunable grounded lossy inductance into a FI of the same value. Starting from the grounded inductance circuit of [45], its nullor model is drawn, a two port is created by ungrounding all grounded elements/terminals where from finally, a circuit simulating the same kind of impedance in floating form using FTFN is derivable (see Fig. 2.15).

Thus, GDPI using an op-amp as well as the derived FI using an FTFN both simulate series RL impedance with inductance value given by

$$R_s = R_1 + R_2 + \frac{R_1 R_2}{R_3} \cdot L_s = CR_1 R_2 \left(1 + \frac{R_4}{R_3} \right) \quad (2.6)$$

where from it is seen that L_s is independently adjustable by R_4 which does not appear in the expression for R_s .

A single FTFN-based floating parallel RL impedance possessing single- resistance controllability of inductance value is similarly derivable from the tunable grounded parallel RL impedance circuits of [45] is shown in Fig. 2.15b for which equivalent resistance R_p and inductance L_p are given by

$$\frac{1}{R_p} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{R_3}{R_1 R_2} \right) \cdot L_p = (CR_1 R_2) \left(1 + \frac{R_3}{R_4} \right)^{-1} \quad (2.7)$$

2.6 Use of Nullors in Deriving Equivalent Circuits of Single-Resistance-Controlled Oscillators (SRCO)

Although there have been several efforts in synthesizing oscillators using FTFNs as active elements, for instance, see [46–48] and the references cited therein, the potential of FTFNs has been particularly appealing in generating oscillator-equivalences which quite often have resulted in alternative oscillator topologies possessing properties not available in the parent circuits. In this section, we will, therefore, focus only on this particular application of FTFNs in the domain of oscillator design.

A general theory of deriving equivalent forms of op-amp RC sinusoidal oscillators using the formalism of nullors was presented earlier in [22]. This theory is based upon the following theorems:

Theorem 2.3. *Suppose there is a sinusoidal oscillator N which employs m nullators, m norators and an arbitrary number of passive resistors and capacitors. If N is transformed into another circuit N^* by interchanging all nullators and norators then N^* has the same characteristic equation (CE) as that of N .*

Theorem 2.4. *Corresponding to any RC-nullor oscillator having n nodes (excluding the ground node which is taken “external” to the circuit) and consisting of m nullors along with an arbitrary number of passive resistor and capacitors, there are $2n$ grounded nullor-RC equivalent oscillator circuits having the same CE since in an oscillator, because there is no external input, the ground node can be chosen arbitrarily without affecting the CE.*

In [22] it was shown that the classical Wein bridge oscillator has ten equivalent forms.⁵ This number was further increased in [51] to sixteen by considering the junction of the series RC branch as another node.

It was shown in [22] that some of such additional realizations are likely to have some interesting properties not available in the original circuit.

In the following, we show how applying the above theorems on an existing SRCO we can derive a number of equivalents having same characterization and that some of the derived equivalents indeed have new and interesting properties not available in the original circuit.

Let us now consider the single op-amp RC SRCO of [52] reproduced here in Fig. 2.16.

This oscillator is characterized by the following condition of oscillation (CO) and frequency of oscillation (FO):

$$\frac{R_4}{R_3} = \frac{2R_5}{R_2} \text{ (with } C_1 = C_2 = C) \text{ and } f_0 = \frac{1}{2\pi C} \sqrt{\frac{1 + \left(\frac{R_3+R_4}{R_1}\right)}{R_2 R_3}} \quad (2.8)$$

⁵It is worthwhile to point out that the theory of [22] was usefully extended to derive a class of two FTFN-based SRCOs employing a minimum possible number of resistors in [49]. Yet another two FTFN-based GC SRCO was presented in [50].

Fig. 2.16 Senani's SRCO
(adapted from [52] © 1979
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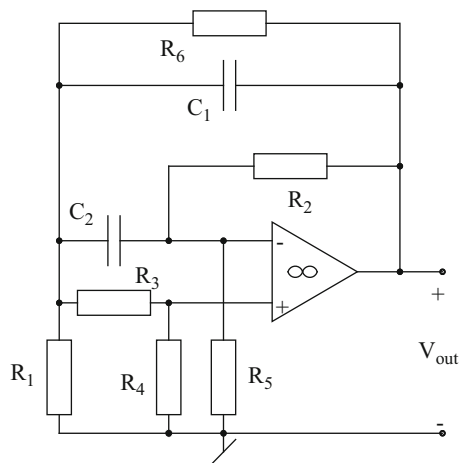
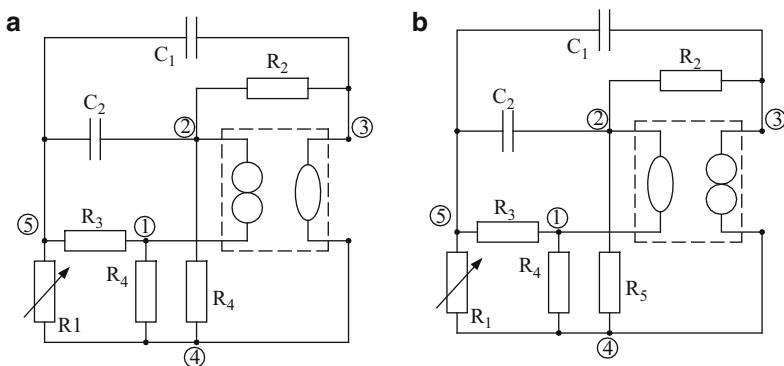


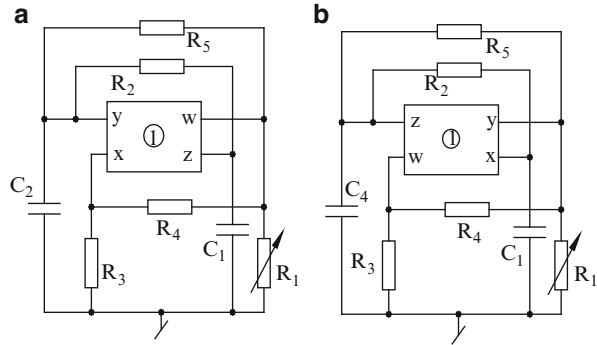
Fig. 2.17 (a) A nullor model of the SRCO of Fig. 2.16. (b) An alternative nullor model of the same circuit

From the above it is seen that CO is controllable independently by R_5 whereas FO is independently controllable by R_1 .

A nullor model of this SRCO, with ground node excluded, is shown in Fig. 2.17a. Figure 2.17b shows an alternative nullor model having the same CE obtained by applying Theorem 2.3. Since each model contains five nodes it follows from Theorem 2.4 that for each model, ground node can be selected in five different ways thereby leading to a total of ten equivalent SRCOs having the same CE. It may be noted that only four of these would be realizable with a normal op-amp while the remaining six require an FTFN (Fig. 2.18).

Two of the new SRCOs generated by this methodology (resulting from treating node 1 as ground) employ grounded capacitors as preferred for IC implementation and are particularly noteworthy since this feature was not present in the original circuit of Fig. 2.16. Also, four of the quoted ten circuits can provide explicit current outputs—again a feature which was not there in the original circuit.

Fig. 2.18 (a) FTFN-based grounded capacitor version of the SRCO of Fig. 2.16. (b) An alternative FTFN-based grounded capacitor version of the SRCO of Fig. 2.16



Thus, the examples in [22, 51] and the one shown here prove the potential of FTFNs in generating new oscillator configurations possessing interesting properties, beyond their normal use as active elements in oscillator realization as demonstrated in [46–48].

2.7 Use of FTFN in Realization of Universal Biquad, Fully Differential and Inverse Filters

In the area of active filter design, the FTFNs have been shown to be very useful building blocks in realizing universal biquad filters, inverse filters and fully differential biquad filters. A brief account of some important works in this direction is provided in the following.

2.7.1 Universal Current-mode Biquad

Although a number of attempts have been made by various researchers in evolving universal biquads in current mode (CM), trans-admittance mode or so the called mixed-mode using a variety of building blocks, a particularly simple CM biquad with a minimum possible number of passive elements (namely only four) along with a minimum possible number of FTFNs to provide three explicit current outputs was proposed by Cicekoglu [53] and is reproduced here in Fig. 2.19.

Selecting $Y_1 = 1/R_1$, $Y_2 = sC_2$, $Y_3 = 1/R_3$, and $Y_4 = sC_4$, the circuit realizes a high pass (HP) response at i_{o1} and a band pass (BP) response at i_{o2} with relevant parameter given by

$$\omega_0 = \sqrt{\frac{1}{R_1 R_3 C_2 C_4}}, \text{ and } Q_0 = \sqrt{\frac{R_3 C_4}{R_1 C_2}} \quad (2.9)$$

Fig. 2.19 Current-mode biquad using FTFN (adapted from [53] © 2001 IEEE)

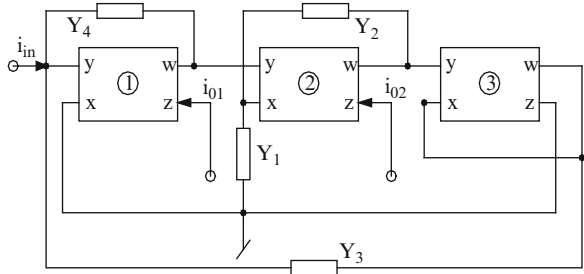
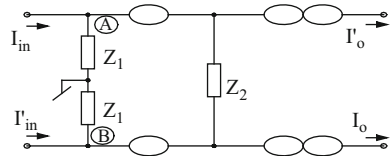


Fig. 2.20 Fully-differential CM building block (adapted from [54])



On the other hand, by selecting $Y_1 = sC_1$, $Y_2 = 1/R_2$, $Y_3 = sC_3$, $Y_4 = 1/R_4$, the same circuit realizes a low pass (LP) response at i_{01} and a BP response i_{02} with relevant parameters being given by

$$\omega_0 = \sqrt{\frac{1}{R_2 R_4 C_1 C_3}} \text{ and } Q_0 = \sqrt{\frac{C_1 R_2}{C_3 R_4}} \quad (2.10)$$

The advantageous features of this circuit are the availability of ideally zero input resistance, ideally infinite output resistances (both expected from an ideal CM filter) together with the use of a minimum possible number of passive elements.

2.7.2 Fully Differential CM Biquad

As another example of the potential of the nullors, we next demonstrate their use in the realization of a fully differential filter. There has been lot of interest in literature in realizing fully differential filters in both VM and CM because of their capability of eliminating common-mode noise. In the following, we discuss a nullor-based approach for constructing a fully differential CM building block which can be used to realize a fully differential CM universal filter in a configuration employing two fully differential integrators and a fully differential summer with complimentary CM outputs. A fully differential CM building block is shown in Fig. 2.20 and is characterized by $i_0 = -i'_0 = Z_1/Z_2(i_{in} - i'_{in})$.

Thus, depending upon the choice (resistive/capacitive) of the impedances Z_1 and Z_2 , this block can realize fully differential scalar, integrator or differentiator. With both impedances as resistors and summing nodes created at nodes “a” and

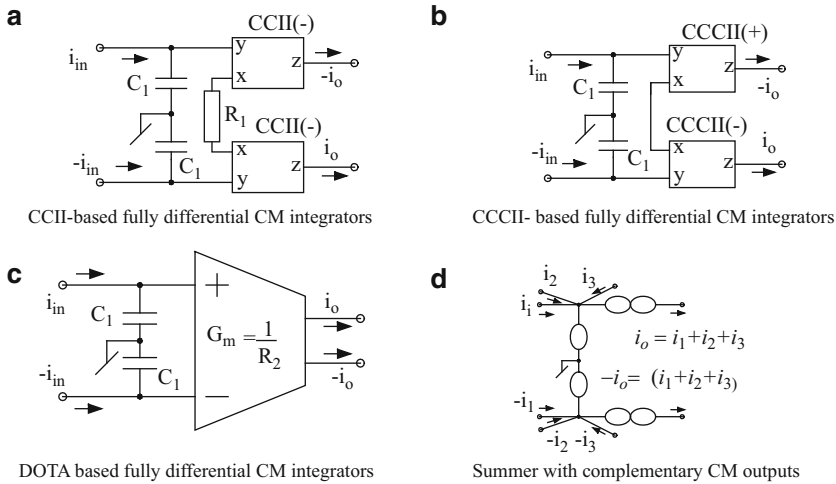


Fig. 2.21 Various realizations of the fully differential CM integrators (adapted from [54])

“b” the configuration can realize fully differential CM summer. We now show that, as widely understood, nullors are indeed useful in realizing and unifying circuit structures using all such different kinds of active elements which can be modeled in terms of nullors. In the present case, the nullor-based configuration of Fig. 2.20 leads to a number of different practical implementations, three of which using CCII–, CCCII+ and differential output OTA (DOTA) are shown in Fig. 2.21.

It is worthwhile to mention that in all cases, the internal hardware of the employed building blocks can be easily modified to facilitate multiple and complementary outputs which should be useful in interconnecting two or more of such configurations as well as to provide feedback paths and summations as needed for either biquad realization or higher order filter designs. Alternatively, differential summer can also be realized by the nullor-based structure of Fig. 2.21d and an exemplary configuration of a fully differential CM universal filter obtained in this manner is shown in Fig. 2.22 which realizes LP, BP, HP outputs where from HP and LP outputs can be combined to realize a band stop filter while HP and BP (inverting) can be combined to realize an all pass filter without requiring any component-matching conditions other than the equality of capacitors (which is prevalent in almost all earlier fully differential filter structures as well). A notable property of the circuit of Fig. 2.22 is that bandwidth and pole frequency can be orthogonally tuned by R_1 and R_2 respectively: the gain is fixed at unity in all the cases. It has been shown elsewhere [54] that this approach can also be extended to the design of higher order filter.

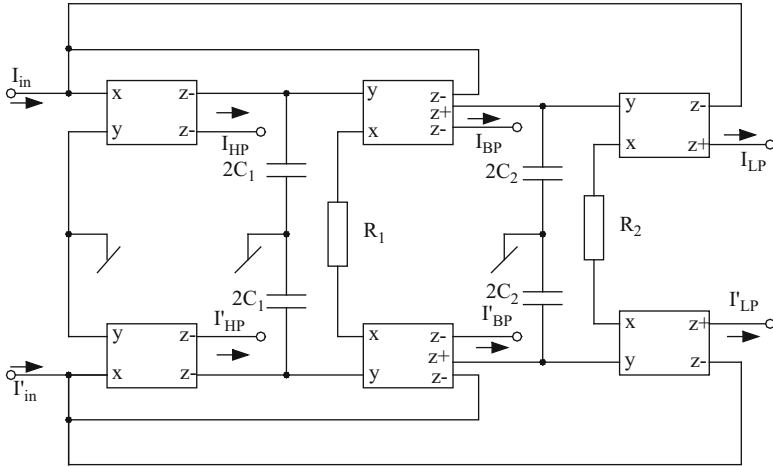


Fig. 2.22 A fully differential CM universal filter (adapted from [54])

The three transfer functions realized by the circuit of Fig. 2.22 are given by

$$\frac{I_{BP}}{I_{in}} = -\frac{s \left(\frac{1}{C_1 R_1} \right)}{\Delta}, \quad \frac{I_{LP}}{I_{in}} = \frac{1}{\Delta}, \quad \frac{I_{HP}}{I_{in}} = \frac{s^2}{\Delta} \quad \text{where} \quad \Delta = s^2 + \frac{s}{C_1 R_1} + \frac{1}{C_1 C_2 R R_2} \quad (2.11)$$

2.7.3 Design of CM Inverse Filter

In the area of filter design another interesting application of FTFNs has been in the derivation of the so-called “inverse filters” [55]. Out of the various approaches of designing inverse filters published earlier, we present here a specific procedure of realizing a current mode FTFN-based inverse filter from a given op-amp RC-based filter based upon [55] which consists of the following steps:

(1) Obtain a nullor model of the given op-amp RC filter by replacing the op-amp by nullator-norator pair, (2) swap the driving source and the norator in the above model, (3) apply RC:CR dual transformation on the model of the previous step, (4) obtain the final inverse filter by replacing the nullors with FTFNs.

An exemplary inverse filter generated by using the above steps, is demonstrated in Fig. 2.23.

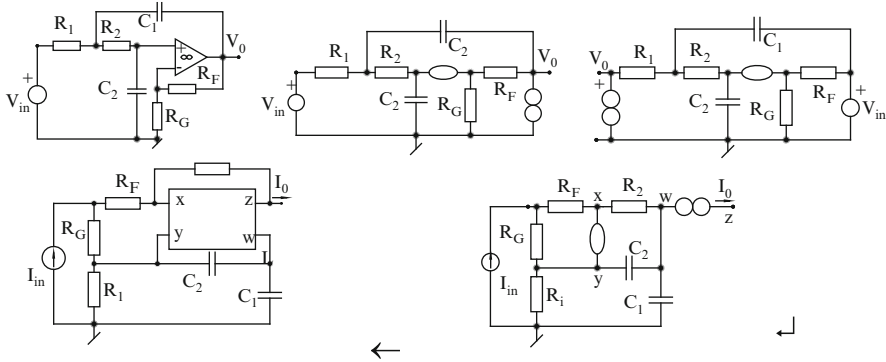


Fig. 2.23 Design of an inverse filter using FTFN (adapted from [55] © 1999 IEE)

The final CM inverse function realized by FTFN circuit of Fig. 2.23 is

$$\frac{I_0}{I_{in}} = \left[\frac{k / (R_1 R_2 C_1 C_2)}{s^2 + s \left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-k}{R_2 C_2} \right) + \frac{1}{R_1 R_2 C_1 C_2}} \right]^{-1} \quad (2.12)$$

where $k = 1 + (R_F/R_G)$.

2.8 Systematic Synthesis of Active RC Circuits Using Nullors

Haigh and co-workers [56] have carried out pioneering work on the systematic synthesis of active RC networks using nullors. While it is difficult to summarize the entire body of their work in a chapter of limited length, we outline here an exemplary synthesis of an immittance inverter circuit which evolves in a systematic way by expansion of the relevant port admittance matrices such that the circuit topology emerges naturally from the synthesis procedure.

We start from the common knowledge that an immittance inverter can be synthesized by a parallel back-to-back connection of a positive voltage controlled current source (VCCS) and a negative VCCS characterized by the two port admittance matrices: $\begin{bmatrix} 0 & 0 \\ G_1 & 0 \end{bmatrix}$ and $\begin{bmatrix} 0 & 0 \\ -G_2 & 0 \end{bmatrix}$ respectively.

Taking the first matrix, we move the element G_1 to the main diagonal so that it can describe a grounded resistor. This is accomplished by adding a blank row 3 and column 3, then moving G_1 term from column 1 to column 3 and from row 2 to row 3 and then adding a nullator between nodes 1 and 3 and a norator between nodes 2 and 3 in order to allow the G_1 term to move to the 3, 3 position, as shown in the following equation:

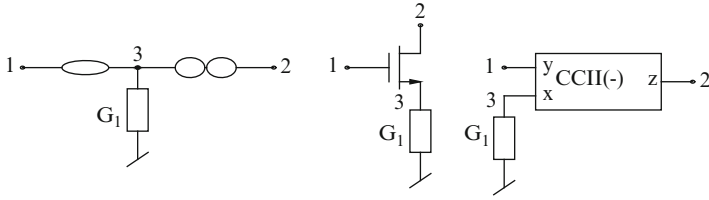


Fig. 2.24 The synthesis of noninverting VCCS and its FET and CCII- realizations (adapted from [56] © 2005 Springer)

$$\left[\begin{array}{ccc|c} 0 & 0 & 0 & 0 \\ G_1 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \end{array} \right] = \left[\begin{array}{ccc|c} 0 & 0 & 0 & 0 \\ G_1 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \end{array} \right] = \left[\begin{array}{ccc|c} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & G_1 \end{array} \right]$$

The circuit realizations corresponding to the last matrix of the above equation are shown in Fig. 2.24.

For the negative VCCS, we note that a negative conductance can be identified with one of the two off-diagonal negative elements describing a non-grounded conductance. The description of non-grounded conductance needs two rows or two columns. Thus, we introduce two blank rows and two blank columns, thereby introducing two new nodes 3 and 4 in the matrix.

$$\left[\begin{array}{cc} 0 & 0 \\ -G_2 & 0 \end{array} \right] \equiv \left[\begin{array}{cccc|c} 0 & 0 & 0 & 0 & 0 \\ -G_2 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{array} \right] \equiv \left[\begin{array}{cccc|c} 0 & 0 & 0 & 0 & 0 \\ -G_2 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{array} \right] \equiv \left[\begin{array}{cccc|c} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -G_2 & 0 & 0 \end{array} \right]$$

Now connecting a nullator from node 3 to node 1 and a norator from node 4 to 2 will permit $-G_2$ to move to position 4, 3. Since an indefinite admittance matrix must have sum of each row and each column equal to zero hence, row 0 and column 0 should contain terms G_2 , $-G_2$ and G_2 , as shown.

$$\left[\begin{array}{cccc|c} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -G_2 & 0 & 0 \end{array} \right] \xrightarrow[G_2]{-G_2} \left[\begin{array}{cccc|c} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -G_2 & 0 & 0 \end{array} \right] \xrightarrow[G_2]{-G_2} \left[\begin{array}{cccc|c} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -G_2 & 0 & 0 \end{array} \right]$$

Now connection of a norator between nodes 3 and 0 will allow the row 0 term to be brought to row 3. Similarly, connection of nullator between nodes 4 and 0 will allow column 0 term to be brought to column 4 as shown. The final admittance matrix in

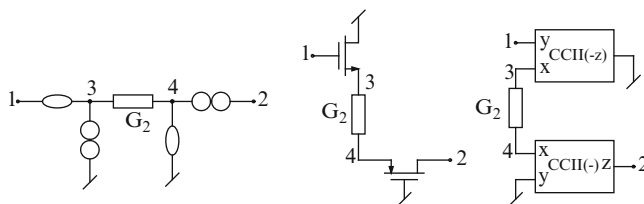


Fig. 2.25 Synthesis of inverting VCCS using nullor MOSFET and CCs (adapted partly from [56] © 2005 Springer)

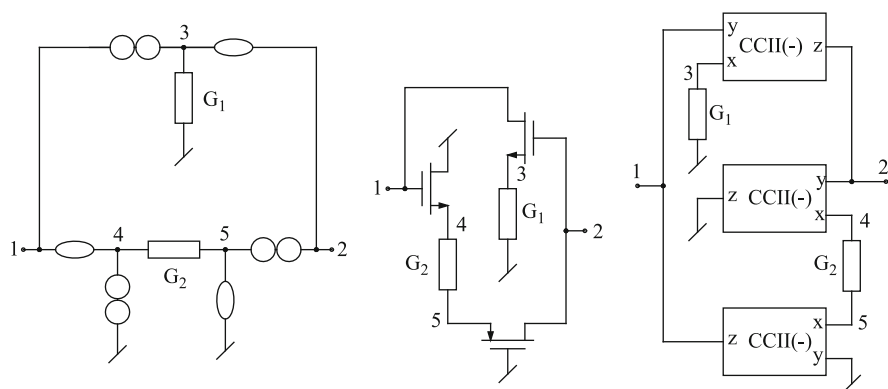


Fig. 2.26 Synthesis of an immittance inverter using nullors, MOSFET and CCII (In the CCII circuits, all three CCII could also be taken as CCII+ (adapted partly from [56] © 2005 Springer)

the above equation shows the connections of two nullors and a floating conductance representing the inverting VCCS, the final circuit for which is shown in Fig. 2.25 along with its FET and CCII– based realizations (not included in [56]).

Finally, the complete nullor representation of the immittance inverter and its FET- and CCII–based realizations are shown in Fig. 2.26.

2.9 Current Mirror and Voltage Mirror as Two New Pathological Elements

While a CCII– can be represented by a three terminal nullor without requiring any resistors, however, a CCII+ cannot be realized by nullators and norators only and does require at least two resistors see Fig. 2.4. This difficulty motivated Awad and Soliman [57, 58] to propose two new pathological elements namely the CM and VM which are basically used to represent active devices with current or voltage reversing properties. A CM is a two port network element for which V_1 and V_2

Fig. 2.27 The symbols of CM and VM (adapted from [58] © 2002 Springer)

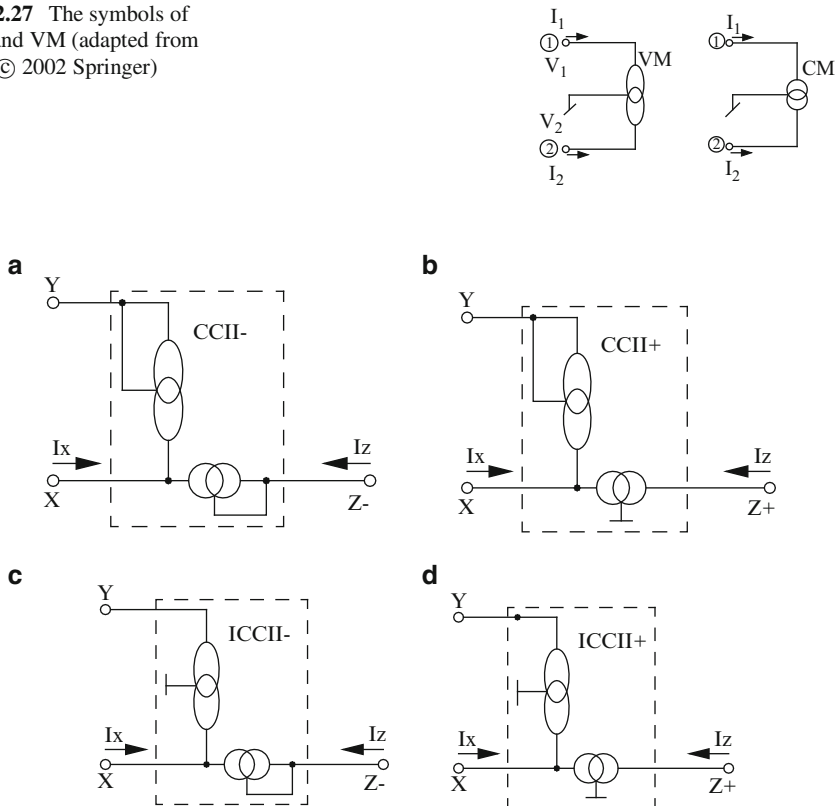


Fig. 2.28 Realization of various building blocks using VM–CM pair. (a) CCII–. (b) CCII+. (c) ICCII–. (d) ICCII+ (adapted from [59] © 2010 John Wiley & Sons)

are arbitrary and $I_1 = I_2$ and they are also arbitrary. The VM is a lossless two-port network element characterized by $V_1 = -V_2$ and $I_1 = I_2 = 0$. The symbolic notations of the CM and VM are shown in Fig. 2.27.

Saad and Soliman in 2010 [59] demonstrated that CM-VM pair constitutes an universal active element since it is capable of representing an op-amp as well as all the four types of current conveyors namely CCII–, CCII+, Inverting CCII– (ICCII–) and inverting CCII+ (ICCII+) without using any resistors (see Fig. 2.28).

Soliman and his co-worker have employed nullator–norator–CM–VM in the systematic synthesis of analog circuits, however, for a detailed discussion of these the reader is referred to [60] and the references cited therein.

2.10 Current Trends and Directions for Future Research

Although about a dozen different CMOS FTFN structures have been reported in literature, a perfect implementation of nullor which can be produced as an IC to take advantage of its universality⁶ is still awaited.

It is also observed from a review of literature that applications of nullors have not been explored as exhaustively as these have been evolved using other devices like operational amplifiers, OTAs, current conveyors and current feedback amplifiers, etc. A good mixed mode universal filter realized with FTFNs providing most of the desirable properties is yet to be evolved and appears to be a worthwhile problem for future investigations.

The more recent works on the utilization of nullors include creation of general admittance matrix stamps for the operational trans-resistance amplifier (OTRA) current output amplifier (COA) [63]. Work is also being conducted by Tlelo-Cuautle and his co-workers [64] on the pathological element based active device modeling and their applications to symbolic analysis. The concept of nullors has also been employed in developing systematic synthesis procedure for realizing CFs and VMs [65].

Thus, continued work on nullors is currently dominantly motivated by the evolution of systematic synthesis procedures using nullator–norator–CM–VM elements for realizing impedance converter inverters, biquad filters and oscillators and it is expected that nullors (or FTFNs) in conjunction with CM–VM pair will continue to find more and more interesting applications in circuit synthesis and design, in days to come.

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⁶It is worth pointing out that it has been shown in [61] that there are nine distinctly different analog building blocks which can be said to be “universal” in a generic sense. Also, it may be noted that as pointed out in [40] and [62], the so called PFTFN or FTFN+-(based on norator +) are strictly speaking not floating nullors and hence, are not included in this chapter.

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